Minimum Unit Capacitance Calculation for Binary-Weighted Capacitor Arrays

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***Abstract*—The layout area and power consumption of a binary-weighted capacitive digital-to-analog converter (DAC) increases exponentially with the number of bits. To meet linearity targets, unit capacitors should be large enough to limit errors caused by various sources of noise and those due to mismatch. This work proposes a systematic approach for minimizing the unit capacitance value that optimizes the linearity metrics of a DAC, accounting for multiple factors that contribute to mismatch, as well as the impact of flicker and thermal noise.**

I. Introduction

The accuracy and performance of charge-scaling digital-to-analog converters (DACs) (Fig. 1(a)) depend on binary-weighted capacitor ratios, which may be perturbed by mismatch. A critical factor is the choice of the unit capacitor, C_u, in the capacitor array. Since an N-bit binary-weighted DAC uses 2^N unit capacitors to provide the required capacitor ratios, its area, total capacitance, and power increase exponentially with N. Selecting a smaller C_u reduces the array size and reduces the settling time, due to the lower time constant for charging/discharging the capacitors. However, a smaller C_u results in larger random mismatch and linearity issues.

In the literature, C_u is often chosen empirically. A systematic approach for determining the minimum C_u is attempted in [1], but the models are built on older bulk technology nodes and ignore the impact of wire parasitics and random variations; in FinFET nodes in particular, these effects can be significant. Moreover, they disregard the impact on critical DAC linearity metrics. In [2], the impact of some components of parasitic capacitance on gain error and thermal noise are studied, but the work does not explore a method for finding C_u.

We present a systematic approach for finding the optimal unit capacitance, C_u, that considers systematic and random variations, wire parasitics, flicker noise, thermal noise, and circuit-level performance metrics including linearity.

II. Finding the optimal value of C_u

For a binary-weighted DAC in Fig. 1(a), the k^{th} capacitor $C_k = n_k C_u$, where $n_0 = 1$ and $n_k = 2^{k-1}, k \geq 1$. To reduce systematic mismatch, the capacitors in the circuit are divided into identical unit capacitor cells placed in a gridded matrix. Routing parasitics in the capacitor array result in nonideal DAC behavior. Fig. 1(b) shows the parasitics for capacitor C_i:

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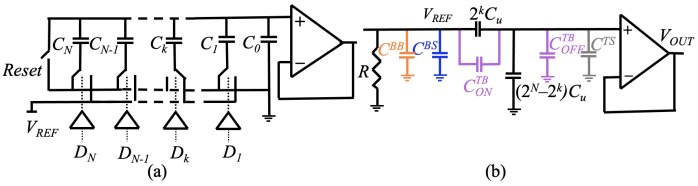

Fig. 1: (a) Schematic circuit of a charge-scaling binary DAC, (b) Equivalent circuit with the k^{th} bit set to 1; all other bits at 0.

(1) top-plate to ground parasitic capacitance, C_i^{TS}, (2) top-plate-to-bottom-plate parasitic capacitance, C_i^{TB}, and (3) the bottom plate capacitance C_i^{BS} to ground. If the bottom plate is switched to V_{DD} [ground], the top-plate-to-bottom-plate parasitic capacitance C_i^{TB} accumulates to C_{ON}^{TB} [C_{OFF}^{TB}].

Impact of C_u on thermal noise. The on-resistance of the charging transistors in the capacitor array introduces thermal noise that affects the DAC output voltage. The equivalent circuit for thermal noise calculation due to the capacitances in the array is shown in Fig. 2, where V_r^2 denotes the thermal noise produced by the switching transistor and r is the on-resistance of the switching transistor. To find the minimum unit C_u, [3] used $V_r^2 = KT/C$, where K is Boltzmann's constant and T is the absolute temperature. However, the thermal noise of the capacitor array is different from a single capacitor since there are N independent thermal noise sources produced by the on-resistances of N switching transistors (Fig. 1(a)) [1].

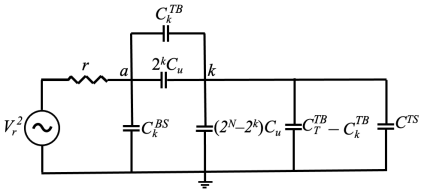

Fig. 2: Equivalent circuit of the capacitor array for thermal noise.

The equivalent circuit for thermal noise consists of the resistance of an individual switching transistor of the k^{th} charging branch, assuming other transistors as ideal switches as in [1]. Let C_T^{TB} be the total top plate to bottom plate parasitic capacitance and C_k^{TB} and C_k^{BS} be the parasitic capacitances for the k^{th} capacitor, denoting the equivalent capacitance of the parallel capacitances at node k in Fig. 2 as C_{eq},

$$C_{eq} = (2^N - 2^k)C_u + (C_T^{TB} - C_k^{TB}) + C^{TS} \qquad (1)$$

The total thermal noise for the binary-weighted capacitor array can be estimated as the RMS value of V_k (the noise contribution

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at node k) from each of the N switches, i.e.,

$$V_T = \sqrt{\sum_{k=0}^{N-1} \frac{2^k C_u + C_k^{TB}}{C_{eq}}} \sqrt{\frac{KT}{2^N C_u + C_T^{TB} + C^{TS}}} \quad (2)$$

Impact of C_u on flicker noise. Flicker noise, also known as $1/f$ noise, is an intrinsic noise source caused by charge carriers being trapped and later released as they move in the channel. Flicker noise is modeled as a voltage source in series with the transistor gate node, and within a bandwidth ranging from low f_L to high cutoff frequency f_H can be expressed as [4]:

$$V_n = \sqrt{k_n/(C_{ox} W L) \cdot \ln(f_H/f_L)} \quad (3)$$

The low cutoff frequency f_L in (3) can be chosen as 0.1Hz under practical considerations. To allow a steady-state voltage to be established early in the DAC cycle, f_H is chosen as $f_H = 10 f_{3dB}$, where f_{3dB} is the 3dB frequency metric, (the switching response of a capacitor array) is computed as in [5].

Optimizing C_u. The minimum value of C_u can be determined by adding up the contributions of the thermal noise (V_T), flicker noise (V_n), *differential nonlinearity (DNL) and integral nonlinearity (INL)* (evaluated by following the work of [5]) and the total error must be within $\pm(1/2)$ for an N-bit DAC, i.e.,

$$3\sigma_{V_T} + 3\sigma_{V_n} + \max\{INL, DNL\} \leq \frac{1}{2}\text{LSB} \quad (4)$$

We find C_u^{min} by enumerating C_u over a range to determine the smallest value that satisfies (4).

III. Results

We evaluate the proposed approaches on a commercial FinFET process, using the PDK to obtain per-unit wire models for resistance, capacitance to ground, and coupling capacitance. To model variability, we set the systematic variation parameters to $\gamma = 10$ppm, $\rho_u = 0.9$, $L_c = 1$mm [6], $A_f^2 = 0.85\% \times 1$fF [7] and $k_n = 10^{-25} V^2 F$. We use the values for C_{ox} and μ from a commercial FinFET process. For the switching transistors, we use the width W_t and length L_t corresponding to the pitch of one poly and eight fins in the commercial FinFET process.

To evaluate our approach, we use the spiral common-centroid placement approach from [5] proposed for FinFET technology (with high via resistances), but the scheme could also be used on other placements for the capacitive array. The results for the chessboard scheme are similar, since both schemes have similar top-place capacitances for the same number of DAC bits.

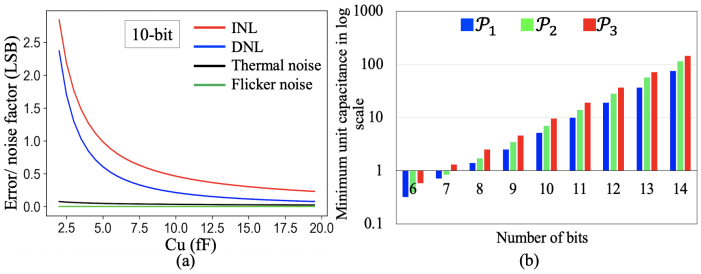

Fig. 3: (a) Error and noise components, as a function of C_u, in a 10-bit DAC, (b) Minimum unit capacitance, C_u^{min}, for $\mathcal{P}_1$ (nominal values of C^{TB}, C^{TS}), $\mathcal{P}_2$ (C^{TS} is doubled), and $\mathcal{P}_3$ (C^{TB} is doubled).

Noise and error components. Fig. 3(a) shows various components of error and noise as a function of C_u. For various values of C_u, we show the INL, DNL, flicker noise, and thermal noise at room temperature for the 10-bit DAC. The effects of thermal noise and flicker noise are seen to be negligible compared to INL/DNL. The specific results will vary with choice of placement and routing methods, which will result in different routing induced parasitics and different levels of mismatch.

Evaluating C_u^{min}. We use the above models to find the minimum unit capacitance value, C_u^{min}, required to meet noise and linearity thresholds, based on the criteria in (4), where the threshold for the sum of all errors is set to 0.5 LSB.

We consider multiple routing scenarios for the parasitics. In FinFET technologies, where wire resistance is a limiting factor, it is common to use wider wires (implemented as multiple parallel wires in lower metal layers due to coloring rules, which require wire widths to be constant) to reduce resistance. This also increases the wire parasitic capacitance, e.g., if the wire width is doubled, the capacitive parasitics are approximately doubled. For each value of the number of bits N, we consider three sets of parasitics for C^{TB} and C^{TS}:

(1) $\mathcal{P}_1$ uses the nominal parasitics, C^{TB} and C^{TS}, from the spiral layout for a single wire connection, as in [5].

(2) $\mathcal{P}_2$ uses the same value of C^{TB}, but doubles C^{TS}, for a different routing scheme with worse parasitics.

(3) $\mathcal{P}_3$ doubles the value of C^{TB}, and uses the nominal C^{TS}.

Fig. 3(b) shows C_u^{min} for these three cases. As the number of bits in the DAC increases, a larger C_u^{min} is required to overcome all the external and internal noise in each case.

We compare the C_u^{min} for the nominal case against cases $\mathcal{P}_2$ and $\mathcal{P}_3$. In both cases, as the parasitic capacitance is increased, the value of C_u^{min}, that satisfies (4), also increases: doubling C^{TB} almost doubles C_u^{min} as compared to the nominal case, and the effect is a little less significant when C^{TS} is doubled.

IV. Conclusion

Our method above determines the minimum unit capacitance, C_u^{min} in a capacitive binary-weighted DAC under mismatch and noise. This value of C_u^{min} minimizes the layout area and power consumption while meeting performance metrics.

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