ADEE-LID: Automated Design of Energy-Efficient Hardware Accelerators for Levodopa-Induced Dyskinesia Classifiers

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***Abstract*—Levodopa, a drug used to treat symptoms of Parkinson's disease, is connected to side effects known as Levodopa-induced dyskinesia (LID). LID is difficult to classify during a physician's visit. A wearable device allowing long-term and continuous classification would significantly help with dosage adjustments. This paper deals with an automated design of energy-efficient hardware accelerators for such LID classifiers. The proposed accelerator consists of a feature extractor and a classifier co-designed using genetic programming. Improvements are achieved by introducing a variable bit width for arithmetic operators, eliminating redundant registers, and using precise energy consumption estimation for Pareto front creation. Evolved solutions reduce energy consumption while maintaining classification accuracy comparable to the state of the art.**

***Index Terms*—levodopa-induced dyskinesia, energy efficiency, hardware accelerator, genetic programming.**

I. Introduction

Parkinson's disease (PD) is one of the most common neurological conditions. Patient care primarily suppresses symptoms using a *levodopa* drug, which can result in *levodopa-induced dyskinesia* (LID). A wearable device allowing long-term continuous LID classification would be a great source of information and help physicians adjust the dosage to suppress PD symptoms and, at the same time, reduce LID.

The usual goal of studies covering the design of the LID classifier is achieving the highest accuracy while deploying computationally expensive methods [1], [2]. Data transfer to an external device using such an expensive method is inconvenient and involves transferring vulnerable health data. Lones et al. [1] proposed a LID-classifier model utilising a sliding window of 32 samples of low-level movement features and designed it using *genetic programming* (GP). Hurta et al. [3] proposed a model of the LID classifier and used GP for the automatic design of an energy-efficient feature extractor (FE). The FE and classifier design is a complex problem that was solved using a co-design approach. Their model also reduced data representation to an 8-bit integer.

The state-of-the-art solution [3] does not consider the sub-byte operations successfully used in machine learning accelerators [4], [5]. Moreover, as evolved classifiers do not often utilize all sliding window samples, eliminating unnecessary circuits could reduce energy consumption. Lastly, the hardware complexity of evolved circuits was estimated using the number of arithmetic operations in [3], while adopting a standard synthesis procedure would provide more precise results.

II. Proposed Methodology

The proposed approach for the automated design of an energy-efficient LID classifier is shown in Fig. 1. FE and classifier are evolved using *Cartesian GP* (CGP) [6]. CGP is an iterative optimization algorithm with integer netlist representation trying to maximize the design quality. The FE and classifier have their bit widths (3 to 12 bits considered) included in their netlists. They are designed simultaneously by switching the currently-evolved *population* in each epoch. Populations interact through the evaluation phase, where *candidate solutions* of one population (e.g., the classifiers) are evaluated in connection with the currently best candidate solution from the other population (i.e., the FE). The best candidate solution from the current population is used as the parent of the next generation of candidate solutions. The fitness of candidate solutions is given as the classifier accuracy (AUC) of the composition of the FE and classifier. We also implement the coevolution of *Adaptive Size Fitness Predictors* [3] that accelerated the evolution process further. The final combination of FE and classifier is evaluated on separate test data.

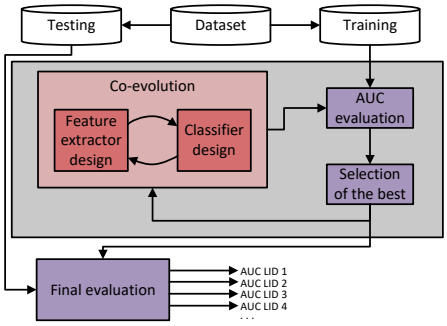

Fig. 1. Overview of the proposed methodology for the evolutionary design of energy-efficient LID classifiers.

LID classifier comprises two central units being evolved, i.e. the FE and classifier, and the rest of the model needed for their interaction. First, the FE is applied separately to each data source. Individual features are then aggregated to form an approximate mean, using the bit shift to the right by two and subsequent additions. Features are extracted every 0.01 s, and stored in up to 32 registers representing the sliding window used by the classifier. The exact number of registers is given by the oldest sample used by the classifier. The whole LID

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classifier generates $L-31$ responses for recording L samples. The generated response contains information about the detected level of dyskinesia. Due to the possibility of different bit widths of input data, FE, and classifier, logical shifts to the right are used to achieve the required widths.

III. Results

The CGP evolves both populations in the same way as presented in [3], with a limit of 10,000 generations. As CGP is a stochastic method, 1,100 independent runs were performed to allow precise evaluation of the method. Data used for training and evaluation (i.e. four LIDs, Sitting, and Walking data sets) came from two separate clinical studies; they were used in the same way as in [1]. The synthesis using Synopsys Design Compiler targeting 45 nm ASIC technology on 100 MHz frequency was used to estimate the energy consumption.

Fig. 2 shows that introducing the variable bit width does not prevent in achieving the maximum AUC. Further, the Mann-Whitney U-test confirmed a non-significant difference, for $\alpha = 0.05$, between the proposed and former method for all test groups (except LID1 and Sitting, where an improvement is observed). The variable bit width requires deciding on the initial value of either eight bits, as in the current state-of-the-art solution, or a random value. Results show that the random initialisation leads to higher AUC in all test groups except LID1, where a significant difference in favour of the 8-bit initial setting was registered. A significant difference in favour of random initialisation was then registered in test groups LID3 and Sitting. The variable bit width setting, encoded as part of the chromosome, with a random initial value is thus fully capable of producing results of comparable quality to the previous solutions.

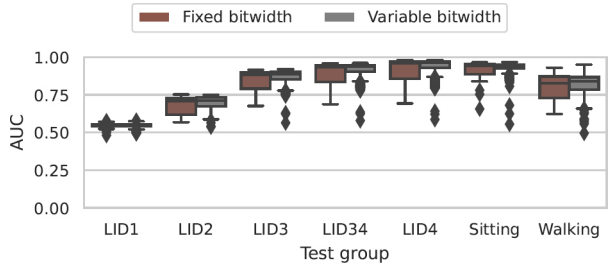

Fig. 2. The AUC score obtained from 1100 CGP runs for various bit width settings and data sets.

A. Resulting Classifiers

A Pareto front based on the accuracy (in terms of AUC) and energy consumption obtained by the synthesis of evolved solutions was created to allow the selection of the best LID classifiers possible. The parameters of selected Pareto optimal solutions are in Tab. I. Comparison with the results of Lones et al. [1] and Hurta et al. [3] reveals that the proposed method provides comparable or higher AUC across all test groups except for test group LID1.

In the case of Lones et al. [1], energy consumption is not reported. Nevertheless, their energy consumption is assumed to be orders of magnitude higher due to the floating point data representation, computationally expensive magnitude calculation and a set of building blocks containing expensive functions such as multiplication. A comparison with the results of Hurta et al. [3] (reimplemented in our fabrication technology) shows a decrease in energy consumption, justifying thus the need to employ proper hardware characteristics during the evolution.

TABLE I
Energy and AUC for various test groups of selected Pareto-optimal solutions

Methodology	FE/Clas. bitwidths	Window size	Energy [pJ]	AUC LID1	LID2	LID3	LID34	LID4	Sitting	Walking
This	9/11	28	0.228	0.553	0.737	**0.921**	**0.962**	**0.983**	**0.968**	0.906
This	9/8	24	0.226	0.557	0.740	0.916	0.958	0.979	0.959	0.901
This	8/11	26	0.218	0.550	0.739	0.913	0.956	0.978	0.957	0.905
This	9/12	26	0.192	0.552	0.741	0.916	0.956	0.975	0.959	0.912
This	9/12	22	0.167	0.555	**0.746**	0.912	0.955	0.976	0.957	**0.914**
This	10/9	31	0.146	0.552	**0.747**	0.916	0.953	0.971	0.957	0.868
This	6/7	32	0.093	0.527	0.708	0.889	0.946	0.974	0.951	**0.914**
Lones [1]	floats	—	—	**0.56**	0.69	0.85	—	0.93	0.92	0.73
Hurta [3]	8/8	32	0.859	0.55	0.73	0.89	—	0.96	0.95	0.82
Hurta [3]	8/8	32	0.465	**0.56**	0.73	0.89	—	0.97	0.95	0.87
Hurta [3]	8/8	32	0.513	0.55	0.73	0.90	—	0.97	0.95	0.83

IV. Conclusions

In this paper, we proposed a method for the automated design of energy-efficient hardware accelerators for LID classifiers. Several improvements over the state-of-the-art method were proposed and experimentally evaluated. These improvements include using reduced bit widths during the automated co-design process, optimized circuits, and estimated energy consumption when creating the Pareto front.

Solutions designed by the proposed method achieved an increase of AUC across most test groups while having significantly lower energy consumption than solutions presented in the literature.

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