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High Performance and DNU-Recovery Spintronic Retention Latch for Hybrid MTJ/CMOS Technology

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***Abstract*—With the advancement of CMOS technologies, circuits have become more vulnerable to soft errors, such as single-node-upsets (SNUs) and double-node-upsets (DNUs). To effectively provide nonvolatility as well as tolerance against DNUs caused by radiation, this paper proposes a nonvolatile and DNU resilient latch that mainly comprises two magnetic tunnel junction (MTJ), two inverters and eight C-elements. Since two MTJs are used and all internal nodes are interlocked, the latch can provide nonvolatility and recovery from all possible DNUs. Simulation results demonstrate the nonvolatility, DNU recovery and high performance of the proposed latch.**

***Index Terms*—Radiation hardening, latch reliability, soft error, recovery, nonvolatility**

I. Introduction

As the dimensions of CMOS transistors scale down, the critical charge and threshold voltage of CMOS transistors are sharply reduced. Radiation effects have become a severe reliability challenge for nano-scale CMOS circuits [1]. CMOS integrated circuits are becoming more and more vulnerable to soft errors. Instead, magnetic tunnel junction (MTJ) is intrinsically immune to radiation effects, and it is considered as a promising candidate for building next-generation nonvolatile memory due to its nonvolatility, high speed and compatibility with CMOS circuits [2-4]. However, the CMOS peripheral circuits remain vulnerable to particle strikes [5]. Moreover, in advanced nano-scale CMOS technologies, the impact of a particle striking can lead to the state changes of two nodes in a cell, which is called a DNU [6]. Therefore, the reliability of hybrid MTJ/CMOS circuits is a critical problem.

In this paper, we propose a high-performance (low-delay) and DNU-recoverable spintronic retention latch. The nonvolatility achieved by MTJ guarantees zero standby power without losing data when the circuit is in the Power-OFF state.

II. Proposed Solution and Simulation Results

Figure 1 shows the schematic of the proposed radiation hardened nonvolatile latch. It can be seen that the latch comprises two parts, namely DNU Recoverable Latch Part and Nonvolatile Shadow Part. When CLK = 1 and NCK = 0, the transmission gates are ON. Therefore, nodes N1, N2, N7 and Q are driven by D through the transmission gates. N3, N4, N5, N6, N8 and N9 can obtain values by inverters or C-elements (CEs). Meanwhile, the current flowing through the MTJs changes the relative direction of magnetization of the free layer and the fixed layer. Then, the values can be stored in the two MTJs. When CLK = 0 and NCK = 1, the transistors in transmission gates connected to D are OFF. Simultaneously, the clock-controlled transistors in the clock-gating (CG)-based CEs are ON. As a consequence, nodes N1, N2, N7 and Q are driven by the CEs and the CG-based CEs, respectively. At this moment, all interlocked feedback loops in the latch can be formed to retain values reliably.

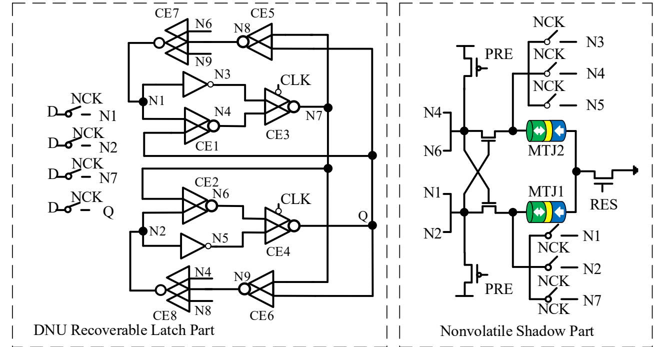

Fig. 1. Proposed radiation hardened nonvolatile latch.

When the power supply is reconnected, the circuit starts to restore values. When PRE = 0, N1, N2, N4, and N6 can be charged to VDD. At this time, the circuit does not form any feedback loop, so that the above four nodes cannot be affected by other nodes. When RES = 1, the fixed layer of MTJ1 and MTJ2 connects to the ground. The nodes connected to the MTJ with the P state are discharged faster than the nodes connected to the MTJ with the AP state because the AP state has a higher resistance than the P state. As a result, with the different states of the two MTJs, <N1, N2> and <N4, N6> have different logic states. Therefore, the other nodes successively obtain their correct values.

Let us discuss the DNU self-recovery of the latch. Due to the symmetric structure of the latch, we only need to consider four possible cases, i.e., Case 1 to Case 4 in the following.

Case 1: A DNU impacts two nodes, which are both the input of an inverter and one input of a CE.

Case 2: A DNU impacts two nodes, one node being both the input of an inverter and one input of a CE and another node being the only input of CEs. There are two types. The first type is that the two nodes are both the inputs of a CE, e.g., CE1. The second type is that the two nodes are the inputs of different CEs, e.g., CE1 and CE3.

Case 3: A DNU impacts two nodes that are only the inputs of CEs (one node is one input of a CE and another node is one input of another CE).

Case 4: A DNU impacts two nodes that are the inputs of a CE except the node-pairs in Cases 1 through 3.

The DNU resilience of the proposed radiation hardened nonvolatile latch was demonstrated by simulations. The simulations were performed by using an advanced 45 nm CMOS technology with the Synopsys HSPICE tool. The spin transfer torque magnetic tunnel junction (STT-MTJ) model proposed in [7] was used. The simulation results for the key DNU injections of cases 1-4 are shown in Fig. 2. It can be seen that, two SNUs with sufficient charge were injected to

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the above-mentioned node pairs to simulate DNUs, respectively. It is clear that the influenced node-pairs can rapidly recover from DNUs.

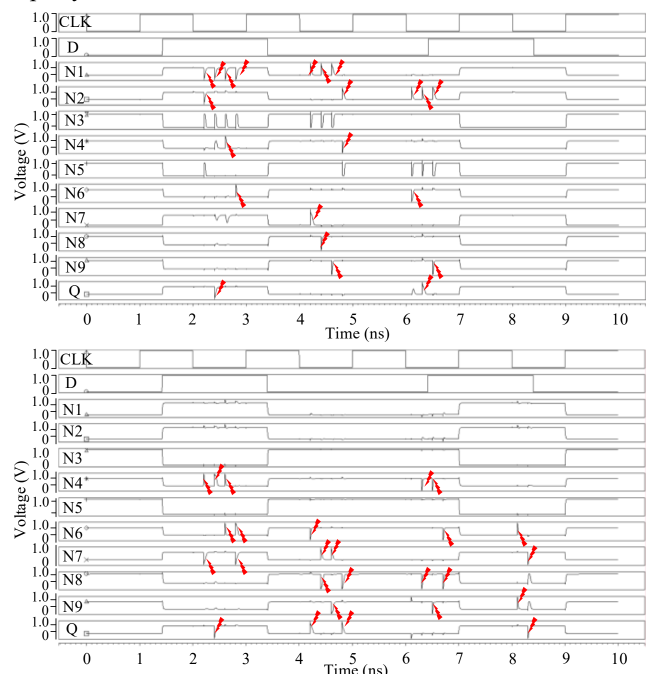

Fig. 2. Simulation results for key DNU injections of the proposed latch.

Note that, in all the above simulations, we used a double exponential current source model to simulate all the DNU injections [8]. The worst-case injected charge was up to 45fC. The time constants of the rise and fall of the current pulse were set to 0.1 ps and 3.0 ps, respectively. In summary, the above-mentioned simulation results demonstrate the self-recovery from DNUs of the proposed latch.

III. Comparison and Evaluation

In this section, the proposed latch is compared with the previous STT-MTJ based radiation hardened nonvolatile latch designs to further assess its reliability and overhead. For a fair comparison, the reviewed latches were also designed using the same conditions, i.e., the same working temperature, the same supply voltage, and the same CMOS technology.

TABLE I
Reliability Comparison among the Radiation Hardened Nonvolatile Latch Designs

Latch	SNU Tolerance	DNU Tolerance	DNU Resilience	Backup Ability	Restore Ability
Design in [1]	√	×	×	√	√
Design in [2]	√	×	×	√	√
Design in [3]	√	×	×	√	√
Design in [4]	√	×	×	√	√
Design in [5]	√	×	×	×	√
Design in [6]	√	√	×	×	√
Proposed	√	√	√	√	√

***Note that, there is no existing STT-based nonvolatile latch that can provide DNU resilience and nonvolatile function simultaneously.**

The reliability comparisons among the radiation hardened nonvolatile latch designs are shown in Table I. We can see that none of the previous latches can provide DNU self-recovery, and some latches cannot provide backup capability. Regarding our proposed nonvolatile latch, it can provide backup ability and restore ability. Moreover, it can recover from DNUs. In summary, the proposed latch can provide better fault tolerance.

TABLE II
Overhead Comparison among the Radiation Hardened Nonvolatile Latch Designs

Latch	D-Q Delay (ps)	10^{-4}×CMOS Area (nm^2)	MTJ Counts	Power (μW)
Design in [1]	54.37	10.13	2	19.26
Design in [2]	37.56	9.52	2	12.50
Design in [3]	6.72	4.34	2	11.84
Design in [4]	43.78	8.30	2	12.37
Design in [5]	51.84	6.89	4	16.13
Design in [6]	98.53	15.39	2	18.34
Proposed	3.71	16.87	2	20.46

***Note that, the first-ever DNU resilience with nonvolatile function for the proposed latch is at the cost of indispensable CMOS area and power.**

Table II shows the overhead comparison among the radiation hardened nonvolatile latch designs. It can be seen that the proposed latch has the smallest D to Q transmission delay. In order to provide complete self-recovery from DNUs to obtain better fault tolerance for the proposed latch, slightly more elements are used in the latch in comparison with the other latches. Hence, the proposed latch has larger area and higher power consumption. It can be seen that the area and power consumption of the proposed latch are close to the DNU tolerant latch proposed in [6]. However, the proposed latch has better fault tolerance and smaller delay.

IV. Conclusions and Further Work

In this paper, we have proposed a high performance and DNU recovery nonvolatile latch. Compared to existing latches, the proposed latch provides better fault tolerance and has the smallest delay. Simulation results have demonstrated the DNU recovery and low delay of the proposed latch so that the latch can be applied to aerospace applications that require radiation hardening with high performance. In our further work, we will consider the single event transient issue as in [9].

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