Smart Hammering: A practical method of pinhole detection in MRAM memories

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Abstract— **As we move toward the commercialization of Spin-Transfer Torque Magnetic Random Access Memories (STT-MRAM), cost-effective testing and in-field reliability have become more prominent. Among STT-MRAM manufacturing defects, pinholes are one of the important ones. Pinholes are defects on the surface of the oxide layer which degrade the resistive values and, in some cases, cause an oxide breakdown. Some moderate levels of pinhole defects can remain undetected during standard functional tests and may cause a field failure. A stress test of the whole memory, including multiple cycles of long writes, has been suggested to detect candidate pinhole defects. However, this test not only causes extra costs but also degrades the reliability of MRAM for the entire array. In this paper, we have statistically studied the behavior of pinholes and proposed a cost-effective testing scheme to capture pinhole defects and increase the reliability of the end product. Our method limits the number of test candidate cells that need to be hammered, providing a reduced test time of up to 96.42% for our case studies compared to existing methods. This is while the advantages of standard tests are all preserved with our method. The proposed approach is compatible with memory-built-in self-test (MBIST) schemes.**

I. INTRODUCTION

Many integrated chip manufacturers announced *Spin-Transfer Torque Magnetic Random Access Memories* (STT-MRAM) production as a good candidate to replace embedded flash and eDRAM [1]–[3]. Despite all the attractive features of STT-MRAM, its full commercialization requires further steps to guarantee sufficient product quality [4], [5]. An important step towards this goal would be providing practical guidelines to ensure the lifetime functionality of the memory chips and avoid test escapes [6]. This issue has become more serious since recent studies have shown that there is a possibility of manufacturing defects that may not be easily detectable by simple testing schemes based on March C- [7].

Magnetic Tunnel Junction (MTJ), the core element of STT-MRAM, is manufactured during the back-end-of-line manufacturing phase. During this process, pinholes can be formed in the MgO layer of MTJs due to the diffusion of conducting materials (e.g., CoFeB) into the oxide layer [4]–[6]. The impact of these defects could be different based on their pinhole size. In severe cases (pinholes area > 0.62% of MTJ area), faulty cells can be easily detected by standard tests [4], [5]. On the contrary, in marginal cases (areas of pinholes < 0.62% area of MTJ), their influence on the performance may not be significant enough and remain undetected by existing test schemes [4], [5]. These pinholes can grow in size during their life cycle and cause early-life failure in the memory. Increasing the *error correction code* (ECC) to cover these extra potential faults would be too costly, and ignoring them could cause field failures and leakage problems. Therefore, a practical method of evaluating potential pinhole defects considering the ECC budget is quite of interest.

Recent research has tried to model these defects based on physical characteristics rather than electrical shorts/opens. They have shown that modeling pinholes based on resistive defects may not be accurate enough to capture all aspects of pinhole defects [4], [5]. In addition to modeling the pinholes, it is necessary to devise proper testing schemes with high coverage and low test time and costs. In [5], it is suggested to use the hammering method to further aggravate the effect of the present pinholes, making them more detectable during testing. The hammering method comprises multiple cycles of long back-to-back write pulses, ideally with higher voltages. Despite its effectiveness, the testing-time overhead of hammering every individual cell is too much to be practical for production tests.

This paper proposes a *Memory Built-in Self-Test* (MBIST) compatible, low-cost testing scheme for pinhole detection. It provides a guideline considering multiple factors, including process controllability, ECC budget, and defect coverage. The contributions of this paper are as follows.

- We have statistically studied the pinhole defects, their influence on the characteristics of MTJ, and how they change their resistive distributions.

- We have provided a recommended spec to set a target defect coverage based on process maturity and product configuration. If the expected pinhole defect level is higher, which could cause an unrepairable row by existing ECC, the hammer test is needed to guarantee the product's functionality.

- To reduce the test burden, we limit the number of cells required to perform hammer tests to guarantee target pinhole defect coverage. A number of test candidates were selected based on bit performance and variation. We calculate the expected performance level to mark enough pinhole defect population to meet the target defect coverage for correct chip functioning. The test candidate cells in the chip are selected among low-performing cells during the read test with modified reference resistance values.

The rest of this paper is organized as follows. Section II provides background on STT-MRAM structure and pinhole defects. Section III explains how we modeled pinholes based on literature and offers a guideline for calculating different test requirements. Section IV presents the simulation setups, results, and related discussion. We conclude the paper in section V.

II. BACKGROUND

A. Magnetic Tunnel Junction

The MTJ is the core element of STT-MRAM memories. An MTJ comprises two magnetic layers separated by a thin oxide layer. One of the layers has a configurable magnetic orientation, while the other has a fixed one.

The resistance of MTJ could be modulated depending on the orientation of its magnetic layers. If the layers have the parallel spin direction (R_P), then the resistance of the MTJ will be lower compared to the case in which the layers are in the opposite orientation (R_{AP}) [8]. The ratio between these two values is referred to as *tunnel magnetoresistance* (TMR) and is calculated by (1) [8], [9].

$$TMR = \frac{R_{AP} - R_P}{R_P} \tag{1}$$

Higher TMR provides better readability and read-stability [10]. Reading the value stored in MTJ can be done by comparing the current passing through it to a reference current generated by the reference source [11]. For reconfiguring an MTJ, we can pass a current higher than the critical current through the MTJ, and based on the current direction, the MTJ can be configured to two states. If the current is passed through the fixed layer toward the free layer, the MTJ is changed to the P state. On the contrary, if the current is passed from the free to the fixed layer, the configuration will be set to AP.

B. Memory architecture and trim circuitry

Fig. 1 shows the structure of an STT-MRAM memory consisting of an MTJ array, read circuitry, address decoder, and write circuitry. The read circuit consists of a sense amplifier and a trimming circuit to set the reference resistance. The reference resistance value will be fine-tuned to the corresponding trim level by a configurable digital input setting [12], [13]. The trim circuitry can be composed of a series of resistors that can be individually bypassed. This provides tunability for reference resistance that is used to improve the read margin, increase the yield, and mitigate the process and temperature variation effects [14], [15].

The trimming process, which is performed at the initialization phase, can be completed through different approaches. A naive solution would be performing a functional test and collecting fail-bit information for every trim step. However, more efficient ways of searching for optimum trim settings using existing MBIST circuitry were proposed in the literature. In [15], the authors suggested an MBIST-based automated trim search method that minimizes the test time by utilizing a binary search approach. This method computes the optimized read reference trim value within the chip through a built-in analysis circuit rather than manual test and extraction for engineering analysis.

C. Pinhole defects and Hammering method

Manufacturing MTJ in the back-end-of-line phase is a process that requires the deposition of more than ten layers for performance purposes [16]. Unique defects can be introduced during this process that could cause MRAM operation failure [4]. One of the important MTJ failure mechanisms is the pinhole defect shown in Fig. 2.a. This defect can be caused by the diffusion of Boron or other metallic impurities into the MgO layer during the deposition process [17], [18]. Other potential causes are the filling of pinholes in the MgO layer with CoFeB material and the diffusion of Oxygen atoms out of the MgO layer due to over-annealing [19], [20].

The pinholes in the MgO layer form a leakage path between two ferromagnetic layers and reduce the TMR value [17]. In some cases, the presence of pinholes could cause a field breakdown in the MgO layer due to the joule heating generated by the leakage current passing through the MTJ [5].
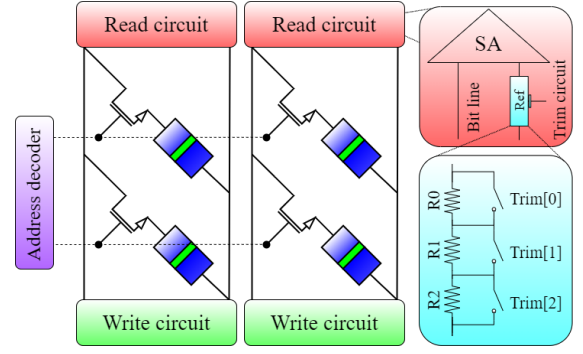

Fig. 1. Structure of a standard STT-MRAM along with trim circuitry.

Many attempts have been made to model the pinhole effects [4], [5], [21], [22]. Initial efforts were made to model pinholes using electrical shorts and opens [21], [22]. However, Wu et al. demonstrated that using resistive-based defects is too pessimistic to precisely model the physical behavior of pinholes [4], [5]. Instead, they have suggested a model based on the *resistance-area product* (RA) and TMR degradation, as shown in equations (2) and (3), respectively. In these equations $A_{ph} = [0,1]$ is the normalized pinhole area with respect to cross-section area of MTJ denoted by A. RA_{gc} and TMR_{gc} are respectively RA and TMR of a good MTJ (meaning that $A_{ph} = 0$). RA_{fc} is the RA of faulty device which can be obtained by extrapolating the date of RA degradation for a device under stress test [5].

$$RA_{eff\_ph}(A_{ph}) = \frac{A}{\frac{A(1-A_{ph})}{RA_{gc}} + \frac{A.A_{ph}}{RA_{fc}}} \tag{2}$$

$$TMR_{eff\_ph}(A_{ph}) = TMR_{gc}.\frac{RA_{eff\_ph}(A_{ph}) - RA_{fc}}{RA_{gc} - RA_{fc}} \tag{3}$$

Based on the relative area of pinholes, we could classify them into three different categories, as shown in Fig. 2. The first category is the cells with a relative pinhole area below 0.0015. There is no data showing the failure of these cells within their expected lifetime [4]–[6]. For devices with a relative pinhole area between 0.0015 and 0.0062, the pinhole defect will cause a TMR degradation. However, the behavior of devices is still in the range of normal operation at the manufacturing test time. We call these devices marginal since their pinholes could potentially grow in size and cause a complete oxide breakdown earlier than good cells [6]. At last, if the pinhole defect area is larger than 0.0062, the effective resistance of the cell is below the reference resistance value, and the cell will fail during the standard March test.

Detecting potential breakdowns is not only essential to guarantee the functionality of the chips but also important for maintaining their power consumption level during their lifetime. Faulty MTJs act as electrical shorts, and therefore a high current passes through them when activated. Therefore, if not detected and treated in the test stage, they may cause leakage issues even if the ECC budget covers them.

A testing algorithm that could be used to trigger marginal cells to fail is a repeated back-to-back write operation known as a hammer test [5], [6]. In this test, the accessed MTJ will be continuously stressed to cause joule heating and voltage stress. It has been shown that the marginal cells that are not detectable during routine March tests could become detectable as their pinhole size grows during the hammering test [4]–[6].

Using high voltage or extended write cycles makes MTJs reach temperature saturation faster and accelerates the exposure of marginal cells during the functional test. However, such conditions are difficult to apply in production tests [23].

III. PROPOSED APPROACH

A. Modeling

First, a model of pinhole defects is needed to investigate their behavior and provide a testing scheme to detect them. For this purpose, we have used the MTJ model of [9] as our framework and embedded formulas (2) and (3) in order to capture the RA and TMR degradation effects. In addition, we have utilized equations (4) and (5) to capture the voltage effects on resistance and TMR drops as a function of voltage [5]. In these formulas R_0 and TMR_0 are respectively the R_P and TMR values at voltage zero. V_h is the voltage which the TMR drops to half of TMR_0 value. And δ and ρ are fitting parameters.

$$R_P(V) = \frac{R_0}{1+\delta.|V|} \quad (4) \qquad TMR(V) = \frac{TMR_0}{1+\frac{V^2}{V_h^2}+\rho.V^{\frac{4}{3}}} \quad (5)$$

Our model is calibrated and verified according to the experimental measurements presented in [4]–[6]. Fig. 3 shows the simulation results for R-V hysteresis loops of a good MTJ, two marginal (blue and cyan), and three faulty ones (purple, orange, and red). As expected, the loops for marginal and faulty devices are smaller compared to the good ones indicating lower R_P, TMR, and switching voltage (V_c). The decreased switching voltage is associated with lower resistance values which increase the amount of current passing through the MTJ for a specific voltage. It is notable that in case the hysteresis loop of an MTJ shrinks to make Rap below a reference level, it will be indistinguishable between the resistive states R_P and R_{AP}, leading to a stuck-at fault.

B. Resistance distribution in MRAM

In Fig. 4, we show a distribution of resistance values for two types of MTJ cells. The green lines show the distribution of good cells, and the red lines show how the green distribution would shift if all green cells had a pinhole with a relative area of 0.0015. The solid lines represent the R_{AP} states, and the dashed lines stand for R_P state. The different adjustable references by the trim circuit are also shown on the x-axis. The reference resistance setting below Trim_a (2.7kΩ) will increase Read '0' fails, while the reference resistance setting above Trim_b (4.7kΩ) will increase Read '1' fails. Considering the distributions, we can conclude that the optimal trim step for this example array would be trim_c at 3.7kΩ, where it provides the balanced read margin for data '0' and '1'.
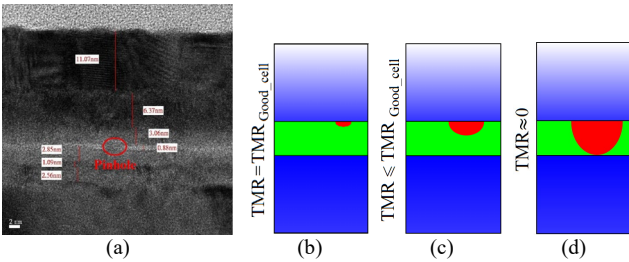

Fig. 2. Structure of pinhole defect. a) TEM image of a pinhole in the MgO layer (Source: [17]). b) good MTJ cell. c) marginal MTJ cell. d) faulty MTJ cell.
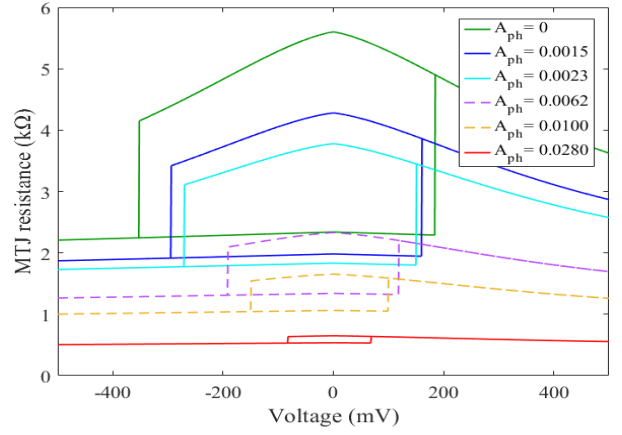

Fig. 3. R-V hysteresis loop of a good MTJ (green), two marginal (blue and cyan), and three faulty ones (purple, orange, and red). The solid lines show the results calibrated according to experimental measurements of [4]–[6]. The dashed lines show additional results predicted by our model.
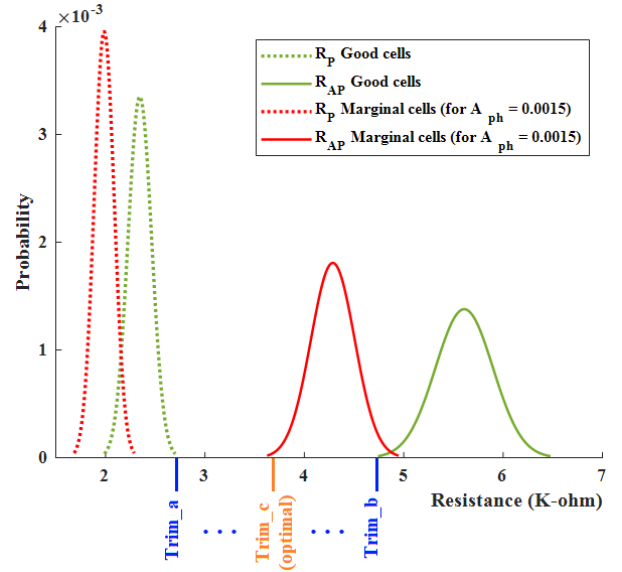

Fig. 4. Resistance distribution for good and marginal ($A_{ph} = 0.0015$) cells.

C. The proposed methodology of smart hammering

As shown in the previous section, the presence of pinholes in marginal cells degrades their resistance. However, in some cases, even the decreased resistance falls within the range of good cells and, therefore, cannot be detected by standard tests. The test escape pinhole defects can degrade further and cause early bit failures. In case these bit failures exceed the ECC budget of the memory, they will cause reliability issues. In addition, the leakage caused by their low resistance values can become an early performance degradation issue. However, a massive test on the entire array for pinholes is not a feasible solution since the memory sizes are too large to conduct such a thorough analysis in a cost-efficient manner. Therefore, our goal here is to calculate the limited test access number based on the target defect coverage so that we can achieve good coverage value under the limited test budget. Once we decide on the target defect coverage, we can calculate the required resistance range to limit the number of candidate cells for the hammer test. This test candidate cell selection can be made by reading out cell values with a modified trim step to capture cells with low resistance in the pool of all memory cells. Fig. 5 shows an overview of our proposed methodology.

As shown in Fig. 5, the hammer test for pinhole detection is not always required to guarantee field failure coverage, as it can be covered by ECC and other repair solutions (including pinholes and other hard errors). To calculate the required defect coverage, we need to consider multiple factors, namely, memory architecture, the probability of pinhole defects, baseline defect rate, and their coincidence on the same row to exceed the repair budget.

D. Calculating required pinhole defect coverage

We first calculate the *fail bit count* (FBC) to compute the required pinhole coverage ($R_{coverage}$), which guarantees fault-free functionality. We defined multiple memory parameters, including the number of bits per word (W_{lenght}), the number of words per chip ($Memory_{size}$), and the number of manufactured chips ($Product_{volume}$). It is assumed that pinhole failures of individual cells are independent and uncorrelated and identically distributed over the entire memory array. Assuming P_{pd} for pinhole defect probability, N_{pd} for pinhole defect count per word, P_{hr} for hard fail probability, which indicates entire functional fails, including write failures, read decision failures, read disturb faults, etc., and N_{hr} for the number of hard fail bits in a word. We can calculate FBC using equation (6). Consequently, the *expected number of occurrences* (ENO) for a different combination of defects (e.g., one pinhole and one hard fail, or two pinholes and no hard fail, etc.) could be calculated using (7).

$$FBC = \binom{W_{lenght}}{N_{pd}} \times P_{pd}^{(N_{pd})} \times \binom{W_{lenght} - N_{pd}}{N_{hr}} \times P_{hr}^{(N_{hr})} \times$$
$$\left(1 - P_{pd} - P_{hr}\right)^{(W_{lenght} - N_{pd} - N_{hr})} \tag{6}$$

$$ENO = FBC \times Memory_{size} \times Product_{volume} \tag{7}$$

This number shows how many words per manufacturing process will have N_{pd} number of pinhole defects and N_{hr} number of hard defect errors inside. In case $N_{pd} + N_{hr}$ exceeds the ECC budget, we will have a faulty chip in the field. Therefore, it is necessary to test such chips at the manufacturing time in order to prevent them from failing in the field. Assuming all hard errors need to be covered by ECC, we need to successfully detect a specific amount of pinhole defects so that the breakdown of the remaining ones does not cause any future chip failures in the field. To achieve this, the probability of undetected pinholes after the manufacturing test should be low enough that they could not cause a field failure. The required pinhole probability after the test (D_{pd}) can be calculated by replacing P_{pd} with D_{pd} in equation (6) and solving equation (7) for an ENO value lower than one. This solution needs to be solved for all possible combinations of faults in which $N_{pd} + N_{hr}$ exceeds the ECC budget. For instance, if we have a 2-bit ECC budget and one of the bits is reserved for other types of field failures, we need to solve the equation for ($N_{pd} = 1, N_{hr} = 1$) and ($N_{pd} = 2, N_{hr} = 0$). The case of ($N_{pd} = 0, N_{hr} = 2$) exceeds the repair budget but does not need to be considered, as we assumed all hard errors are detectable with a standard test [24]. It is noteworthy that we don't need to consider a higher number of faults (e.g., $N_{pd} = 2, N_{hr} = 1$) as they are a subset of the prementioned conditions ($N_{pd} = 1, N_{hr} = 1$). After calculating D_{pd} for all different cases, the required $R_{coverage}$ could be calculated by (8) where $D_{pd,max}$ is the maximum value of D_{pd} for all the cases.

$$R_{coverage} = \frac{P_{pd} - D_{pd,max}}{P_{pd}} \times 100 (\%) \tag{8}$$

After calculating the required pinhole defect coverage, one can use the hammering method to detect the marginal cells in a poll of suspect cells to achieve the desired defect coverage. By doing this, the initially undetectable pinholes will become large enough to be detected by the standard test procedure.

In order to determine which cells and what percentage of memory need to be hammered, we used a MATLAB code that calculates the achievable coverage ($A_{coverage}$) per trim step (see Fig. 6). In this code, the $A_{coverage}$ will be calculated for every trim step starting from the first trim step (Trim_a in Fig. 4). If the $A_{coverage}$ of a stage is equal to or higher than our target $R_{coverage}$, the code will return this step number as an output. The results provided by this code also determine which trim step needs to be used for the hammering procedure and what percentage of memory will go through hammering to achieve the target $R_{coverage}$.

After the target trim step is obtained, it can be used to perform the hammering test in the following manner. First, the trim setup is set to the target resistance level. Then all the MTJs are written to the AP state, and the entire memory is tested with this specific predetermined trim. In case a cell read fails with this trim step, the cell will be hammered for a specific number of long write pulses. The hammering method can be done in two directions. In [25], it is suggested that hammering in the AP to P direction could be more effective due to the self-heating effect, while it is argued in [26] that the hammering would be more effective in P to AP state due to higher voltage stress on MTJs. Notably, since the pinhole effect on resistance is more detectable in the AP state, we try to capture them in this configuration. After marching through the entire memory this way, we proceed with a standard test procedure to capture the previously marginal cells that have been broken down due to the Joule heating and voltage stress effects.
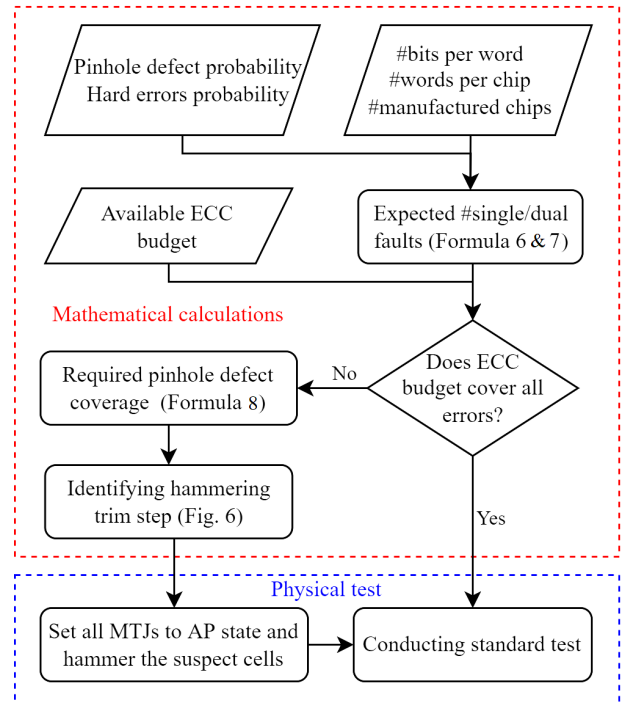

Fig. 5. Flowchart of our proposed method for pinhole detection.

```
input: Required pinhole defect coverage (TPDC)
output: Trim step number (TSN), Memory hammer percentage (MHP)
for each trim_step
    calculate PDC
    if PDC > TPDC
        TSN ← trim_step
        MHP ← calculate the memory hammer percentage
        break
    end
end
```

Fig. 6.   Pseudo code for determining the trim step needed for the hammering procedure.

It is notable that in some cases, the target PDC will not be achievable if the trim steps are limited. For these cases, we can either increase the trim step counts (e.g., from 32 to 64) or use a manufacturing process with higher variation control. Since the number of trim steps cannot be modified after manufacturing, designers need to consider the possible requirement of trim extension beforehand.

IV. SIMULATION RESULTS AND DISCUSSION

A. Simulation setup

To demonstrate the importance of pinhole detection, two study cases are considered, as shown in Table I. In all our simulations, we consider the room temperature and the MTJ characteristics presented in Table II [9]. The R_P and TMR variations are considered 6.95% and 4.1%, respectively [27]. The effective pinhole defectivity rate and hard error rate are assumed to be 0.2 ppm and 1 ppm [24]. We also assume that a relative pinhole area needs to be equal to or larger than 0.0015 in order to cause an early field failure since there is no data showing smaller pinholes could cause failures within the expected lifetime of the device [4]–[6]. We also consider a trim circuit ranging from $R_P + 3\sigma_P$ to $R_{AP} - 3\sigma_{AP}$ with 64 steps [12], [14].

B. Simulation results

Fig. 7 shows the simulation result of the MTJ distribution based on their pinhole size. We have considered the effective pinhole ratio of 0.2 ppm; therefore, the accumulative area below the cell distribution line needs to be equal to 0.2×10^{-6} for pinhole with a relative area larger than 0.0015. In this graph, the red area shows the probability density of the pinhole defects that standard test procedures can always detect, while the green area shows the probability density of the pinhole defects that are detectable by smart hammering test based on candidate cell selection with a trim circuitry [12], [14]. The blue area includes the entire population of pinhole defects where the overlap with the green and red colored areas can be detected, but the remaining blue area is undetectable even with our proposed approach. The cells in this area have resistance values within the normal cell range, even with the presence of a pinhole. They are excluded from the candidate pool since their resistance value exceeds the maximum reference level set in our trim range.

TABLE I.   CASE STUDIES

Parameter	Case-1	Case-2
#Manufactured chips	10^5	10^5
Chip capacity	1MB	8MB
Word length	128	256
ECC budget	2*	2*

* One bit reserved for field failures caused by sources other than the pinhole

TABLE II.   MTJ PARAMETERS

Parameter	Value
Oxide barrier thickness	0.9nm
Free layer thickness	0.85nm
MTJ surface	60nm×60nm
Resistance-area product	4.52Ω.μm²
TMR ratio with $V_{bias=0}$	~140%
MTJ resistance	~2.3kΩ, ~5.5kΩ

To show the importance of pinhole defect detection and the advantage of smart hammering, we have performed two case studies, as shown in Table II. We have calculated the required defect coverage for discovering all pinhole defects under the ECC budget and computed what percentage of memory needs to be hammered to capture unrepairable rows with ECC. Table III shows the required pinhole defect coverage, the target reference resistance, whether the target reference resistance is under the max trim, and the percentage of memory that needs to be hammered for both cases. For larger memory sizes, with an increase in word length, number of words, or manufactured chip count, the pinhole defect escape rate will increase; therefore, the need for pinhole detection also increases.

As mentioned before, one of the factors that makes pinhole defect detection more difficult is process variation. Smaller process variation makes defect properties more dominant and easier to differentiate. However, wider process variation makes the differentiation more difficult due to the overlap of the properties of good and marginal cells. To further investigate this issue, we performed the same steps considering a process with half of the variation as before. As we can see in Table III, the number of memory cells requiring hammering reduces at least five orders of magnitude as the overlap among good and marginal cells decreases. In addition, higher pinhole detection is achievable with smaller trim steps.

To further demonstrate the superiority of our method, we have plotted our accuracy and memory hammer percentage against the standard hammering test in which all the cells are hammered (Fig. 8). As we can see, our method can guarantee the chip functionality with a far lower percentage of memory cell hammering. In case-2, our proposed method achieves nearly the same accuracy while only hammering a 3.58% of memory. This gives us a time advantage of up to 96.42% while providing the same quality as the standard test. This is while the only change made was the extension of trim steps.
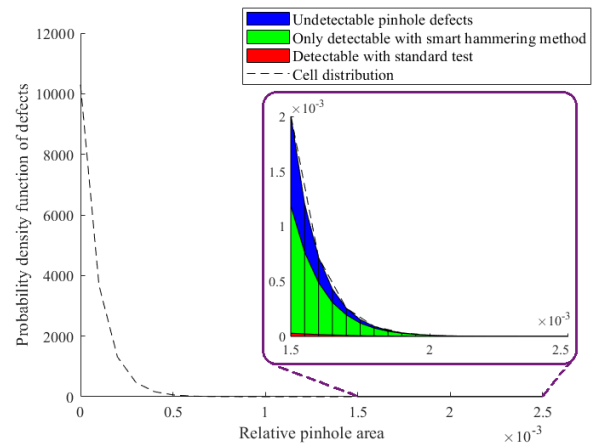

Fig. 7.   Distribution of cells for pinhole defectivity rate of 0.2ppm.

TABLE III. COMPARATIVE ANALYSIS FOR DIFFERENT MEMORY MANUFACTURING PROCESSES

Manufacturing process	Case-1		Case-2	
	Standard	Highly controlled	Standard	Highly controlled
Required pinhole defect coverage	62.45%		97.66%	
Target Reference resistance	4275Ω	4200Ω	4750Ω	4400Ω
Is an extended trim step needed?	No	No	Yes	No
Memory hammer percentage	0.11	2.4×10^{-8}	3.58	3.3×10^{-5}

TEST COST AND COVERAGE

■ Coverage percentage ■ Relative memory access number (test time)

SMART HAMMERING CASE-1: 62.45%, 0.11%
SMART HAMMERING CASE-2: 97.66%, 3.58%
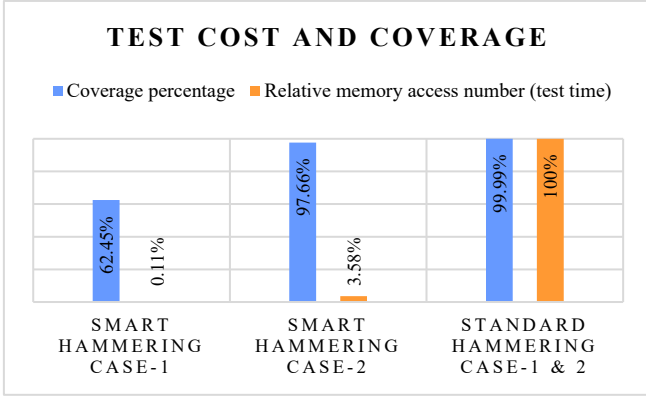STANDARD HAMMERING CASE-1 & 2: 99.99%, 100%

Fig. 8. Comparative analysis of smart vs. standard hammering.

V. CONCLUSION

Pinholes in the MgO layer are one of the most important MTJ defects that are crucial to detect and can cause test escapes and subsequent field failures. In this paper, we have thoroughly investigated their statistical effect on the resistive distribution of STT-MRAMs with pinhole defects to find a methodology that can be used to capture a suspect poll of marginal cells. The smart incremental hammering procedure guarantees reliability and high yield for the final product with a reduced test time of up to 96.42% for our case studies compared to standard hammering solutions. Our approach is compatible with the existing MBIST, only requiring minor modifications to its circuit.

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