Electromigration-aware design technology co-optimization for SRAM in advanced technology nodes

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***Abstract*—Static RAM (SRAM) is one of the critical components in advanced VLSI systems whose performance, capacity, and reliability have a decisive impact on the entire system. It offers the fastest memory in the storage hierarchy of modern computer systems. By moving toward the smaller CMOS technology nodes, the back end of the line (BEoL) interconnects are also fabricated in tighter pitch size. Hence, besides the power lines, SRAM word- and bit-line (WL and BL) are also susceptible to electromigration (EM). Therefore, EM reliability of SRAM's WL and BL needs to be analyzed during design technology co-optimization (DTCO) cycle. In this work, we investigate the impact of technology scaling on SRAM designs and perform a detailed analysis on the trend of their EM reliability and energy consumption. Our analysis shows that although scaling down the CMOS technology can result in a 2.68x improvement in the energy efficiency of the SRAM module, it increases the EM-induced hydrostatic stress by 2.53x.**

I. Introduction

Static random access memory (SRAM) is one of the most demanding memory structures in the storage hierarchy of many modern computers. The conventional SRAM cell has typically a large area. Therefore, utilizing the SRAM for larger cache memories would be too costly. Further, scaling down the technology can significantly improve the area efficiency and performance of the CMOS-based electronic designs [1]. In fact, smaller CMOS, as well as back end of the line (BEoL) interconnect technologies, can be leveraged for the realization of the large and energy-efficient SRAM-based memories.

Besides the performance and energy efficiency gains of the technology scaling, the reliability aspect of the systems fabricated in the advanced technologies is of paramount importance and hence, needs to be considered during the design technology co-optimization (DTCO) cycles. In particular, long-term interconnect reliability needs to be taken into account [2], [3]. By scaling down the CMOS technology, BEoL interconnects are also fabricated in tighter pitch sizes. Therefore, the current density passing through the BEoL interconnects is higher. Moreover, by targeting high-performance applications in large cache memories, the chip temperature becomes higher, and both the high current density and high temperature increase the risk of *electromigration (EM)* [4].

In the literature, interconnects carrying small alternating current, under certain scenarios of *Blech length* satisfaction, are proven to be immortal against EM [5]. Nevertheless, tight-pitch memory word- and bit-line (WL and BL), as required in advanced nm-scale interconnect, when operating at high temperature, are susceptible to the EM. Although the EM vulnerability of the memory BL has already been shown in SRAM [6], [7], and Spin Transfer Torque Magnetic RAM (STT-MRAM) [8], [9], the impact of nm-scale metal lines in scaled memory has not been studied yet.

The impact of the EM on the memory WL, BL, and BL-bar (BLB) heavily depends on the current passing through these lines. The type (read or write), data, and address of the operation change the EM reliability profile of the WL and BL since these factors alter the current passing through the memory lines. Besides the effect of the WL's and BL's current on their EM profile, they have a significant effect on the overall energy and performance. In other words, there is a trade-off between these design merits and DTCO needs to be performed by carefully considering these trade-offs.

In sub-10 nm technology, it has become increasingly challenging to extend the conventional scaling laws. Classical Dennard's lambda scaling rules have broken already. What is left is the economical cost scaling law of Moore's law, and the node terminology for that roadmap is defined by industrial foundries once a new 'node' is put in production. As a workable alternative, advanced technology research has focused on so-called DTCO iterations, where critical parameters in the device and wire fabrication are co-optimized with important (circuit) design parameters. Without such a crucial co-optimization, technology scaling would have stopped already. Hence, in the research phase, the concept of a node does not make sense any longer, and it is not used even by scientists. Instead, the values of the above-mentioned critical parameters are determining the state-of-the-art to compare different results.

In this work, we consider two SRAM technologies, because of the predominant wire focus of this paper, we will mainly focus on CD (critical dimension of a wire), and sometimes pitch (distance between 2 wires) [10]. Specifically, we compare two cases represented by the 22 nm and the 12 nm smallest BL CD, which are respectively referred to as 22 nm and sub-5 nm technology nodes by industry.

Our contributions in this paper are as follows: **i**. Show the trend of the EM risk exacerbation with respect to technology scaling in SRAM WL and BL. **ii**. Perform a detailed analysis on the electrical-level characteristics of the SRAM design and show the access dependency of the EM profile. **iii**. Propose an EM-aware DTCO for the advanced SRAM design based on 12 nm CD.

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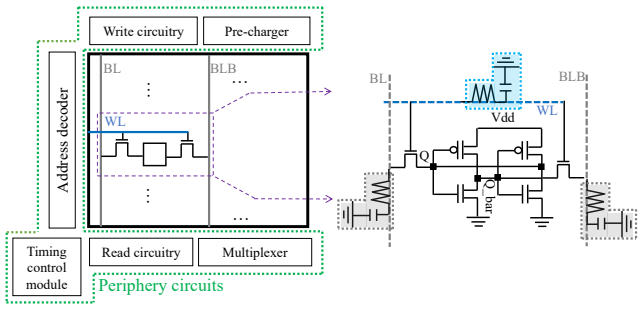

Fig. 1. (a) Schematic of the SRAM sub-array, including the SRAM crossbar and the required periphery circuits, (b) the transistor-level schematic of the SRAM cell and the corresponding WL and BL parasitic

II. Background and Related Work

A. SRAM organization

An SRAM memory is organized in a hierarchical structure. As is shown by Fig. 1 (a), the smallest organization is *sub-array* which consists of the SRAM crossbar and the required periphery circuits, including address decoder, read and write circuitries, multiplexers, timing control module, and pre-charger. To ensure the reliability of the SRAM operation, after each access cycle, the BL and BLB are pre-charged to a certain voltage level which in our design, is V_{DD}.

B. EM phenomenon and modeling

In the current-carrying conductor, the conducting electrons transfer momentum to the atomic metals and force them to *migrate* from their positions, and consequently, *void*, is created in the specific position of the interconnect. The creation of the void increases the resistance of the interconnect and finally, leads to timing violations and failures.

Modeling of the EM such that all the involved parameters have actual physical correspondence or *physical-based modeling* (in contrast to the empirical modeling) is desirable since it enables the exploration and optimization of the design parameter during the DTCO. The main equation of the physical-based modeling is Korhonen's partial derivative equation (PDE) [11]. The problem with Korhonen's PDE is that it can capture the $\sigma(x,t)$ as a function of *constant* current density.

1) Steady-state EM modeling:

In BEoL fabrications, interconnects have resistive (R) and capacitive (C) parasitic. Fig. 1 (b) shows a realistic segmented RC model of the SRAM WL and BL by considering an RC element corresponding to each SRAM cell. The effect of such *segmented* wire is that the current passing through the segments is not equal for all the segments. Therefore, Korhonen's PDE which captures the *constant* current density is not proper modeling.

EM modeling in the *steady-state* has been suggested for dealing with the multi-segment interconnect [12]. For a multi-segment interconnect the following equations are valid.

$$\sigma(x) = \frac{Ze\rho}{\Omega} jx + \sigma_{res} \tag{1}$$

$$\sigma_i^c - \sigma_j^a = \Delta\sigma_{ij} = \frac{-eZ\rho(j_{ij} \times l_{ij})}{\Omega} \tag{2}$$

$$\sum_{i,j=1}^{k} \left(\sigma_i - \left[\sigma_t - \frac{eZ\rho(j_{ij} \times l_{ij})}{2\Omega} \right] \right) l_{ij} = 0 \tag{3}$$

In Eq. (1)-(3), x represents the location, Z is the effective valance charge, e is the electron charge, ρ is the metal resistivity, Ω is the atomic lattice volume, and j is the current density. Moreover, σ_{res} is the initial stress that existed in the interconnect due to its fabrication procedure. Eq. (1) can be derived from the solution of Korhonen's PDE by having the transient variable $t \to \infty$ [13]. Eq. (2) is obtained from Eq. (1) by the consideration of one wire segment (with the length of l_{ij} between nodes i, j). Furthermore, Eq. (3) ensures the satisfaction of the *mass conservative law*, while σ_t is the thermal stress.

C. Related work

The EM susceptibility of the memory BL has been investigated in several related works. In [6], [7], the susceptibility of the SRAM's BL has been studied. The EM modeling which has been used in this work is Black's equation that obtains the EM-induced mean time to failure [14]. Due to the empirical nature of Black's equation, it cannot capture the direct effect of different design parameters such as the wire length (l), and hence, such formulation cannot be used during EM-aware DTCO. Moreover, although the BL has been modeled as a segmented wire with distributed RC network, its effect on the unequal segment current has not been taken into account. On the other side, [8], [9] investigate the effect of the EM on the BL of the STT-MRAM. The authors have considered the physical-based EM modeling and analyzed the data-dependent impact of the EM on the BL of the STT-MRAM. However, due to ignorance of the wire RC parasitic, the address dependency and effect of the segmented wire have not been studied in [8], [9]. To the best of our knowledge, in this paper, we are the first to comparatively investigate the EM reliability of the WL and BL of the SRAM under strong access-dependent conditions. Hence it is not possible for us to perform a quantitative comparison with related work. So, only qualitative statements are provided above.

According to the *Blech length constraint*, the longer the line, the more susceptible to EM [5]. Although there are other long lines exist in the large SRAM macros (such as interconnect networks), the main focus of this work is to investigate the impact of EM on the WL and BL. Due to the severe space limitation inside the SRAM sub-array, WL and BL have the tightest pitch size, and hence, are more susceptible to EM.

III. EM-aware DTCO Methodology

Fig. 2 shows our proposed EM-aware DTCO methodology. The *temperature*, *standard voltage*, *wire parasitic* and *BEoL wire dimensions* are the input for our proposed EM-aware DTCO mechanism. Our aim is to find the largest SRAM size, working at the highest performance, however, by ensuring the satisfaction of the EM reliability criteria, which is the maximum current density (j_{max}).

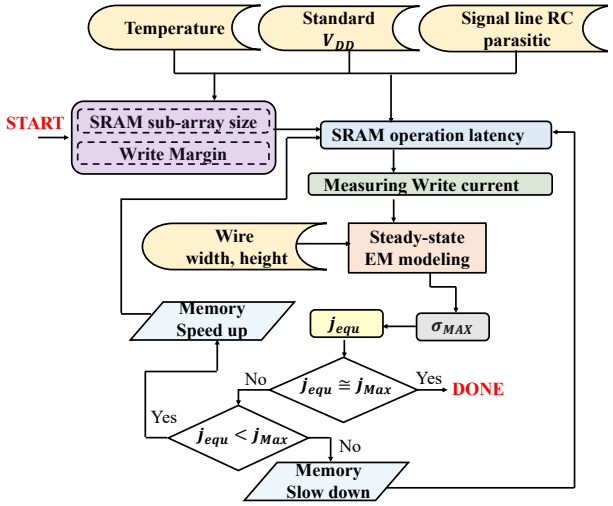

Fig. 2. The proposed EM-aware DTCO methodology for SRAM fabricated in 12 nm CD

A. SRAM sub-array size

Obtaining the *SRAM sub-array size* (number of rows and columns) is crucial for DTCO, typically, having large memory sub-arrays are beneficial for the overall performance and energy efficiency, however, large resistive parasitic results in SRAM writing failure. In resistance-dominated advanced tight-pitch interconnect, the increased BEoL resistance per unit length has degraded the SRAM write margin [15]. Applying the negative write voltage driver is one of the mechanisms that can improve the SRAM writability [16]. We also utilize the negative write driver and try to maximize the SRAM sub-array size by using this *write assist mechanism*.

To have a fair comparison between the SRAM designs based on 22 nm and 12 nm CD, we consider the same sub-array size in both technologies, which is determined based on the maximum possible size in SRAM, based on 12 nm CD. During the proposed EM-aware DTCO, we increase the SRAM sub-array size until it is limited by the SRAM writability.

B. EM reliability analysis

For the copper-based BEoL interconnect corresponds to the 12 nm CD, which is also longer than $5\mu m$, the maximum allowed current density (j_{max}) (For 10 years EM lifetime) is drastically decreasing to $\sim 1\frac{MA}{cm^2}$ [17].

Increasing the current density far beyond this value increases the risk of EM failure. Nevertheless, investigating this criterion in the interconnects with RC parasitic can be misleading. As discussed in section II-B1, the current for the segmented SRAM WL and BL is not equal for all the segments and the value of the current is heavily access-dependent. Hence, generalizing the current passing through one segment to the entire line may either overestimate or underestimate the EM risk.

1) EM-aware equivalent constant current density:

To address the issue of non-constant current in the interconnect segments, we propose to use an *EM-aware equivalent constant current density* (j_{equ}). If a realistic segment-dependent current density induces $\sigma^{\text{MAX}}_{\text{steady-state}}$, the ($j_{equ}$) is a constant *segment-independent* current density that induces the same $\sigma^{\text{MAX}}_{\text{steady-state}}$ on the wire.

Monitoring the j_{max} needs to be done based on the access that results in the highest current passing through the line. The SRAM write operation typically results in a much higher current than the read operation. The change of the BL (or BLB) voltage during the read operation is relatively smaller than the write operation. In read operation $\Delta V_{\text{either BL or BLB}} \geq SM_{\text{sense amplifier}}$ (SM: sense margin). However, the write operation requires the change of the BL (or BLB) voltage to 0 V. Moreover, utilizing the negative write driver to improve the writability of the SRAM, particularly in the 12 nm CD, results in an even higher voltage drop on the BL. So, due to the larger current during the SRAM write, we consider this operation for our proposed EM-aware DTCO mechanism.

2) Trade-off between the EM reliability and performance:

To investigate the EM reliability, we take into account the maximum induced stress at the steady-state through Eq. (1)-(3), which requires the current of each segment. The current passing through the WL and BL of the SRAM is access dependent; in other words, it varies depending on the access (read or write), data and address. Taking into account the address dependency implies activating each memory address and measuring the currents, which is extremely effortful. Moreover, besides the access dependency of the write current, measuring the current of all the segments of the SRAM sub-array is not practical. To overcome this issue, we consider all four transitions in the write operation: $0 \rightarrow 0$, $0 \rightarrow 1$, $1 \rightarrow 0$, and $1 \rightarrow 1$, however, only on a limited number of selected rows. These selected rows are located at first (closest to the write driver and the pre-charger, and farthest from the sense amplifier), middle, and end (farthest from the write driver and pre-charger, and closest to the sense amplifier) of the sub-array. Moreover, for each activated row, we only sample from the current of a few segments, and *extrapolate* the rest, by fitting the current samples to a polynomial curve.

By having the current-segment information, we can obtain the steady-state σ_{max} and eventually, the j_{equ}. If the j_{equ} is less than the j_{max}, it implies that there is still room to decrease the SRAM latency. Otherwise, the latency of the SRAM needs to be compromised to meet the EM reliability criterion: for the interconnect corresponds to 12 nm CD, $j_{max} \leq\sim 1\frac{MA}{cm^2}$. To find the optimized point for the latency and EM-reliability, we tune the SRAM operating cycle in such a way that the current density of both the WL and BL is close to $\sim 1\frac{MA}{cm^2}$.

IV. Results and Discussion

The technology parameters corresponding to 22nm and 12nm CDs which are used for our analysis are summarized in Table I. The temperature has been selected by targeting the high-performance cache units. Moreover, as it has already been discussed in Section III-A, the size of the SRAM sub-array has been determined based on the 12 nm CD, which has a degraded write margin of $\sim$-570 mV, compared to the write margin of 0 V in 22 nm CD technology. In the 12 nm

TABLE I
PARAMETERS FOR CO-SIMULATION OF THE ENERGY AND EM RELIABILITY

Parameter	**22 nm CD**	**12 nm CD**
Temperature ($^{\circ}C$)	100	
Array organization	256 Rows and 256 Columns	
Standard V_{dd} (mV)	800	700
Wire length per cell (nm)	BL = 231 WL = 220 [18]	BL = 90* WL = 168*
Wire (Width/Height) (nm)	BL: (22/41.8) WL: (22/41.8) [18]	BL: (12/12)** WL: (13/26)**
Copper resistivity (ρ_{Cu}) ($\Omega \cdot nm$) [19]	6.8e-8	9.5e-8
Wire ($R(\Omega), C(aF)$) per cell	BL: (35.18, 89.92) WL: (24.09, 61.59) [18]	BL: (74.47, 37.7)* WL: (13.07, 107)*

* information extracted through the layout
** information extracted through the model fitting

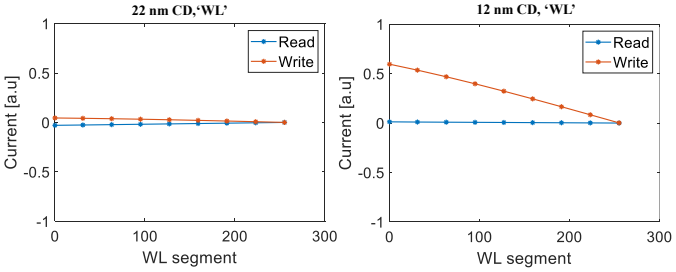

Fig. 3. The current versus the WL segment during the read and write operations in two 22 nm and 12 nm CD technologies

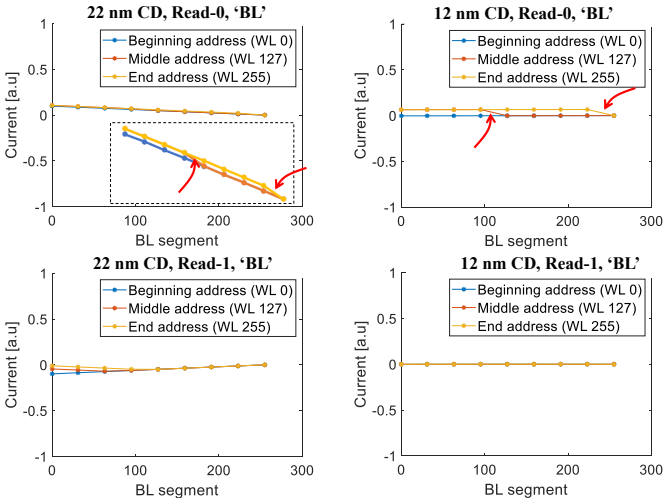

Fig. 4. The current versus the BL segment during the read operation in two SRAM designs based on 22 nm and 12 nm CD, red arrows show the sudden decrease of the current at the activated segment during read-0

TABLE II
SUMMARY OF THE RESULTS FOR PERFORMING THE EM-AWARE DTCO ON THE SRAM BASED ON 22 nm AND 12 nm CD

Parameter	**22 nm CD**	**12 nm CD**
EM reliability criteria (j_{max}) [17]	$\leq\sim 3.5 \frac{Ma}{cm^2}$	$\leq\sim 1 \frac{Ma}{cm^2}$
EM-aware DTCO analysis	Not required ($j \sim 0.589 \frac{Ma}{cm^2}$)	Required
Achieved j after DTCO (WL)	–	$0.884 \frac{Ma}{cm^2}$
Achieved j after DTCO (BL)	–	$1.04 \frac{Ma}{cm^2}$

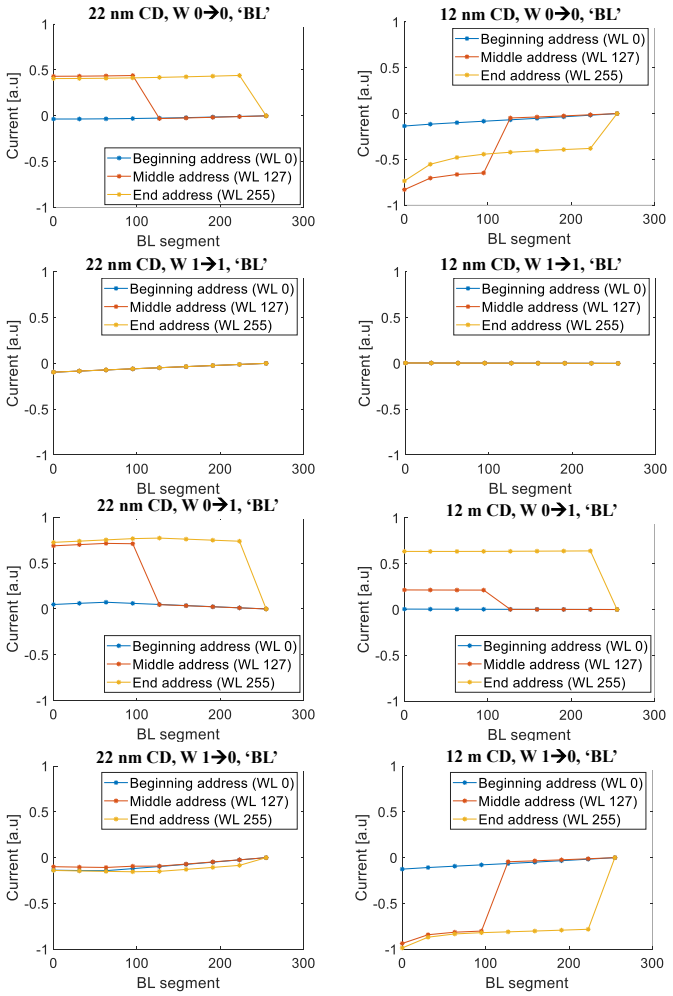

Fig. 5. The current versus the BL segment during the write operation in two SRAM designs based on 22 nm and 12 nm CD

TABLE III
SUMMARY OF THE COMPARISON IN SRAM BASED ON 22 nm CD AND 12 nm CD, THE PARAMETERS ARE NORMALIZED TO VALUES BASED ON 22 nm CD

Design Merit	**22 nm CD**	**12 nm CD**
SRAM cell area	1	0.214
Operating Cycle	1	0.531
Average Read PDP	1	0.318
Average Write PDP	1.514	0.685
EM-driven stress, BL, Read	1	1.329
EM-driven stress BL, Write	4.012	14.304
EM-driven stress WL, Read	0.187	0.433
EM-driven stress WL, Write	7.835	22.785
C.V for Stress values dispersion (access dependency)	1	1.548

CD, the wire length per cell, as well as the RC parasitic have been extracted from the layout. While the wire width and height have been obtained by using the R and C model as a function of wire length and ρ_{Cu} [18]. For 22 nm CD, the wire dimensions, as well as the RC parasitic, have been extracted from NVSim [18].

A. Required periphery circuit for the SRAM sub-array

The sense amplifier circuit simulated for both the 22 nm and 12 nm CD technologies is a latch-type sense amplifier

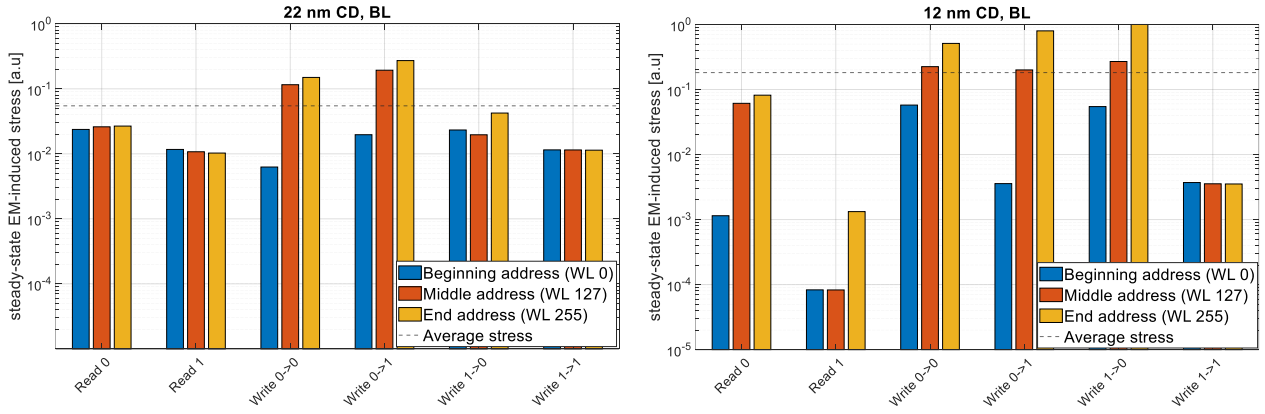

Fig. 6. Steady-state hydrostatic stress on the BL, based on 22 nm and 12 nm CD

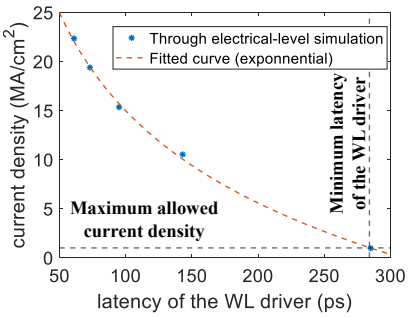

Fig. 7. The WL current density versus the latency of the WL driver

from [20], the write drivers are based on the active-high inverting tri-state buffers, and the pre-chargers are consists of a P-FET element.

B. Impact of the access dependency on the current passing through the WL and BL

As discussed in Section III-B1, the current passing through the WL and BL is access dependent. As we will discuss, this access dependency is not similar for the WL and BL.

1) WL: Charging the WL is required to make the row accessible. Among the access-dependent parameters (access type, data, and address), only access type affects the current passing through the WL. Since the duration of the time that the WL is activated is not equal for the read and write operations. Fig. 3 shows that the current versus segment for both the 22 nm and 12 nm CD technologies is *linearly* decreasing with the number of segments, in other words, by getting farther away from the WL driver.

2) BL: The current passing through the BL shows significant access dependency not only to the type of SRAM operation but also to the data and address. We investigate the segment dependency of the BL current for read and write operations. As discussed in Section III-B1, and also shown in Fig. 4, the read current is typically lower. In the case of read-0, the BL current shows a sudden decrease at the activated segment which is not the case in read-1. For each SRAM operation, the BL (and BLB) are pre-charged to V_{DD}. In the case of read-0, a current path from the BL and through the SRAM cell is forming, which results in the sudden decrease of the current at the activated segment (which is marked with the *red arrow* in Fig. 4). Due to the non-existence of voltage drop between the BL and the SRAM cell which stored '1', the current is decreasing linearly in the case of read-1.

Fig. 5 shows the segment-dependent current passing through the BL of the SRAM during the write operation. Similar to the read operation, in case of the existence of the voltage drop between the BL and SRAM cell, the sudden decrease of the BL current happens at the segment corresponding to the activated row. Please note that after each SRAM operation, the BL and BLB are pre-charged to V_{DD}. Therefore, for Write $\rightarrow$ 0, the BL needs to be discharged, hence the BL current for this operation is relatively higher. As already discussed in Section III-A, the negative write driver has been considered for the SRAM design based on the 12 nm CD, so the BL needs to be discharged to a negative value (in other words, a higher voltage drop). Therefore the write current in this technology is even higher.

On top of the current magnitude, the negative write driver affects the current direction. Please note the different current directions of write 0 $\rightarrow$ 0 in 22 nm and 12 nm CD designs which are '+' and '-', respectively. Moreover, in the 12 nm CD, transistors have lower *threshold voltage* (V_{th}), and hence, higher current. Besides the higher current, the smaller cross-sectional area of the BEoL WL and BL in the 12 nm CD results in relatively high current density (j).

C. Impact of the access dependency on the EM reliability

Fig. 6 shows the access dependency of the EM-induced hydrostatic stress of the SRAM's BL in both 22 nm and 12 nm CD. The average EM-induced stress is significantly higher in the 12 nm CD, and typically, write operation results in higher stress. The access dependency of the EM profile is observed in both 22 nm and 12 nm CD. For instance, in both of the designs, performing the write operation on the end rows of the SRAM sub-array results in considerably higher stress on the BL, compared to performing the same operation on the beginning addresses. Although the access dependency of the EM profile exists for both 22 nm and 12 nm CD designs, the significance of its impact on the dispersion of the stress values is technology-dependent. We use the *coefficient of variation*

(C.V = $\frac{mean\ (\mu)}{standard\ deviation\ (\sigma)}$*)* as the statistical metric to show the effect of the access dependency on the EM profile. The higher the C.V, the more significant the access dependency of the EM profile.

In our simulations, we focus on the individual SRAM operations, in other words, we do not consider the effect of the *access sequence* on the EM profile. As discussed in Section II-A, after each SRAM operation, the BL and BLB are pre-charged until V_{DD}. Such pre-charging almost de-couples the subsequent SRAM accesses. Therefore, the effect of the access sequence on the EM profile is negligible. To the best of our knowledge, such memory access-dependent EM modeling has not been performed yet in the literature, and our results (summarized in Fig. 4, 5, and 6) incorporate these effects.

D. EM-aware DTCO analysis

To perform the EM-aware DTCO we use the methodology discussed in Section III. The EM reliability for the 22 nm CD design is not crucial, since not only the current values are smaller, and BEoL cross-sectional area is larger, but also the j_{max} criteria is far more relaxed; $\sim 3.5\frac{MA}{cm^2}$ compared to $\sim 1\frac{MA}{cm^2}$ for the wire width corresponds to 12 nm CD design [17]. Our method to tune the operating cycle of the 12 nm CD SRAM is adjusting the latency of the WL driver. Fig. 7 shows the j_{equ} of the WL with respect to the latency of the WL driver. In fact, the WL driver needs to be slowed down until the j_{max} criteria can be met. Table II shows the summary of our EM-aware DTCO analysis. In the 12 nm CD design, by increasing the delay of the WL up to $\sim 284\ ps$ (according to Fig. 7), the current density of WL decreases to $\sim 0.884\frac{MA}{cm^2}$. In addition to ensuring the EM reliability of the WL, the same procedure for the BL needs to be repeated. However, our results (based on the parameters outlined in Table I) show that by the aforementioned WL driver slow down, the current density of the BL can also meet the criteria of $j_{max} \sim 1\frac{MA}{cm^2}$, and further slowing down the BL driver (and hence, the entire 12 nm CD SRAM design) is not necessary. Besides, due to the process variation, the BEoL interconnects can be fabricated in a smaller cross-sectional area than the nominal one. Hence, in the more advanced technologies, the process variation can result in the exacerbation of the EM risk even further.

Table III shows a summary of the design merits for the SRAM designs in two earlier introduced, 22 nm and 12 nm CD. The cell area is obtained through the SRAM layout in 22 nm and 12 nm CD technologies. While the operating cycles, average read and write power-delay-product (PDP) are based on our electrical-level simulations on both the 22 nm and 12 nm CD designs. Finally, the stress values have been obtained through the steady-state stress modeling (Section II-B1). Technology scale down (from 22 nm to 12 nm CD) improves the area efficiency, latency, and energy (PDP) efficiency by 4.67x, 1.88x, and, 2.68x, respectively. However, from the EM reliability point of view, technology scale-down exacerbates the EM risk by 2.53x.

V. CONCLUSION

Due to the technology scaling, BEoL interconnect are also fabricated in tighter pitch size. Smaller cross-sectional area of the interconnect, higher switching speed of transistors, as well as the higher chip temperature in dense and high performance VLSI designs, exacerbates the EM risk even for the memory WL and BL. In this work, we have performed a detailed analysis on the SRAM designs in two technologies with different wire critical dimensions. We have shown the necessity of the EM-aware DTCO for the advanced technology designs, and proposed a mechanism for it. We have shown that though scaling down the transistor size and BEoL CD is promising in terms of the performance, and energy efficiency, it dramatically increases the EM risk.

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