Fast Performance Evaluation Methodology for High-speed Memory Interfaces

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***Abstract*—An increase in the data rate of memory interfaces causes higher inter-symbol interference (ISI). To mitigate ISI, recent high-speed memory interfaces have started employing complex datapath, utilizing equalization techniques such as continuous-time linear equalizer and decision-feedback equalizer. This incurs huge overhead for design verification with conventional methods using transient simulation. This paper proposes a fast and accurate verification methodology to evaluate the voltage and timing margin of the interface, based on the impulse sensitivity function. To take nonlinear circuit behavior into account, the small- and large-signal responses were separately calculated to improve accuracy, using the data obtained from the periodic AC and periodic steady-state analyses. This approach achieves high accuracy, with shmoo similarity rates of over 95 %, while also significantly reducing verification time, up to 23× faster. Moreover, two different methods are proposed for evaluating the multi-stage Rx performance, providing a trade-off between accuracy and efficiency that can be tailored to the specific purpose, e.g., the verification or design process.**

***Index Terms*—Memory interface, performance evaluation, timing/voltage margin, shmoo plot, impulse sensitivity function**

I. Introduction

As the data rate of the memory interfaces increases, the interface circuits grow more complex and the challenge of accurately verifying the designed circuit becomes more pronounced. To evaluate the performance of receiver (Rx) circuits, voltage and timing margins are generally checked at a target bit error rate (BER) or through a shmoo test. In the memory industry, the shmoo test is often used to determine the superiority of interface circuits among competitors. Memory companies manage the margin as a principal performance indicator. The shmoo test is essential for evaluating transceivers' characteristics and performance, or for indirectly examining the eye diagram on the receiving side.

The impact of channels on the interface circuit performance becomes more severe as the data rate increases. To compensate for the channel loss, various design techniques, such as continuous-time linear equalizers (CTLEs) and decision-feedback equalizers (DFEs), are being applied for high-speed memory interfaces. Moreover, these equalizers are designed with adjustable control knobs to cover variations in interface circuits and channels.

A single point on the shmoo indicates whether the transmitted data and the received ones are identical under the corresponding setting of transceivers, e.g., driver strengths, termination resistors, reference voltage, clock timing, coefficients of DFE, and various other settings. It takes a significant amount of time to fill out the entire shmoo with the transient simulation, and checking the shmoo with the combination of multiple settings in the iterative design process is practically impossible. For instance, if the number of DFE taps increases, the number of evaluation targets increases exponentially.

Therefore, in order to design a robust high-speed memory interface, there is a need for an efficient method to evaluate the interface performance. The evaluation method should be much faster than the existing verification procedure while maintaining accuracy. To tackle this challenge, this paper presents a fast performance evaluation methodology for high-speed interface circuits. The proposed method can characterize the voltage and timing margin at the receiver for the transmitted signal in an efficient manner, utilizing an impulse sensitivity function (ISF) of a linear periodically time-varying (LPTV) system.

Specifically, this paper makes the following contributions:

- To accurately evaluate the performance of nonlinear interface circuits, the proposed method separates small- and large-signal analyses and processes them separately. To the best of our knowledge, this is the first work presenting a practical performance evaluation methodology, whereas previously only small sub-block circuits like clocked comparators have been characterized using small-signal analysis based on ISF.
- The proposed method enables fast evaluation with high accuracy. In the case of a simple receiver (such as LPDDR4,5), the obtained shmoo results are about 97 % similar to the reference shmoo obtained by HSPICE transient simulation, and it is 23× faster.
- The proposed method is also applied to a high-speed interface system with both a linear (CTLE) and a nonlinear equalizer (DFE) to validate its effectiveness. Compared to the conventional method, it shows over 3.8× speedup with around 98 % similarity.

II. Impulse Sensitivity Function for Periodic System

A linear time-varying (LTV) system satisfies the superposition principle but not the time-invariance property. The response $y(t)$ of an LTV system to an input $x(t)$ can be expressed as an integral formula [1].

$$y(t) = \int_{-\infty}^{\infty} h(t,\tau) \cdot x(\tau) d\tau \tag{1}$$

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where a time-varying impulse response $h(t,\tau)$ describes the system response at time t for an impulse arriving at time τ.

The clocked comparator is a critical element in a receiver as it makes a decision on the incoming data based on the polarity of input signals. While the comparator is generally considered a nonlinear circuit due to its rail-to-rail amplification behavior, its detailed phases can be treated as a linear system [2]. Additionally, Rx that includes a clocked comparator operates periodically by reset, and since its characteristics vary depending on the sampling time, it can be treated as an LPTV system [3]. For LPTV systems, the impulse response $h(t,\tau) = h(t+T,\tau+T)$ where T is the period of operation.

In order to analyze and model the receiver as an LPTV system, we first introduce the definition of ISF. The ISF is defined as a time-varying impulse response evaluated at a particular observation time t_{obs}: ISF $\Gamma(\tau) = h(t_{obs},\tau)$. This concept has been applied in the analysis of phase noise in oscillators and the characterization of periodic circuits, such as clocked comparators [4-6]. The ISF of a clocked comparator describes many of its key performance characteristics. The input value around the time of the peak ISF is integrated and sampled by the comparator. The width and area of ISF correspond to the sampling aperture and the DC sampling gain, respectively. Additionally, the Fourier transform of ISF represents the sampling bandwidth [2]. It is noteworthy that the response at a particular time to stimulated input can be known according to the ISF definition in (2).

$$y(t_{obs}) = \int_{-\infty}^{\infty} h(t_{obs},\tau)\cdot x(\tau)d\tau = \int_{-\infty}^{\infty} \Gamma(\tau)\cdot x(\tau)d\tau \tag{2}$$

The approaches to obtain ISF for a clocked comparator have been introduced in [3,7]. Comparator metastability was obtained through transient simulation, and sensitivity was defined therefrom to characterize ISF in [7]. The feedback made it reach the metastable state quickly, but it still took a long simulation time. Moreover, it may cause a numerical error because it cannot apply the ideal step pulse for differentiation. In [3], an efficient method was proposed for characterizing the ISF of a clocked comparator using periodic AC (PAC) analysis.

The PAC simulation, which is available by RF circuit simulators like Cadence SpectreRF, computes the series of transfer functions for the fundamental frequency and its various harmonic sidebands. PAC is a small-signal analysis similar to a well-known AC analysis, and the only difference is that the circuit is linearized around a periodically varying operating point instead of a DC operating point. Linearizing at a periodically time-varying operating point allows analyzing transfer functions that include frequency translation due to time-varying properties. In an LPTV system, when a sinusoidal stimulus at frequency ω is applied, the harmonic sideband is modulated and multiple responses appear at $\omega + m\omega_c$, where $m\omega_c$ means the fundamental frequency ω_c and its m-th sideband, and this behavior can be captured by the PAC analysis. In other words, the sideband transfer functions $H_m(j\omega)$ for sinusoidal excitation can be obtained through PAC. It corresponds theoretically

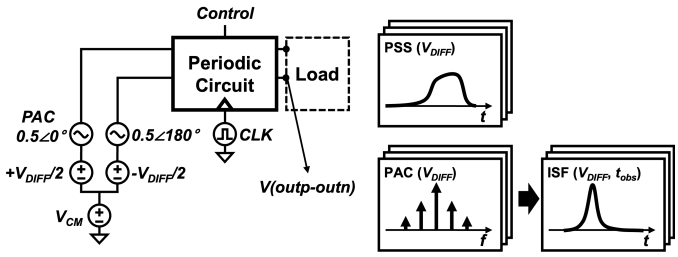


Fig. 1: Characterization of a periodic system.

to the Fourier coefficients of the transfer function of the time-varying system:

$$H(j\omega;t) = \sum_{m=-\infty}^{\infty} H_m(j\omega)\cdot e^{jm\omega_c t} \tag{3}$$

The Fourier transform of the periodic impulse train is:

$$X(j\omega) = \frac{\omega_c}{k}\sum_{n=-\infty}^{\infty}\delta(\omega - n\frac{\omega_c}{k})\cdot e^{-j\omega\tau} \tag{4}$$

An approximate time-varying impulse response can be obtained by substituting equations (3) and (4) and expressing it in the frequency domain.

$$h(t,\tau) \cong \frac{1}{kT}\sum_{n=-\infty}^{\infty}\sum_{m=-\infty}^{\infty} H_m(jn\frac{\omega_c}{k})\cdot e^{jm\omega_c t}\cdot e^{jn\frac{\omega_c}{k}\cdot(t-\tau)} \tag{5}$$

The ISF $\Gamma(\tau)$ is a subset of $h(t,\tau)$ when only $t = t_{obs}$. Equation (6) is used to calculate the ISF from the PAC simulation results.

$$\begin{aligned}\Gamma(\tau) &= h(t_{obs},\tau)\\ &= \frac{1}{kT}\sum_{n=-\infty}^{\infty}\sum_{m=-\infty}^{\infty} H_m(jn\frac{\omega_c}{k})\cdot e^{j\{m\omega_c t_{obs}+n\frac{\omega_c}{k}\cdot(t_{obs}-\tau)\}}\end{aligned} \tag{6}$$

III. Characterizing Rx Using Periodic Analysis

We now describe the details of the characterization used for our method. As mentioned earlier, the term obtained through PAC simulation is $H_m(jn\frac{\omega_c}{k})$ in (6), where $\frac{\omega_c}{k}$ is the step size of the input frequency and ω_c is the fundamental frequency. In practice, m and n in (6) should be set to a finite range, and in our case, their range is set from -50 to 50. For each m and n, harmonic responses are recorded to compute ISF.

Performing PAC simulation requires a Periodic Steady-State (PSS) simulation. PSS is a large-signal analysis that determines the period and periodic operating point that results in a steady state. The PSS analysis is performed iteratively until all node voltages and branch currents fall within a specified tolerance.

In order to perform PSS and PAC simulations, a testbench for a periodic block is configured as shown in Fig. 1. The testbench includes the parameters for the DC offset V_{DIFF} and input common mode voltage V_{CM}, which are set based on the output of the preceding block. The PSS simulation stores the output waveform during a period into a look-up table (LUT). The usage of PSS in the proposed method will be described

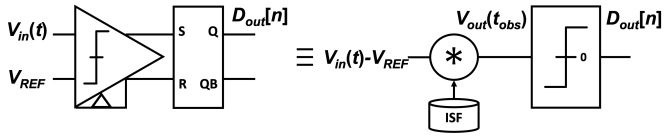


Fig. 2: ISF-based modeling for a clocked comparator.

in detail in Section IV. Based on the formula (6), the results of PAC are transformed into the ISF at t_{obs}, and these results are also stored as an LUT. In the following, how to efficiently evaluate performance using the characterized LUTs of PSSs and ISFs will be described.

IV. Proposed Evaluation Method

A. ISF-based Modeling for Clocked Comparator

We propose an efficient performance evaluation methodology using the ISF-based modeling. The proposed approach is first applied to the clocked comparator, the key building block of the unmatched Rx, and then expanded to more complex circuits.

Note that the contour of a shmoo plot is primarily governed by the decision error from the small-signal input to the clocked comparator. Therefore, the ISF-based modeling method is a very efficient approach because the ISF represents the time-varying sensitivity profile of the output with respect to small-signal inputs, and the proposed method is especially useful when the timing and voltage margins from a shmoo need to be characterized.

The ISF is the time-varying impulse response corresponding to a specific observation time t_{obs}, i.e., $\Gamma(\tau) = h(t_{obs}, \tau)$, where t_{obs} is the time point at which sampled data is delivered to the next sequential logic blocks, such as latches or flip-flops. Using ISF, the behavior of a clocked comparator can be modeled equivalently as shown in Fig. 2 [2].

$$V_{out}(t_{obs}) = \int^{Period} \Gamma(\tau) \cdot \{V_{in}(\tau) - V_{REF}\} d\tau \tag{7}$$

$$D_{out}[n] = \begin{cases} 1 & \text{if } V_{out}(t_{obs}) > +V_{THRE} \\ 0 & \text{if } V_{out}(t_{obs}) < -V_{THRE} \\ X(Meta) & \text{otherwise} \end{cases} \tag{8}$$

where $\pm V_{THRE}$ denotes the logic threshold voltage level of the latch in the next stage. As shown in (7), the output voltage at t_{obs} is calculated by integrating over one period, and then the output logic value can be determined based on the logic threshold.

Note that, because the PAC analysis assumes that the circuit responds linearly in a small-signal fashion to the sinusoidal stimulus, (7) is valid only when the input to the comparator is sufficiently small. In practice, even a small input (tens of mV) can cause a huge error in (7). This can be clearly seen from Fig. 3, which shows the output voltage of a clocked comparator over input stimuli. It compares transient simulation and calculation results obtained from (7). While the output for the small-signal is accurately calculated, the calculation error starts growing when the input becomes larger than 2.5 mV or so, as illustrated in Fig. 3.

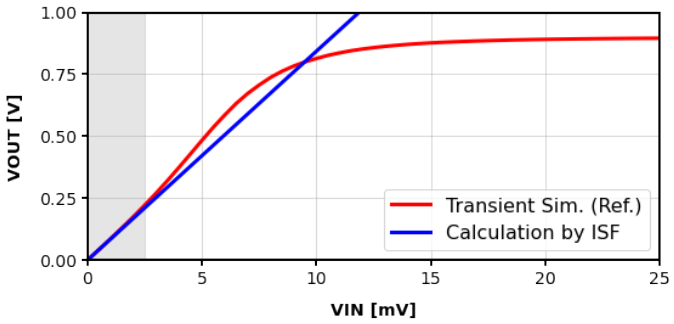


Fig. 3: Accuracy of the small-signal analysis by ISF.

To improve accuracy, nonlinear behavior due to the large-signal response should be taken into account. To this end, the input signal is decomposed into two terms: $V_{in}(t) = V_{IN} + v_{in}(t)$, where V_{IN} is the DC value that decides the large-signal behavior and $v_{in}(t)$ is the small-signal value that changes over time. Then, the final output voltage $V_{out}(t_{obs})$ is the sum of the values obtained from each input term as follows:

$$v_{out}(t_{obs}) = \int^{Period} \Gamma(\tau) \cdot \{v_{in}(\tau) - V_{REF}\} d\tau \tag{9}$$

$$V_{OUT}(t_{obs}) = PSS(t_{obs})|_{V_{DIFF}=V_{IN}} \tag{10}$$

$$V_{out}(t_{obs}) = v_{out}(t_{obs}) + V_{OUT}(t_{obs}) \tag{11}$$

As shown in (9), the small-signal output is calculated in the same manner as (7). Note that its input is the small-signal part $v_{in}(t)$ without the DC value V_{IN}. The output corresponding to the input offset V_{IN} is considered as a large-signal output, which can be extracted from the output node waveform obtained from PSS. There is no additional computational overhead as PSS is required when performing PAC analysis.

The proposed method can improve accuracy by considering nonlinear large-signal behavior, and it is highly effective in evaluating circuits that generate the intended input offset, such as DFE. DFE is placed in front of the clocked comparator in the Rx datapath and is utilized to eliminate the inter-symbol interference (ISI) by producing the intended offset based on the preceding data value. Behavior due to this offset cannot be captured accurately by the small-signal analysis only, especially when the DFE tap coefficient is large. In order to apply the proposed method in this case, since both the data input and the offset due to DFE cause large-signal responses, the PSS results should be obtained for various V_{diff} and the DFE tap coefficients. This will be covered in detail in Section IV-B.

From (9-11), the sampled data for each clock cycle can be obtained and compared with the digital reference pattern transmitted from Tx. To generate a shmoo plot, this calculation is carried out repeatedly while sweeping the clock phase ($\Delta\tau$) and V_{REF} voltage level. The detailed procedure is expressed in pseudo-code in Algorithm 1. ISF and PSS are characterized through simulations and calculations and are retrieved from a look-up table. This approach is highly efficient as it allows the program to access a specific index without the need for

Algorithm 1: Generating the Shmoo

Input: $V_{in}, t_{obs}, LUT_{ISF}, LUT_{PSS}, Ref_{pattern}$
Output: $shmoo$

Function `FromDB` $(LUT, index, ..)$ **:**
  Search the closest value in indices
  return selected ISF or PSS

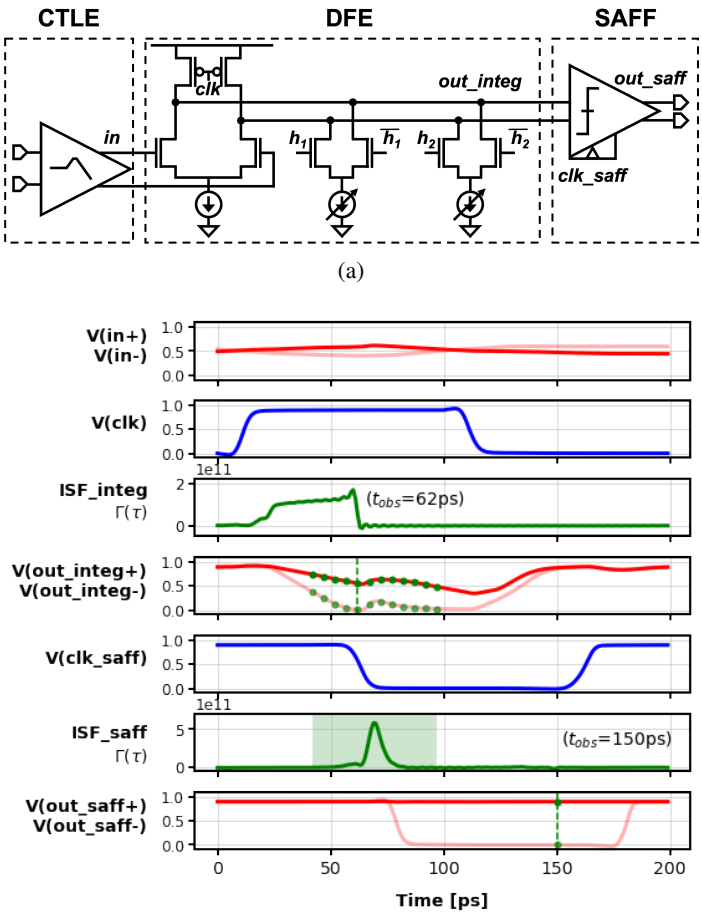
Function `CalculateVout` $(V_{in}(t), t_{obs}, LUT_{ISF}, LUT_{PSS})$ **:**
  $t_{act} \leftarrow$ Activating timing to separate DC
  Let $V_{IN} = V_{in}(t_{act})$ & $v_{in}(t) = V_{in}(t) - V_{IN}$
  $\Gamma(\tau)$=`FromDB`$(LUT_{ISF}, V_{IN}, t_{obs})$
  $PSS(t)$=`FromDB`(LUT_{PSS}, V_{IN})
  Calculate small-signal response from $\Gamma(\tau)$ & $v_{in}(t) \rightarrow v_{out}(t_{obs})$
  Get large-signal response from $PSS(t_{obs}) \rightarrow V_{OUT}(t_{obs})$
  $V_{out}(t_{obs}) = V_{OUT}(t_{obs}) + v_{out}(t_{obs})$
  return $V_{out}(t_{obs})$

Function `ShmooGen` $(V_{in}, t_{obs}, LUT_{ISF}, LUT_{PSS}, Ref_{pattern})$ **:**
  for V'_{REF} in V_{REF} range **do**
    for $\Delta\tau$ in 1 Unit interval **do**
      Initialize $shmoo(\Delta\tau, V'_{REF})$ = PASS
      for n in Bit-stream **do**
        Chop up $V_{in}(t - \Delta\tau)$ during one period $\rightarrow V'_{in}(t)$
        Let $V_{in\_REF}(t) = V'_{in}(t) - V'_{REF}$
        $V_{out}(t_{obs})$=`CalculateVout`$(V_{in\_REF}(t), t_{obs}, LUT_{ISF}, LUT_{PSS})$
        Determine the logic of $V_{out}(t_{obs}) \rightarrow D[n]$
        if $D[n] \neq Ref_{pattern}[n]$ **then**
          Let $shmoo(\Delta\tau, V'_{REF})$ = FAIL
          break
  return $shmoo$

additional calculations and enables the reuse of data for similar inputs.

B. Extension for Multi-stage Rx

We now extend the proposed methodology to multi-stage receivers. For ease of explanation, an example of a typical high-speed Rx circuit is shown, and the waveform corresponding to each node and ISFs at t_{obs} are illustrated in Fig. 4. The Rx circuit in Fig. 4a is composed of a CTLE and a summing block implementing 2-tap DFE, followed by a clocked comparator. The CTLE characteristics can be integrated in the proposed method by either incorporating CTLE into the testbench during the characterization of ISF or by using the CTLE output waveforms as the input for the proposed method. When another periodically time-varying components like DFEs are added in



(a)

(b)

Fig. 4: (a) Circuit schematics of Rx datapath with CTLE and DFE and (b) waveforms illustrating its operation.

the Rx datapath, the proposed methodology can be applied in two different ways:

1) The first is to combine and model periodically operating components together. To obtain ISF by PAC, the system must be an LPTV system. As shown in Fig. 4b, the DFE and the clocked comparator are reset to their initial states for each period, allowing accurate ISF characterization. If this periodic operation is guaranteed, it can be modeled together. The ISF and PSS for the circuit depicted above can be extracted by stimulating an AC source to node in and analyzing the response at node out_saff. When modeling periodically operating components together using a single ISF, it can speed up the evaluation time significantly, but the nonlinear behavior of the comparator (see Fig. 3) may cause a loss of accuracy.
2) The second method is to model each component separately and calculate the response sequentially using the "Divide-and-Conquer" approach. This approach improves accuracy as it reflects the behavior of each component, but it requires more computation as it needs to restore the waveform of the intermediate node. In Fig. 4a, DFE and sense amplifier

Algorithm 2: Extension for Multi-stage Receivers

Input: $V_{in}, t_{obs}, LUT_{PSS0}, LUT_{ISF0}, LUT_{PSS1}, LUT_{ISF1}, Ref_{pattern}$
Output: $shmoo$

Function `ShmooGenExt` ($V_{in}, LUT_{ISF0}, LUT_{PSS0}, LUT_{ISF1}, LUT_{PSS1}, Ref_{pattern}$) **:**
- **for** V'_{REF} in V_{REF} range **do**
  - **for** $\Delta\tau$ in 1 Unit interval **do**
    - Initialize $shmoo(\Delta\tau, V'_{REF})$ = PASS
    - **for** n in Bit-stream **do**
      - Chop up $V_{in}(t - \Delta\tau)$ during one period $\rightarrow V'_{in}(t)$
      - Let $V_{in\_REF}(t) = V'_{in}(t) - V'_{REF}$
      - **for** t_{obs0} in valid range for next bl'k **do**
        - $V_{mid}(t_{obs0})$=`CalculateVout`($V_{in\_REF}(t), t_{obs0}, LUT_{ISF0}, LUT_{PSS0}$)
      - Regenerate $V_{mid}(t)$ of internal node
      - Interpolate $V_{mid}(t)$
      - $V_{out}(t_{obs})$=`CalculateVout`($V_{mid}(t), t_{obs}, LUT_{ISF1}, LUT_{PSS1}$)
      - Determine the polarity of $V_{out}(t_{obs}) \rightarrow D[n]$
      - **if** $D[n] \neq Ref_{pattern}[n]$ **then**
        - Let $shmoo(\Delta\tau, V'_{REF})$ = FAIL
        - **break**
- **return** $shmoo$

flip-flop (SAFF) are characterized separately (from in to out_integ and from out_integ to out_saff). The t_{obs} value of the intermediate node is the entire period, which will be input for the next stage. Therefore, the computation must be performed for each time point. The waveform of the restored intermediate node is used as an input, and the final response is calculated for the clocked comparator. To reduce the computational load, for the regions where the ISF(t) of the next stage is close to zero, the calculation of responses can be skipped, or interpolation can be performed after only calculating key points. This process is described as pseudo-code in Algorithm 2.

We are faced with a trade-off between accuracy and efficiency. The appropriate method should be selected according to the purpose of the analysis.

V. Simulation Results

We applied the proposed method to two types of receivers, assuming an arbitrary memory system environment. Both cases had a data rate of 10 Gbps, with a clock frequency of 5 GHz operating on both edges of the clock. The shmoo was plotted with the following settings:

- V_{REF} ranging from 0 to 300 mV, with a step size of 10 mV
- Clock phase ranging from 0 to 100 ps, with a step size of 2 ps
- Pseudo-random binary sequence (PBRS) 10 bit-stream transmitted by a Tx driver (1023 bits)

To verify the accuracy of the shmoo plot, the results from HSPICE transient simulations were used as references. The circuit simulations were run on a 3.0 GHz Intel Xeon processor with 256 GB of main memory, and the proposed algorithms were implemented in python 3.8.

First, the receiver *Rx-A* scheme consisting only of a clocked comparator was used for comparison. It represents a mobile DRAM and has a structure similar to that of LPDDR4 and LPDDR5. In general, mobile DRAMs are designed to minimize I/O capacitance loading to reduce power consumption. Therefore, there is typically no additional equalizer or extra circuit blocks in these types of receivers. Second, the receiver scheme *Rx-B* was used, which is typically found in computing DRAMs used in servers or PCs, such as DDR4 and DDR5. The structure of this scheme includes CTLE and DFE to improve the signaling in front of the clocked comparator, as previously discussed in Section IV-B.

The discrepancy in the contour of the shmoo plot between the references and the proposed method is shown in Figure 5. Additionally, the results with DFE on and off were compared to further evaluate the accuracy of the proposed method.

In the case of Rx-B with DFE, Fig. 5b-c show the results obtained using the first method described in Section IV-B, combined ISF (Combined), and Fig. 5d-e are the results obtained using the "Divide-and-Conquer" (D&C) method. It can be seen that the DFE's behavior of increasing voltage margins is properly reflected in the results. Additionally, the D&C method shows more accurate results compared to the combined ISF method. In Table I, the accuracy and run-time of the references and the proposed method were compared. The shmoo similarity, used for accuracy comparison, is a numerical value representing the match rate of the shmoo plots. It is defined as the ratio of identical spots to the number of passed spots of the reference shmoo plot. The reference shmoo's eye-opening size varies depending on the channel, but it is sufficient to recognize the relative similarity. The results show a high level of accuracy, with shmoo similarity rates of approximately 95 and 98 % for the combined ISF and D&C methods, respectively. While achieving this high level of similarity with the reference shmoo plots, the execution time is significantly faster than that of transient simulation. Specifically, the combined ISF method was over 8× faster, and the relatively simple Rx-A circuit was even 23× faster.

VI. Conclusion

This paper proposes a fast performance evaluation method for high-speed memory interfaces. The method utilizes LUTs to quickly calculate the response for an input waveform by characterizing the large-signal response and small-signal impulse responses through periodic analysis. The small-signal response is obtained by converting the PAC to ISF, and the large-signal response is obtained from the PSS. The proposed methodology has been extended to evaluate the system with equalizers such as CTLE and DFE, and any circuits with

TABLE I: COMPARISON OF THE ACCURACY AND RUN-TIME FOR THE PROPOSED METHOD

	Rx-A		***Rx-B***				
	Tran.(Ref.)	**Proposed**	**Tran.(Ref.)**	**Proposed (Combined)**		**Proposed (D&C)**	
				DFE off	DFE on	DFE off	DFE on
Remark		Fig.5a		Fig.5b	Fig.5c	Fig.5d	Fig.5e
Shmoo Similarity[1]	**-**	**97.25%**	**-**	**96.44%**	**94.52%**	**98.70%**	**97.80%**
Sim. Time (HSPICE or PAC)[2]	2hr 30min	2min	16hr 15min	1hr 39min		1hr 39min	
Calculating ISF at t_{obs}	-	19sec	-	9min		1hr 46min	
Generating Shmoo	1min	4min	1min	4min		48min	
Total Time	**2hr 31min**	**6min**	**16hr 16min**	**1hr 52min**		**4hr 13min**	
Speedup over Tran.(Ref.)	**-**	**23.53×**	**-**	**8.69×**		**3.85×**	

[1] Shmoo similarity is calculated as the ratio of identical points to the total number of passing points of the reference shmoo.
[2] Max. concurrent processing is set to 20.

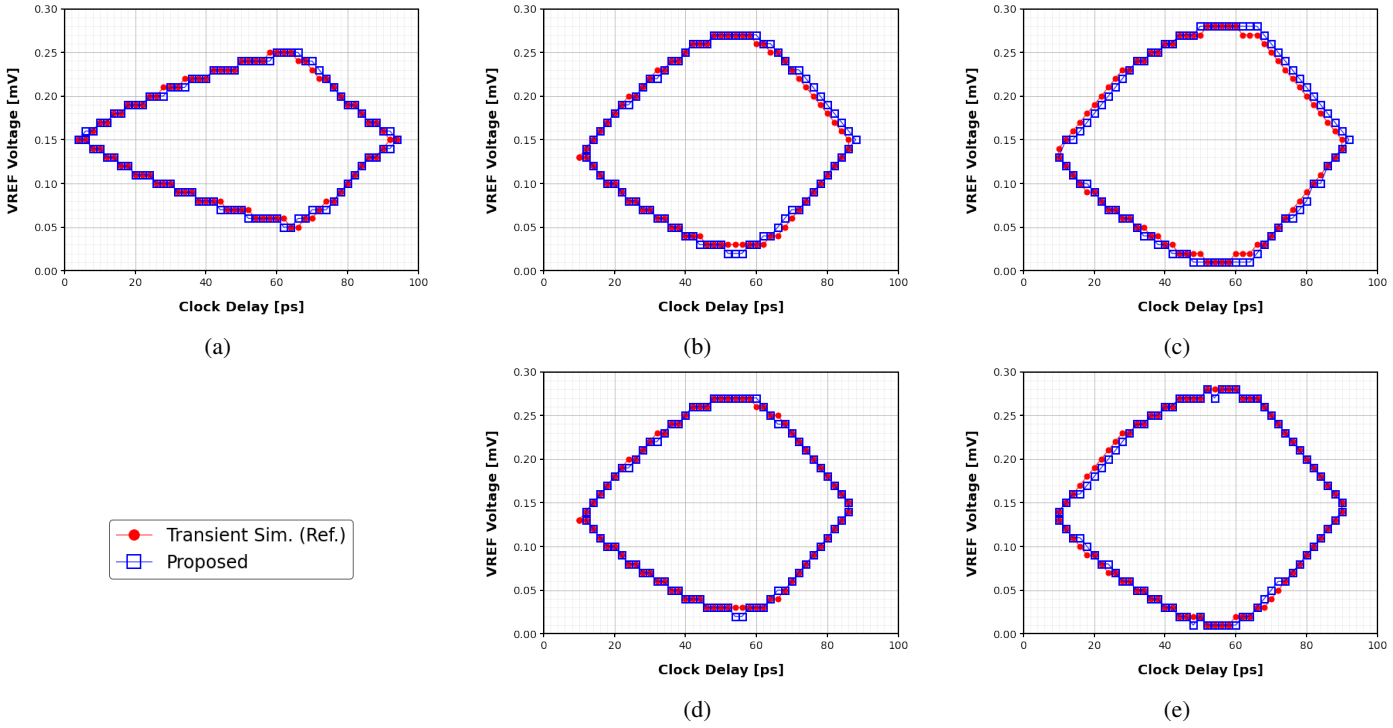


Fig. 5: Contour of shmoo: (a)*Rx-A*, (b)*Rx-B: DFE off (Combined)*, (c)*Rx-B: DFE on (Combined)*, (d)*Rx-B: DFE off (D&C)*, and (e)*Rx-B: DFE on (D&C)*.

periodic operation can be evaluated efficiently using the proposed method. The proposed evaluation method achieves high accuracy, with shmoo similarity rates of over 95 %, while significantly reducing evaluation time, up to 23×.

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