A Cryo-CMOS Transmon Qubit Controller and Verification with FPGA Emulation

Kevin Tien[1], Ken Inoue[1], Scott Lekuch[1], David J. Frank[1], Sudipto Chakraborty[1], Pat Rosno[2], Thomas Fox[1], Mark Yeck[1], Joseph A. Glick[1], Raphael Robertazzi[1], Ray Richetta[2], John F. Bulzacchelli[1], Daniel Ramirez[2], Dereje Yilma[2], Andrew Davies[2], Rajiv V. Joshi[1], Devin Underwood[1], Dorothy Wisnieff[1], Chris Baks[1], Donald Bethune[3], John Timmerwilke[1], Blake R. Johnson[1], Brian P. Gaucher[1], Daniel J. Friedman[1]

[1]IBM T. J. Watson Research Center, Yorktown Heights NY, USA, [2]IBM Systems, Rochester MN, USA, [3]IBM Almaden Research Center, San Jose CA, USA

***Abstract*—Future generations of quantum computers are expected to operate in a paradigm where multi-qubit devices will predominantly perform circuits to support quantum error correction. Highly integrated cryogenic electronics are a key enabling technology to support the control of the large numbers of physical qubits that will be required in this fault-tolerant, error-corrected regime. Here, we describe our perspectives on cryoelectronics-driven qubit control architectures, and will then describe an implementation of a scalable, low-power, cryogenic qubit state controller that includes a domain-specific processor and a SSB upconversion I/Q-mixer-based RF AWG. We will also describe an FPGA-based emulation platform that is able to closely reproduce the system intention, and which was used to verify different aspects of the ASIC system design in *in situ* transmon qubit control experiments.**

Keywords—quantum computing, superconducting qubits, cryo-CMOS, FPGA emulation

I. Introduction

Recent advances in cryogenic electronics for quantum computing systems have demonstrated the viability of shifting key operations for qubit control from room temperature into the cryostat. These successful demonstrations of control waveform generation [1-4], components for cryogenic frequency/clock synthesis [5-6], and readout processing [3,6-8] allow one to envision the eventual deployment of quantum computers where significant processing is located close to the qubits themselves. Indeed, any deployment of the thousands of physical qubits that are required for meaningful noisy intermediate scale and robust fault tolerant quantum computing will inevitably hit challenging system-level integration roadblocks; one path to addressing such roadblocks is the mapping of electronics into the cryostat. Such a system re-partitioning promises overall increased system performance and yield through increasing local link bandwidths and signal integrity, decreasing thermal load from wiring to/from room temperature, and easing the assembly burden of the full quantum computer.

However, introducing an expanded role for cryogenic electronics places strong constraints on the power consumption of any implementation of the requisite control/readout operations of interest in any potential system partition. Especially for fault tolerant quantum computers, which will spend significant time executing syndrome circuits for quantum error correction [9], the power required per qubit under active control must be kept low so that the aggregate power consumption remains within the cooling budget of the cryostat. Though several proposals have been made for leveraging time-domain multiplexing [1-4] in order to amortize the cost of a single controller unit over many qubits, the need for sustained, simultaneous activity across those qubits stresses the performance requirements for multiplexed controllers while lowering the potential for amortization.

Additionally, a design methodology that minimizes the need for resource-intensive cooldown cycles for part validation is imperative for scaling the yield of the cryo-electronics in step with the qubit count. Such a methodology needs to encompass cryogenic-aware electrical design but also should include a pathway to fast turnaround validation of control algorithms in situ so as to maximally capture the subtleties of the quantum computing application.

As a feasibility demonstration of cryo-CMOS control, we have designed, implemented, and verified a superconducting qubit state controller in a 14 nm FinFET technology. The controller comprises a digital processing unit with instruction-level augmentations targeting qubit control driving an upconversion I/Q-mixer-based RF arbitrary waveform generator (AWG), realized largely with current-mode circuits. This highly flexible, low-power platform strikes a balance between enabling explorations of novel superconducting qubit-based circuits while fitting into a long-term roadmap for power scaling.

A major component of verification of the processing unit and its augmentations was the use of a hybrid field programmable gate array (FPGA) platform to exactly emulate the processor, proposed programs for qubit control, and a representative RF sub-system. This emulation platform enables fast iterations of logic changes and subsequent direct verification in a qubit control context. In this work, the emulation platform was key to verifying the completeness of the proposed digital architecture and software stack that would ultimately significantly shorten the bring-up cycle towards qubit control experiments by allowing software development to proceed in tandem with the ASIC design.

II. Qubit state controller architecture

A block diagram of the implemented state controller is shown in Figure 1. The controlling digital processor feeds two 10-bit current-mode DACs synchronously to synthesize a baseband waveform. After filtering, the baseband waveform is upconverted into a single sideband signal using an I/Q mixer. The I/Q mixer is loaded by a balun which implements both differential-to-single ended conversion and current gain; the balun's single-ended port is connected to the downstream 50 Ohm system.

The digital processor implements a custom instruction set architecture (ISA) with a general-purpose framework of

32-bit fixed point instructions together with dedicated instructions that streamline operations critical to waveform generation. The processor includes four memory banks: instruction memory, data memory, a separate waveform data memory, and a debug results memory; the latter memory enables interrogation of the results generated by the vector arithmetic engine. The memory banks are realized with SRAMs. To decrease the required power consumption given a target DAC sampling rate, the bulk of the processor operates on a synchronously divided clock domain. The waveform math is performed in a vector fashion and serialized as late as possible to minimize the amount of active digital circuitry operating at the DAC sampling rate.

III. Mixed Analog and Digital Emulation Platform

A. Overview

To verify the architectural choices made during the development of the ISA, a full emulation platform capable of controlling qubits was developed. There is significant value in being able to verify the qubit-control-specific applications in the context of real-world system requirements and thus gain learning that both informs the overall ISA design and accelerates chip bringup. A Xilinx Zynq UltraScale+ RFSoC FPGA [10] was selected as the FPGA emulation device because of its unique inclusion of both reprogrammable logic along with high speed digital-to-analog (RF-DAC) data converters. By using a hybrid FPGA, the implemented verification hardware was able to both emulate the ASIC design and be exercised at speed to control actual qubits well in advance of receiving the state controller in silicon.

B. Prototyping using FPGAs

FPGAs have often been used to emulate and prototype digital ASIC systems [11-12]. In a general FPGA-based digital prototyping flow, the pre-silicon ASIC-targeted logic implementation is mapped to the reprogrammable device and then run well before the ASIC itself is fabricated. This approach allows for early software development and significantly improves verification coverage of the design, as such a platform can typically run a much larger number of cycles than is practical in a software-based simulator. A major challenge in emulating an ASIC designed for quantum control arises from the constrained nature of the requisite analog waveform control. Inherent to the quantum system is that qubit behavior is very difficult to simulate, and the timing of the phase and amplitudes of the analog pulses produced needs to be very precise. This challenge effectively means that the emulation of only the digital portion of a microcontroller designed for qubit control would have limited practical benefit because it would be difficult to verify if the digital design would have the intended effect on a quantum system.

Moreover, such ASIC-to-FPGA mapping typically requires significant changes in low-level logic due to the fundamental differences in the available primitives for implementation. In particular, the emulation platform may need to run at reduced speed or implement a distinctly different clocking structure versus an ASIC, since many ASICs are designed with GHz operating frequencies and specialized clocking fabrics. As one example, consider an Ethernet controller which may be used as an I/O device for an emulated microcontroller platform. For this interface to be useful for general software development, the Ethernet line rates need to be compatible with existing network line speeds of ≥ 1 Gbps. However, if the emulated microcontroller unit logic can only run at 1/10th of the ASIC logic target speed due to limitations of the FPGA architecture, then the peripheral unit appears to be operating with an effective 10x speedup in the emulated system. As such, FPGA-based emulation systems often need to consider these rate differences and compensate for them by artificially adjusting the speed of the I/O peripherals to maintain an I/O rate to digital clock speed ratio consistent with that of the final design.

If one considers the qubit itself to be the 'peripheral' in this example, it is clear the requirement to maintain consistent ratios poses a significant challenge for emulation of quantum computing applications. All qubit control operations in a quantum system are dependent on the phase and amplitude of the microwave pulses produced by the control hardware, with the dependencies extending through all previous pulses, and additionally across all qubit control channels in the case of a multi-qubit experiment. If the emulation platform were to run at a slower speed than the fabricated ASIC, the software sequences that generate the waveform pulses would in fact occur at the incorrect times and cause the experiment to fail. Thus, the only practical way to support early quantum software development and control is to also emulate the *analog* drive portion of the ASIC such that it can be coupled to an actual qubit system. In our approach, this result was achieved by using the multiple DAC channels of the Xilinx RFSoC to produce real time analog signals consistent with the specifications of the ASIC, and thus also the requirements for qubit control.

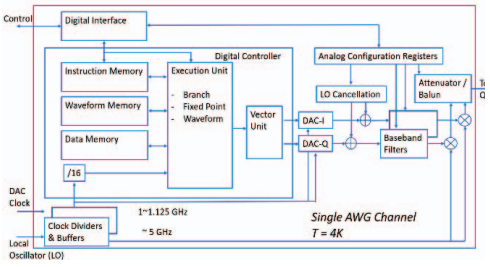

Figure 1. Block diagram of the implemented quantum state controller.

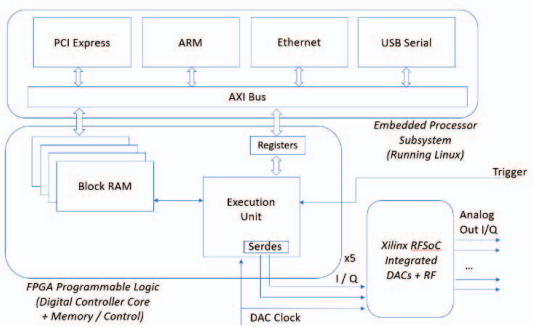

Figure 2. Block diagram of the FPGA emulator implementation.

C. Emulation platform implementation

Overall, the design choices for the state controller design made it uniquely aligned with attainable FPGA clock rates, and the mapping from the full ASIC-targeted register-transfer logic to the Xilinx Vivado flow was not only possible, but relatively straightforward. Significantly, the low operating frequency allowed for at-speed mapping to the FPGA with no significant timing adjustments. This mapping compatibility allowed for direct emulation of the synchronous vector arithmetic operation while maintaining the absolute system sampling rate for the DAC consistent with rates supported by ASIC design (here 1.125 GSPS). The number of bits per sample at the output of the DACs was also artificially limited to the same 10-bit resolution as implemented in the ASIC.

There are some significant differences in the analog signal chain downstream of the ASIC DACs as compared to the RFSoC DACs: primarily, the low-power state analog portion of the state controller was designed to operate in a cryogenic environment, relatively close to the qubit. The emulation system outputs need to reach the qubit from room temperature and experience significantly more attenuation as a result. In the implemented emulation platform, a much higher power was therefore required at the output of the system, and ad hoc adjustments were made to account for the increased losses in the signal path. Thus, the output amplitude incident at the qubit is not expected to be emulated to the same degree of accuracy as the timing/phase relationships in the emulated control path. There are other discrepancies as well; they are presented in Table I.

The small resource footprint of the digital processor also made the unit very portable relative to available FPGA resources. The highly power-optimized control logic is small enough that up to five instances of the processor can be instantiated on a single FPGA, with the memories for all supportable using only the FPGA's available internal block RAM. The design fitting comfortably with the FPGA resource constraints greatly simplifies the design and bring up of the emulation platform. Finally, with five control units included, multiple DAC output drive channels were required, with up to 8 channels of integrated DAC output available inside the signal FPGA package. These DAC units can run at up to 6 GSPS in the part selected for the emulation platform, which made it possible to in turn run the FPGA emulation platform at full speed with a core logic clock of roughly 70.3 MHz– exactly emulating the intended specifications of the implemented ASIC state controller.

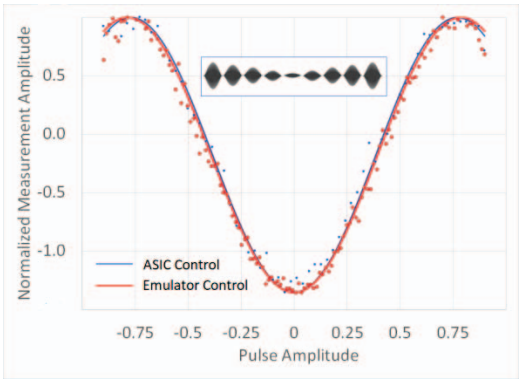

Figure 3. Rabi results generated using ASIC and emulator control.

Figure 2 illustrates the internal block diagram of the emulator, consisting of: 1) the FPGA programmable logic implementing 5 copies of the digital controller core, memory, and control logic; 2) Xilinx RFSoC-deployed integrated DACs and RF modules; and 3) an embedded ARM Cortex A5 processor subsystem running Linux, with support for software control over Ethernet and USB serial port.

IV. Emulation and ASIC Results

Both the emulation platform and the ASIC have been demonstrated successfully in qubit control scenarios. Basic Rabi measurements match very well, showing the expected sinusoidal oscillation of the measured qubit readout signal amplitude as a function of control pulse amplitude, as indicated in figure 3. The achieved power per qubit under active control for the cryo-CMOS control was 23 mW, which is competitive in the space of cryo-CMOS qubit controllers implementing arbitrary waveform generation. The emulation platform was of major importance in allowing for efficient and practical verification of the code used to actuate the microwave pulses implementing the Rabi experiment.

Because the emulation platform is capable of emulating multiple state controllers, it was moreover successfully used to calibrate a 5-qubit sample and run a full set of basic characterizations. This work was done in preparation for the execution of corresponding experiments with the ASIC, which are still pending. Fig. 4 shows the results of

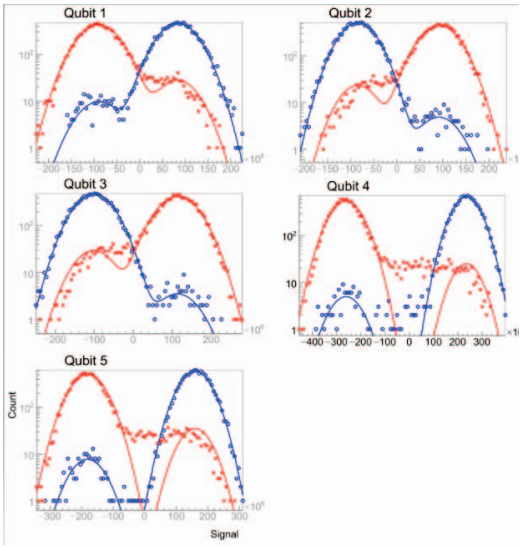

Figure 4. Results from basic characterization of 5 qubit sample completed using emulation platform.

Table I. Comparison of Quantum Control ASIC and FPGA

Platform	Microcontroller Logic Speed	DAC Attributes	Analog Mixer	Attenuation	LO Cancellation
Quantum Control ASIC	70.3 MHz	1.125 GSPS 10 bits I/Q Channels	Integrated	On-chip controllable by processor	Balanced in on-chip Mixer
FPGA Emulated ASIC	70.3 MHz	1.125 GSPS 16 bits (only 10 used) I/Q Channels to RF cables	External	Adjusted manually	External filter to remove LO

simultaneously running qubit readout test for ground (blue) and excited (red) states, achieving readout fidelities of 94.33% / 95.74% / 95.16% / 97.05% / 95.84%, respectively, for qubits 1 through 5. These results provide strong evidence that the processor functionality, the DAC resolution/sample rate, and the existing code stack will be sufficient for even multi-qubit experiments.

V. Conclusion

A low-power qubit state controller has been implemented and demonstrated in single-qubit control applications. An emulation platform based on the Xilinx Zynq UltraScale+ RFSoC FPGA was used to perform early validation of high-level specifications for the instruction set architecture of the controller processor and for the baseband DAC core. Future work includes demonstration of more complex multi-qubit control using both the ASIC platform and the emulation platform, as well as continued cryo-CMOS development towards decreasing power consumption.

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