Revisiting Pass-Transistor Logic Styles in a 12nm FinFET Technology Node

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***Abstract*—With the slow-down of Moore's law and the increasing requirements on energy efficiency, alternative logic styles compared to complementary static CMOS have to be revisited for digital circuit implementations. Pass Transistor Logic (PTL) gained much attention in the '90s, however, only a limited number of recent investigations and publications regarding PTL exist that use advanced technology nodes. This paper compares key performance metrics of 22 different PTL based 1-bit full adder designs to a complementary static CMOS logic reference, using a recent 12nm FinFET technology. The figures of merit are the propagation delay, the energy consumption, and the energy-delay-product (EDP). Our investigations show that PTL based adder circuits can have an up to 49% decreased delay and a 48% and 63% reduced energy consumption and EDP, respectively, compared to a state-of-the-art complementary CMOS logic reference. In addition, we analyzed the impact of PVT variations on the delay for selected PTL full adder designs.**

I. Introduction

In the late '90s, the authors of [1] presented a detailed comparison of different PTL styles with complementary CMOS logic. Only a few investigations regarding PTL logic styles exist that use advanced technology nodes e.g., [2]. However, [2] only focused on one special PTL technique and used predictive technology models for the FinFET devices. PTL is still used in state-of-the-art standard cell libraries, however, it is restricted to XOR/XNOR or multiplexer cells. The analysis of more complex PTL circuits is challenging since some PTL styles [1]–[7] show passive, and therefore resistive and capacitive coupled input-output paths. Moreover, some techniques imply voltage level degradation [4].

Recently, a design of an adder tree partially based on PTL to compute convolutional neuronal networks was presented in [8]. The authors reported an energy efficiency for the MAC operations of 97 TOPS/W at a supply voltage of 0.68V. They demonstrated, by simulation, energy efficiency improvements of 30% by interleaving 28T (complementary CMOS logic) and 14T (PTL) full adders in the adder tree, rather than using only the 28T complementary CMOS logic adders. Despite the challenges of PTL circuits, the results presented in [8] confirmed the potential of PTL and the need for detailed PTL investigations in advanced technology nodes. We focus here on the investigation of a 1-bit full adder cell in 22 different PTL implementations as this is a ubiquitous building block (cell) used for digital signal processing, such as multipliers, adders, and comparators. The propagation delay, energy consumption, and energy-delay-product (EDP) are the figures of merit used to analyze the different adder types. The major contributions of this work are

- the detailed investigations and reevaluation of PTL based 1-bit full adders using a recent 12nm FinFET technology,
- a comprehensive comparison to complementary CMOS logic 1-bit full adder cells (28T mirror adder),
- and an analysis of the PVT sensitivity for the most promising (w.r.t. EDP) six adders.

II. Experimental and Simulation Setup

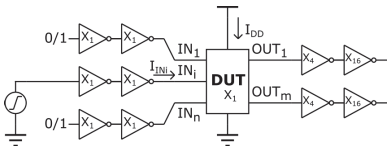

Fig. 1: Simulation setup

The simulation setup used to characterize and compare the different full adder circuits (DUT) is shown in Fig. 1. The inputs are driven by inverters to shape the DUT input signals. Its goal is to generate realistically shaped input signals to the DUTs inputs from the ideal square wave of the pulse source. In this setup, the slew of the ideal pulse source does not determine the input slew seen by the DUT. Instead, the input shapers driver strength (X1 in Fig. 1) defines the input slew. Loads of the DUT are modeled by inverters. The load inverter (X4) and its load (the load-on-load, X16) influence the effective capacitance seen by the DUT outputs. The effective parameters, i.e., the input slew and output capacitances, are calculated from SPICE simulation results, together with the figures of merit, defined as follows:

- Propagation delay:
  $D_{\{IN_i,OUT_j\}} = a_{\{OUT_j,50\%\}} - a_{\{IN_i,50\%\}}$,
  with $a_{\{u,\alpha\}} = t : u(t) = \alpha * V_{DD}$;
- Dynamic power:
  $P_{dyn} = \sum_{V_{INx}} (V_{INi} \cdot I_{INi}) + (V_{DD} \cdot I_{DD})$;
- Energy: $E = \int_{t=0}^{1ns} P_{dyn}$;
- Energy-delay-product: EDP $= E \cdot D$;

We also investigated the influence of different threshold voltages: low V_{th} (LVT) and super low V_{th} (SLVT) for the given 12nm FinFET technology node. Two different transistor sizings are considered: (1) logical effort sizing that is optimized for minimal delays and (2) minimal sizing, which uses for all transistors the minimal sizing (fins/fingers) allowed, therefore optimized for minimal energy consumption. In total, we analyzed 22 PTL based [1]–[8] 1-bit full adders and one state-of-the-art complementary CMOS full adder as reference circuit. Due to space restrictions, we can present only the results of the six most promising adders using SLVT devices, adders

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using LVT devices show the same trend. Further, we analyzed PVT variations while considering all input transitions yielding an output transition at the SUM or COUT signal (in total 56 transitions) for these adder designs (resulting in 48000 SPICE simulations):

- VDD var.: -10% to +10% of nominal 0.8V in 5% steps
- Temperature variation: 0°C to 100°C in 25°C steps.
- Process (P N): SS, SF, TT, FS, FF (S-slow, F-fast, T-typ.).

III. Results and Analysis

DUT	E [aJ] (%)	D(SUM) [ps] (%)	D(COUT) [ps] (%)	EDP(COUT) [fJ·ps] (%)
Mirror 28T	1189 (0.0)	9.81 (0.0)	6.22 (0.00)	7.39 (0.00)
CHIH21 14T [8]	836 (-29.7)	6.21 (-29.5)	4.26 (-31.4)	3.56 (-45.9)
NASERI 20T [7]	846 (-28.9)	6.32 (-28.3)	3.18 (-48.8)	2.69 (-63.6)
NASERI 22T [7]	973 (-21.2)	5.27 (-40.2)	3.14 (-49.5)	2.94 (-60.2)
BUI02 A9 [4]	638 (-46.3)	7.57 (-14.1)	9.65 (+55.2)	6.15 (-16.7)
BUI02 SERF [4]	616 (-48.2)	6.21 (-29.6)	9.15 (+47.2)	5.64 (-23.7)

TABLE I: Summary of 6 adder types - logical effort sized (1)

DUT	E [aJ] (%)	D(SUM) [ps] (%)	D(COUT) [ps] (%)	EDP(COUT) [fJ·ps] (%)
Mirror 28T	893 (0.0)	9.81 (0.0)	7.49 (0.00)	6.69 (0.00)
CHIH21 14T [8]	727 (-18.6)	7.27 (-25.9)	4.98 (-33.5)	3.62 (-45.9)
NASERI 20T [7]	683 (-23.5)	6.75 (-31.2)	4.53 (-39.5)	3.09 (-53.8)
NASERI 22T [7]	754 (-15.6)	5.62 (-42.7)	4.24 (-43.4)	3.20 (-52.2)
BUI02 A9 [4]	581 (-34.9)	9.93 (+ 1.2)	13.36 (+78.3)	7.76 (+16.0)
BUI02 SERF [4]	568 (-36.4)	8.09 (-17.5)	12.85 (+71.5)	7.30 (+ 9.1)

TABLE II: Summary of 6 adder types - minimal sized (2)

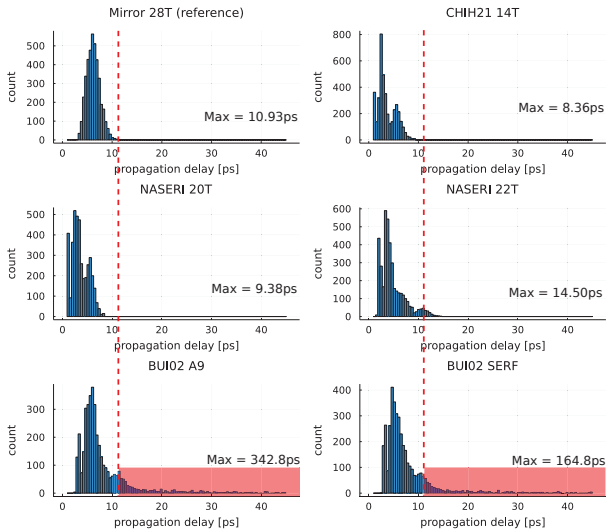

Fig. 2: PVT delay distributions of the COUT path delay, considering all possible input changes yielding a COUT change

Tables I and II summarize the performance characteristics of the six selected adder types at nominal PVT (TT (typical), 0.8V, 25°C). It should be noted that the energy and delay values are averaged across all input transitions. The average COUT delay is used for the EDP calculation since it is often part of the critical path of larger blocks.

The analysis of all 23 adder types, including the CMOS 28T mirror adder, shows that BUI02 [4] adders exhibit the lowest energy independent of sizing and V_{th}. However, the delay of BUI02 adders has a high dependency on V_{th} due to voltage level degradation. The NASERI18 family [7] shows the lowest EDP independent of sizing and V_{th}. In Fig. 2 we plot the results of the exhaustive PVT analysis. It reveals that only the BUI02 adders have a very large tail in their delay distribution, highly exceeding the timing of the 28T mirror reference adder (red dashed line). This is also due to voltage level degradation. A deeper analysis of the PVT data shows that only specific input transitions, "R10", "1R0", "R1R", and "1RR" (Inputs: "A/B/CIN" - R=Rising edge, 0/1=stable 0 or 1), contribute to the large tail of the BUI02 SERF adder [4]. The BUI02 A9 adder has an additional transition "RRR" that impacts the tail distribution. We also analyzed the input capacitance variation of the six adder types with respect to the output load (X1, X4, X8). Table III shows the corresponding results normalized to an X1 inverter. The input capacitance heavily depends on the input transition. As expected, the CIN input capacitance of the mirror adder has a negligible low dependency on the output load. However, for the BUI02 A9 adder we see a variation of up to 80% (load X8) due to resistive and capacitive coupled input-output paths. This large variation in the input capacitance makes the timing analysis of PTL based circuits very challenging.

DUT	Load X1 Inv. avg. (min / max)	Load X4 Inv. avg. (min / max)	Load X8 Inv. avg. (min / max)
Mirror 28T	1.46 (-5.7%/10.0%)	1.46 (-5.7%/10.0%)	1.46(-5.7%/10.0%)
CHIH21 14T [8]	1.99 (-17.6%/18.6%)	2.65 (-22.7%/24.6%)	3.10 (-26.5%/29.8%)
NASERI 20T [7]	2.62 (-28.7%/29.7%)	3.84 (-39.0%/41.7%)	5.02 (-48.0%/53.6%)
NASERI 22T [7]	3.12 (-19.6%/17.9%)	4.37 (-31.1%/30.6%)	5.66 (-41.8%/43.1%)
BUI02 A9 [4]	1.07 (-36.9%/53.4%)	1.19 (-41.3%/72.9%)	1.25 (-43.5%/80.8%)
BUI02 SERF [4]	1.28 (-44.5%/37.2%)	1.59 (-54.8%/57.1%)	1.77 (-59.3%/69.4%)

TABLE III: CIN input capacitance variation, normalized to the C_{in} of a X1 inverter - logical effort sized (1)

We presented here the most relevant results of our analysis and showed that PTL based adder circuits have an up to 49% decreased delay and a 48% and 63% reduced energy consumption and EDP, respectively, compared to the complementary CMOS logic reference (28T mirror adder). In addition, we analyzed the impact of PVT variations on the delay. While the BUI02 SERF and A9 adders show the lowest energy consumption, they exhibit a very large tail in the delay distribution and a high input capacitance variation. Only specific transitions contribute to this tail. These characteristics have to be considered when integrating such PTL styles into current circuit designs.

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