DATE 2022 Technical Programme Topic Chairs

D1 System Specification and Modeling

Chair: Gianluca Palermo, Politecnico di Milano, IT

Co-Chair: Julio Medina, University of Cantabria, ES

D2 System-Level Design Methodologies and High-Level Synthesis

Chair: Philippe Coussy, Universite de Bretagne-Sud / Lab-STICC, FR Co-Chair: Christian Pilato, Politecnico

di Milano, IT

D3 System Simulation and Validation

Chair: Katell Morin-Allory, TIMA Laboratory, FR

Co-Chair: Monica Farkash, AMD, US **DT4 Design and Test for Analog and Mixed-Signal Circuits and Systems, and MEMS**

Chair: Rosa Rodríguez-Montañés, UPC, ES

Co-Chair: Helmut Graeb, Technical University of Munich, DE

DT5 Design and Test of Hardware Security Primitives

Chair: Nele Mentens, KU Leuven, BE Co-Chair: Kazuo Sakiyama, The University of Electro-Communications, JP DT6 Design and Test of Secure Sys-

tems

Chair: Francesco Regazzoni, University of Amsterdam and ALaRI - USI, CH

Co-Chair: Ricardo Chaves, INESC-ID, IST, Universidade de Lisboa, PT

D7 Formal Methods and Verification

Chair: Anna Slobodova, Centaur Technology, US

Co-Chair: Yakir Vizel, The Technion, IL

D8 Network-on-Chip and On-Chip Communication

Chair: Romain Lemaire, CEA-Leti, FR Co-Chair: Li-Shiuan Peh, Professor, National University of Singapore, SG D9 Architectural and Microarchitec-

tural Design

Chair: Olivier Sentieys, INRIA, FR **Co-Chair**: Jeronimo Castrillon, TU Dresden, DE

D10 Low-power, Energy-efficient and Thermal-aware Design

Chair: Pascal Vivet, CEA-Leti, FR Co-Chair: Masanori Hashimoto, Kyoto University, JP

D11 Approximate Computing

Chair: Lukas Sekanina, Brno University of Technology, CZ

Co-Chair: Jie Han, University of Alberta, CA

D12 Reconfigurable Systems

Chair: Suhaib A. Fahmy, KAUST, SA Co-Chair: Michaela Blott, Xilinx, IE D13 Logical and Physical Analysis

and Design

Chair: L. Miguel Silveira, INESC ID/IST - Lisbon University, PT Co-Chair: Mathias Soeken, Microsoft, CH

D14 Emerging Design Technologies for Future Computing

Chair: Elena Gnani, University of Bologna, IT

Co-Chair: Gage Hills, Massachusetts Institute of Technology, US

D15 Emerging Design Technologies for Future Memories

Chair: Shahar Kvatinsky, Technion, IL **Co-Chair**: Damien Querlioz, Univ Paris-Sud, FR

A1 Power-efficient and Sustainable Computing

Chair: Andreas Burg, EPFL-TCL, CH **Co-Chair**: Jungwook Choi, Hanyang University, KR

A2 Smart Cities, Internet of Everything, Industry 4.0

Chair: Saraju Mohanty, University of North Texas, US

Co-Chair: Fabrizio Lamberti, Politecnico di Torino, IT

A3 Automotive Systems and Smart Energy Systems

Chair: Selma Saidi, Technische Universität Dortmund, DE

Co-Chair: Michele Magno, ETH Zürich, CH

A4 Augmented Living and Personalized Healthcare

Chair: Marina Zapater, University of Applied Sciences Western Switzerland (HES-SO), CH

Co-Chair: Elisabetta Farella, Fondazione Bruno Kessler (FBK), IT

A5 Secure Systems, Circuits, and Architectures

Chair: Pascal Benoit, University of Montpellier, FR

Co-Chair: Bertrand Cambou, Northern Arizona University, US

A6 Self-adaptive and Context-aware Systems

Chair: Geoff Merrett, University of Southampton, GB Co-Chair: Andy Pimentel, University of Amsterdam, NL

A7 Applications of Emerging Technologies

Chair: Michael Niemier, University of Notre Dame, US

Co-Chair: Bastien Giraud, CEA LETI, FR

A8 Industrial Experiences Brief Papers

Chair: Christian Weis, University of Kaiserslautern, DE

Co-Chair: Nicolas Ventroux, CEA, LIST, FR

T1 Modeling and Mitigation of Defects, Faults, Variability, and Reliability

Chair: Arnaud Virazel, LIRMM, FR Co-Chair: Bram Kruseman, NXP Semiconductors, NL

T2 Test Generation, Test Architectures, Design for Test, and Diagnosis

Chair: Maria K. Michael, Electrical and Computer Engineering & KIOS Center of Excellence, University of Cyprus, CY

Co-Chair: Grzegorz Mrugalski, Mentor Graphics, PL

T3 Dependability and System-Level Test

Chair: Karthik Pattabiraman, University of British Columbia, CA Co-Chair: Stefano Di Carlo, Politecnico di Torino, IT

DT4 Design and Test for Analog and Mixed-Signal Circuits and Systems, and MEMS

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Co-Chair: Ricardo Chaves, INESC-ID, IST, Universidade de Lisboa, PT

E1 Embedded Software Architecture, Compilers and Tool Chains

Chair: Sara Vinco, Politecnico di Torino, IT

Co-Chair: Sudipta Chattopadhyay, Singapore University of Technology and Design (SUTD), SG

E2 Real-time, dependable and privacy-enhanced systems

Chair: Marko Bertogna, University of Modena, IT

Co-Chair: Mitra Nasri, Eindhoven University of Technology, NL

E3 Machine Learning Solutions for Embedded and Cyber-Physical Systems

Chair: Luca Carloni, Columbia University, US

Co-Chair: Mario R. Casu, Politecnico di Torino, Department of Electronics and Telecommunications, IT

E4 Design Methodologies for Machine Learning Architectures

Chair: Tushar Krishna, Georgia Institute of Technology, US Co-Chair: Marian Verhelst, KU Leu-

ven, BE E5 Design modeling and verification

for embedded and cyber-physical systems

Chair: Davide Quaglia, University of Verona, IT

Co-Chair: Mohammad Al Faruque, University of California Irvine, US