DATE PhD Forum 2022

Date: Wednesday, 16 March 2022
Time: 18:30 - 20:30 CET

Session chair:

Gabriela Nicolescu, École Polytechnique de Montréal, CA

The PhD Forum is an online poster session hosted by EDAA, ACM-SIGDA, and IEEE CEDA for PhD students who have completed their PhD thesis within the last 12 months or who are close to complete their thesis work. It represents an excellent opportunity for them to get feedback on their research and for the industry to get a glance of state-of-the-art in system design and design automation.

Admitted Presentations

NOVEL ATTACK AND DEFENSE STRATEGIES FOR ENHANCED LOGIC LOCKING SECURITY
Lilas Alrahis, New York University Abu Dhabi, AE

PROPER ABSTRACTIONS FOR DIGITAL ELECTRONIC CIRCUITS: A PHYSICALLY GUIDED APPROACH
Jurgen Maier, TU Wien, AT

RETRAINING-FREE WEIGHT-SHARING FOR CNN COMPRESSION
Etienne Dupuis, Lyon Institute of Nanotechnology, FR

INTELLIGENT CIRCUIT DESIGN AND IMPLEMENTATION WITH MACHINE LEARNING IN EDA
Zhiyao Xie, Duke University, US

CROSS-LAYER TECHNIQUES FOR ENERGY-EFFICIENCY AND RESILIENCY OF ADVANCED MACHINE LEARNING ARCHITECTURES
Alberto Marchisio, TU Wien, AT

DESIGN & ANALYSIS OF AN ON-CHIP PROCESSOR FOR THE AUTISM SPECTRUM DISORDER (ASD) CHILDREN ASSISTANCE USING THEIR EMOTIONS
Abdul Rehman Aslam, Lahore University of Management Sciences, PK

RESILIENCE AND ENERGY-EFFICIENCY FOR DEEP LEARNING AND SPIKING NEURAL NETWORKS FOR EMBEDDED SYSTEMS
Rachmad Vidya Wicaksana Putra, TU Wien, AT

MODELING AND OPTIMIZATION OF EMERGING AI ACCELERATORS UNDER RANDOM UNCERTAINTIES
Sanmitra Banerjee, Duke University, US

LOGIC SYNTHESIS IN THE MACHINE LEARNING ERA: IMPROVING CORRELATION AND HEURISTICS
Walter Lau Neto, University of Utah, US

ACCELERATING CNN INFERENCE NEAR TO THE MEMORY BY EXPLOITING PARALLELISM, SPARSITY, AND REDUNDANCY
Palash Das, Indian Institute of Technology, Guwahati, IN

DESIGN AUTOMATION FOR ADVANCED MICROFLUIDIC BIOCHIPS
Debraj Kundu, IITR, IN

ULTRA-FAST TEMPERATURE ESTIMATION METHODS FOR ARCHITECTURE-LEVEL THERMAL MODELING
Hameedah Sultan, Indian Institute of Technology Delhi, IN

MULTI-OBJECTIVE DIGITAL VLSI DESIGN OPTIMISATION
Linan Cao, University of York, GB

TINYDL: EFFICIENT DESIGN OF SCALABLE DEEP NEURAL NETWORKS FOR RESOURCE-CONSTRAINED EDGE DEVICES
Mohammad Loni, Mälardalen University, SE

DECISION DIAGRAMS IN QUANTUM DESIGN AUTOMATION
Stefan Hillmich, Johannes Kepler University Linz, AT

DEPENDABLE RECONFIGURABLE SCAN NETWORKS
Natalia Lylina, University of Stuttgart, DE

BREAKING THE ENERGY CAGE OF INSECT-SCALE AUTONOMOUS DRONES: INTERPLAY OF PROBABILISTIC HARDWARE AND CO-DESIGNED ALGORITHMS
Priyesh Shukla, University of Illinois at Chicago, US

RESILIENT: PROTECTING DESIGN IP FROM MALICIOUS ENTITIES
Nimisha Limaye, New Yor University, US

ALGORITHM-ARCHITECTURE CO-DESIGN FOR ENERGY-EFFICIENT, ROBUST, AND PRIVACY-PRESERVING MACHINE LEARNING
Souvik Kundu, USC, US

PERFORMANCE-AWARE DESIGN-SPACE OPTIMIZATION AND ATTACK MITIGATION FOR EMERGING HETEROGENEOUS ARCHITECTURES
Mitali Sinha, IIIT Delhi, IN

PRACTICAL SIDE-CHANNEL AND FAULT ATTACKS ON LATTICE-BASED CRYPTOGRAPHY
Prasanna Ravi, Nanyang Technological University, SG

MEMORY INTERFERENCE AND MITIGATIONS IN RECONFIGURABLE HESOCS FOR EMBEDDED AI
Gialuca Brilli, University of Modena and Reggio Emilia, IT