Quantum computing with CMOS technology

M. Fernando Gonzalez-Zalba
Qunatum Motion Technologies
Harrogate, UK
fernando@quantummotion.tech

***Abstract*— Quantum computing is poised to be the innovation driver of the next decade. Its information processing capabilities will radically accelerate drug discovery, improve online security, or even boost artificial intelligence [1]. Building a quantum computer promises to have a major positive impact in society, however building the hardware that will enable that paradigm change its one of the greatest technological challenges for humanity.**

The spins of isolated electrons in silicon are one of the most promising solid-state systems to achieve that goal. With the recent demonstrations of long coherence times [2], high-fidelity spin readout [3], and one- and two-qubit gates [4-7], the basic requirements to build a fault-tolerant quantum computer have now been fulfilled. These are promising initial results for this relatively recent approach to quantum computing, indicating that attempting to build a quantum computer based on silicon technology is a realistic proposition.

However, many technological challenges lie ahead. So far, most of the aforementioned milestones were achieved with small-scale devices (one- or two-qubit systems) fabricated in academic cleanrooms offering a relatively modest level of process control and reproducibility. Now, a transition from lab-based demonstrations to spin qubits manufactured at scale is necessary. Recently, important developments in the field of nanodevice engineering have shown this may be possible by using modified field-effect transistors (FET) [8,9], thus creating an opportunity to leverage the scaling capabilities of the complementary metal-oxide-semiconductor (CMOS) industry to address the challenge. From a technological perspective, CMOS-based quantum computing brings compatibility with well-established, highly reproducible Very Large-Scale Integration (VLSI) techniques of the CMOS industry that routinely manufacture billions of quasi-identical transistors on the size of a fingertip. Furthermore, using CMOS technology for quantum computing could enable hybrid integration of quantum and classical technologies facilitating data management and fast information feedback between processing blocks.

In this paper, I will present a series of results on silicon FETs manufactured in an industrial environment that show this technology could provide a platform on to which implement electron spin qubits at scale. I will present our efforts to develop a qubit specific measurement technique that is accurate and scalable while being compatible with the industrial fabrication processes [10-12]. Using this methodology, I will show the first report of electron spin readout in a silicon industry-fabricated device [13]. On the architecture side, I will present results that combine, on chip, digital and quantum devices to perform time-multiplexed readout [14]. And finally, I will show our strategy to use small CMOS quantum processing units in a multi-core approach to solve hybrid quantum-classical algorithms that benefit from massive parallelisation [15,16].

Keywords—silicon, transistors, spins, quantum computing, CMOS, VLSI.

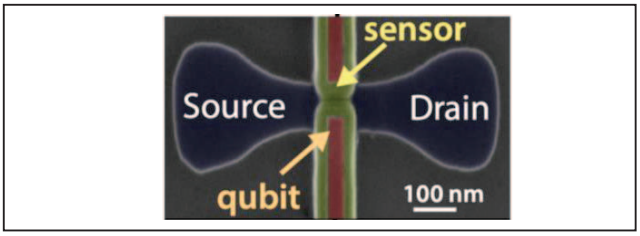

Fig. 1. False-colour transmission electron micrograph of a silicon nanowire transistor with a pair of split gates. Quantum dots are formed under each gate, referred to as “sensor" and “qubit" dots. Manufactured at CEA-Leti.

ACKNOWLEDGMENT

This research has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreements No. 951852 and 688539.

REFERENCES

[1] Montanaro, A. et al. “Quantum algorithms: an overview”. Npj Quantum Inf. 2, 15023 (2016).

[2] Veldhorst, M. et al. “An addresable quantum dot qubit with fault-tolerant control fidelity”. Nat. Nanotech. 9, 981-985 (2014).

[3] Morello, A. et al. “Single-shot readout of an electron spin in silicon”. Nature 467, 687{691 (2010).

[4] Yoneda, J. et al. “A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%.” Nat Nanotech 13, 102-106 (2018).

[5] Veldhorst, M. et al. “A two-qubit logic gate in silicon”. Nature 526, 410-414 (2015).

[6] Zajac, D. M. et al. “Resonantly driven cnot gate for electron spins”. Science 359, 439-442 (2018).

[7] Watson, T. F. et al. “A programmable two-qubit quantum processor in silicon”. Nature 555, 633-637 (2018)

[8] Maurand, R. et al. “A CMOS silicon spin qubit”. Nat Commun 7, 13575 (2016).

[9] Hutin, L. et al. “Gate reflectometry for probing charge and spin states in linear si mos split-gate arrays”. In 2019 IEEE International Electron Devices Meeting (IEDM), 37.7.1-37.7.4 (2019).

[10] Gonzalez-Zalba, M. F., Barraud, S., Ferguson, A. J. & Betz, A. C. “Probing the limits of gate-based charge sensing”. Nat Commun 6, 6084 (2015).

[11] Lundberg, T. “Spin quintet in a silicon double quantum dot: Spin blockade and relaxation” Phys Rev X 10 041010 (2020)

[12] Ibberson, D. J. et al. “Large dispersive interaction between a CMOS double quantum dot and microwave photons” (2020). arxiv2004.00334.

[13] Ciriano-Tejel, V. N. et al. “Spin readout of a cmos quantum dot by gate reflectometry and spin-dependent tunnelling” (2020). arxiv2005.07764.

[14] Schaal, S. et al. “A CMOS dynamic random access architecture for radio-frequency readout of quantum devices”. Nat Elect 2, 236{242 (2019).

[15] Cai, Z. “Resource Estimation for Quantum Variational Simulations of the Hubbard Model”. Phys Rev App 14, 014059 (2020).

[16] Peruzzo, A. et al. “A variational eigenvalue solver on a photonic quantum processor”. Nat Commun 5, 4213 (2014)