TRIGON: A Single-phase-clocking Low Power Hardened Flip-Flop with Tolerance to Double-Node-Upset for Harsh Environments Applications

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***Abstract*—Single Event Upset (SEU) is one of the most susceptible reliability issues for CMOS circuits in a harsh environment, such as space or even a sea-level environment. Especially in the advanced nanoscale node, the phenomenon of Multi-node-upset (MNU) becomes more prominent. Although a lot of work has been proposed to solve this problem, most of them ignored the need for low power consumption. Particularly, most existing solutions are not effective anymore when operating in low supply voltage. Therefore, this paper proposes a novel Flip-Flop called TRIGON based on a single-phase-clocking structure to achieve low power consumption while being able to tolerate Double-node-upset (DNU), even when operating at lower supply voltages. The experimental results show that TRIGON has a significant reduction in the area and Power-delay-area-product (PDAP). Particularly, it achieves about 80% energy saving on average when the input is static compared with the state-of-the-art circuits.**

Keywords—single event upset, low power, single-phase-clocking, radiation hardening by design, Flip-Flop

I. Introduction

Soft errors are one of the most important reliability issues encountered by electronic systems in harsh environments, such as space or even terrestrial environments. It is mainly caused by a serious of radiation effects, of which the Single Event Effect (SEE) is the biggest and most noteworthy. It refers to the process of energy deposition, generation of electron-hole pairs, which are collected by the sensitive nodes of the circuits, and eventually produce abnormal transients when a single high-energy particle hit happens. Typically, this kind of abnormal transient is called Single Event Upset (SEU). For the μm-level process, the most vulnerable circuit-sequential elements, such as Flip-Flop (FF) and SRAM, will only produce Single-node-upset (SNU) when hit happens. Therefore, traditional hardening methods such as the Triple Redundancy Module (TMR) and DICE [1] structure can well solve this SNU issue. However, for advanced nanoscale technology nodes, as a result of the continuing decrease of the device spacing, supply voltage, critical charge, and parasitic capacitance, the Double-node-upset (DNU) will replace SNU as the most urgent issue to be solved [2]. It can be clearly seen from Fig. 1 that during the holding phase of the latch, if two neighboring sensitive nodes collect electron-hole pairs generated by the particles at the same time, two abnormal transients will be generated, finally causing the latch to occur the flip.

In order to solve this DNU issue, many works have been proposed recently [3][4][5][6]. The salient feature of [3][4]is the redundant design based on the DICE structure to tolerate

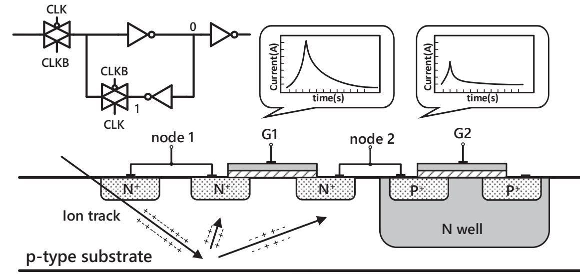

Fig. 1. Double-node-upset happens when the particles hit.

DNU. Similarly, [5] was also based on a similar redundancy idea to process the C-element. One big disadvantage brought by these redundant designs is the large area overhead. Therefore, [6] proposed a coupled Schmitt trigger design and introduced high-threshold transistors to minimize the area cost. However, although these techniques have excellent soft error tolerance capacity according to their experimental results, one important feature has been ignored in the harsh environment, that is, the limited energy supply, so there is a great demand for low power consumption of the circuits. Of course, one point that should be admitted is that [5][6] optimize power consumption to a certain extent, but they are only limited to the simple clock gating technology, which cannot play a big role in reducing power consumption. Moreover, it should be noted that the soft error tolerance features of these most existing methods fail when operating at lower supply voltages, which is a common requirement in low power applications.

Single-phase-clocking technology has received great attention and is considered to be a promising low-power technology [7][8][9] since it eliminates the local clock buffer and thus can lower dynamic power dissipation significantly. ACFF [7], as a classic single-phase clock Flip-Flop structure, only contains 22 transistors and can even save 77% of power consumption compared with conventional transmission-gate based FF (TGFF). The most obvious feature of ACFF is that it is a differential *leader-follower* [1] type with two adaptive-coupling elements, which allow it to be less susceptible to process variation. Given that it has such low power dissipation, several papers have proposed improved radiation-hardened ACFFs [10][11]. However, these improved ones both employed a special FDSOI process to tolerate soft errors. Obviously, this will cause a large increase in process costs, which is unacceptable to some extent.

In order to solve the problems of DNU and low power consumption, while minimizing the cost overhead, this paper proposes low-power radiation-hardened FF based on the ACFF differential structure, named TRIGON. Since this is a leader-follower structure, we have proposed different

[1] This type of flip-flop is usually known by a different name in the community, which the authors refrain from using that term due to its cultural inappropriateness.

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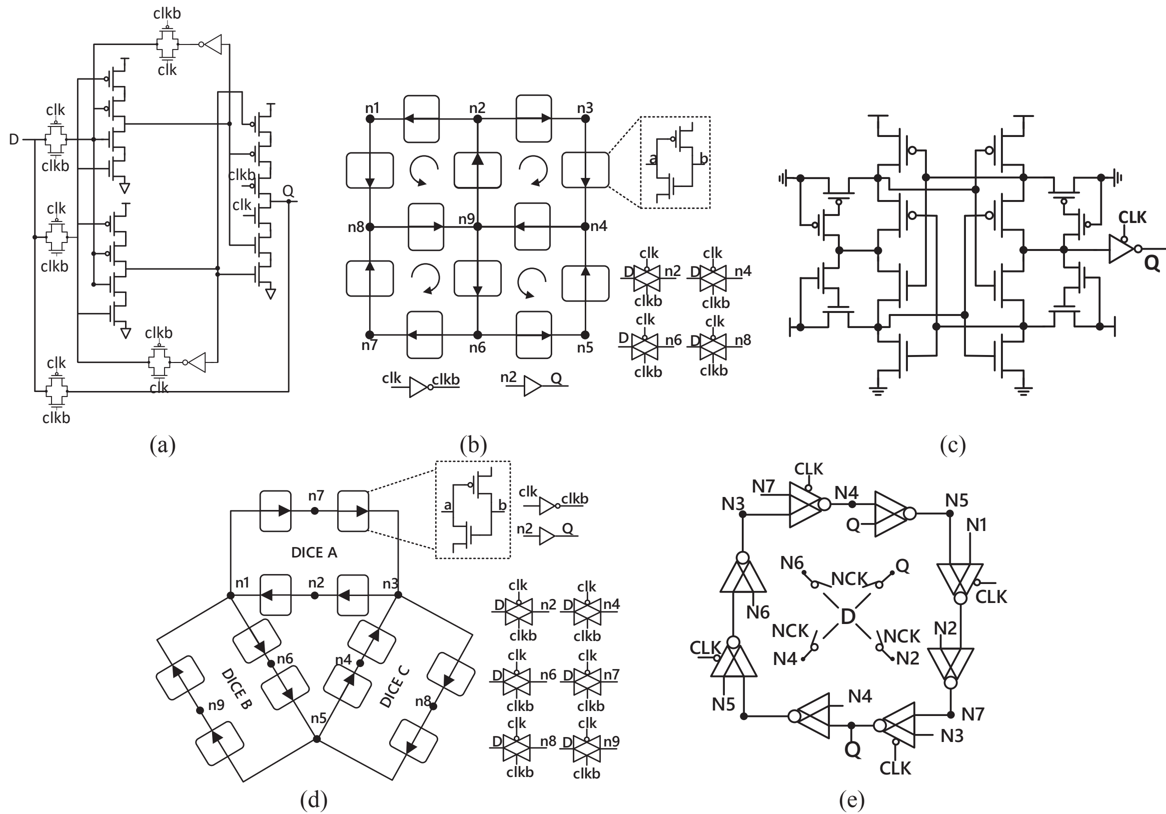


Fig. 2. Previously proposed SNU and DNU tolerant circuits. (a) HPST [12]. (b) DONUT [3]. (c) CROUT [6]. (d) Delta-DICE [4]. (e) DNURHL [5].

hardening methods in both leader and follower latches. In the leader latch, an improved coupled Schmitt trigger was introduced, and in the follower latch, a novel feedback cut-off structure was proposed, respectively. The experimental results show that TRIGON achieves 80% energy saving when the input is static compared with reference works and its power-delay-area-product (PDAP) has a 56% reduction on average under the standard supply voltage 1.1V for the 40nm CMOS process. It addition, TRIGON can reliably work down to 0.7V with DNU tolerance, unlike most other existing solutions. These results are promising for providing an alternative low-power design applied in harsh environments.

The remaining part of the paper proceeds as follows: some previous work will be introduced in Section II, which will be followed by the proposed TRIGON in Section III. It will then go on the experimental results in Section IV and the conclusion in Section V.

II. Previous Work

In this section, we will first present and discuss several recently proposed soft error tolerant sequential circuits. Firstly, the SNU tolerant circuit will be presented in Sec. II. A, which will be followed by the normal DNU tolerant circuits in Sec. II. B. Finally, in Sec. II. C, two low-power hardened circuits will be analyzed.

A. Single-node-upset tolerant circuit

Traditionally, the most classic structure used to tolerate SNU is the DICE [1] structure, which contains two pairs of redundant nodes. If one node in this pair flips erroneously, the other node of this pair will correct it to its original state. In addition, many other structures have also been proposed. HPST [12] was one of them. As can be seen in Fig.2 (a), it performs dual-mode redundancy processing on the basis of the C-element, thereby ensuring that if any of the redundant nodes are flipped, the filtering function of the C-element can be used to output the original correct state. It achieved high performance validated by the experimental results, especially the Power-Delay-Product (PDP). However, it should be noted that if both inputs of the C-element are flipped, the filtering function of the C-element will fail, and the output will be flipped accordingly and becomes unrecoverable.

B. Double-node-upset tolerant circuit

As mentioned before, DICE is a commonly employed method to tolerate soft error. Based on the DICE structure, a lot of work has been proposed to solve the DNU issue [3][4]. As shown in Fig. 2 (b) and (d), the basic idea of these designs is to use DICE to carry out redundant structures to realize an interlocked scheme, so that the redundant nodes in each DICE cell can be enough to tolerate DNU happening in this structure. However, the major shortcoming is significant power and area overhead due to the large number of transistors brought by the redundant structures.

Therefore, how to minimize the overhead, such as power and area overhead, under the premise of ensuring the ability of DNU tolerance, is the direction that has been explored in recent years.

C. Low-power Double-node-upset tolerant circuit

Traditional methods to reduce power consumption usually include clock gating technology. It can reduce the dynamic

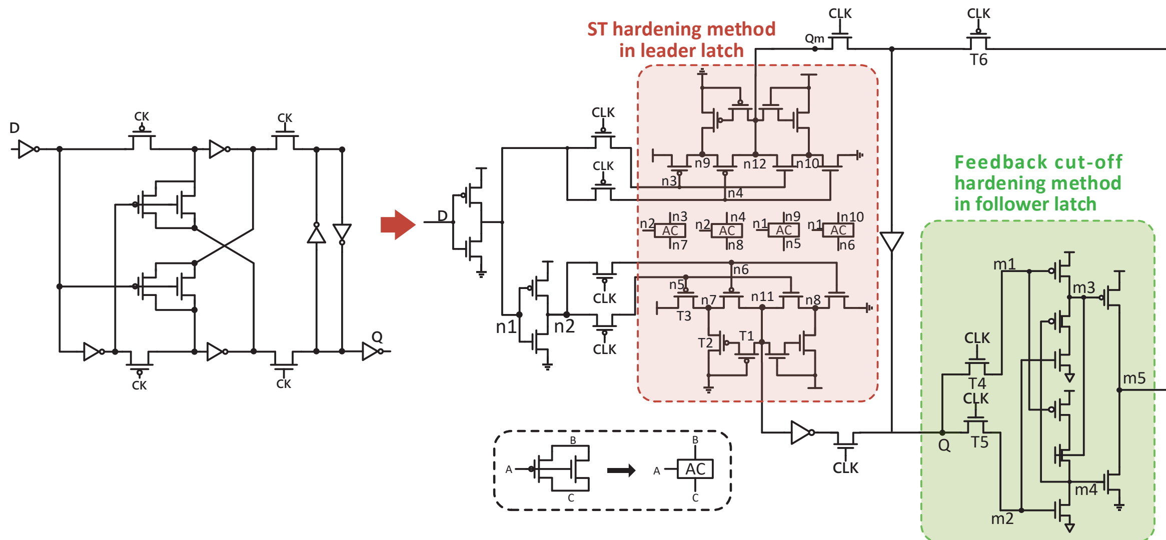


Fig. 3. Shown on the left is the ACFF circuit [7]. Based on this circuit, we proposed low-power hardened TRIGON FF shown on the right.

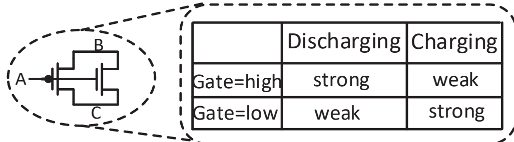
power consumption in the circuit through the clock signal. It can be seen from Fig. 2. (c) and (e), both used this technology. Especially in [6], it integrates the clocking gating with C-element, thus forming feedback to ensure any node can be recovered when the hit happens.

It is not difficult to find that all the above circuits are based on the dual-phase clock, which means the power dissipation of the local clock buffer is included in the total energy consumption. Therefore, if a single-phase clocking structure is used, then this consumption can be totally eliminated.

III. TRIGON

In this section, we will describe the proposed low-power hardened Flip-Flop, TRIGON. This FF adopts the leader-follower composition form. Considering that different hardening methods are employed in both leader latch and follower latch. We will introduce these two hardening methods separately, leader latch in Sec. III. A and follower latch in Sec. III. B.

First of all, note that TRIGON evolves from the ACFF [7] structure. Therefore, let us start with the ACFF operational principle. As can be seen on the left in Fig. 3, ACFF is a differential leader-follower topology evolving from the transmission-gate based FF, also featuring the single-phase clock. Moreover, in order to overcome the shortcoming of state-retention caused by the weak transmission capability of the PMOS transmission gate in the leader latch, two adaptive-coupling (AC) circuits are added, as shown in Fig. 4. If the input state of the AC element is different from the internal state, then the ability of state-retention will be weakened. For the NMOS transmission gate in the follower latch, its transmission capacity is stronger than PMOS, so there is no need to add the AC element to enhance state transition.



	Discharging	Charging
Gate=high	strong	weak
Gate=low	weak	strong

Fig. 4. Adaptive coupling scheme [7].

A. Hardening Method in Leader Latch

As mentioned before, like ACFF, TRIGON is also a differential topology, especially in the leader latch. The hardened circuit–CROUT based on the Schmitt trigger coupling structure was proposed in [6] (shown in Fig. 2(c)). It also conforms to the characteristics of the differential topology. Therefore, we embed CROUT [6] into ACFF's leader latch and make improvements to make it more suitable for ACFF.

As can be seen from Fig. 3, in the process of incorporating CROUT to ACFF, we added two additional PMOS transmission gates and two AC elements. Essentially, CROUT is equivalent to two inverters with double-ended input and a double-ended output coupled with each other. Therefore, the number of PMOS transmission gates and AC elements in ACFF needs to be doubled in the leader latch of the proposed TRIGON FF. In this way, in the leader latch, while DNU can be tolerated, state retention can also be weakened to ensure an easier transition.

In the leader latch, there are a total of 6 sensitive nodes, namely n7~n12. When holding different states, sensitive nodes are also different. Node n12, n10, n7, and n11 are sensitive nodes when holding "1", and when holding "0", node n9, n12, n11, and n8 are sensitive nodes. Therefore, in terms of DNU, taking holding "1" as an example, the sensitive node pairs are <n10, n12> and <n7, n11> , and <n9, n12>, <n8, n11> when holding "0".

Next, let us take tolerating <n8, n11> upset as an example to illustrate the principle of DNU tolerance capability in the leader latch. In the case of D=0, one of the sensitive pairs is <n8, n11>, node n7, n8, and n11 are all at the "1" state. If node n8 flip from 1 to 0, the voltage level at node n9, n10, and n12 will not be changed. If node n11 also flips from 1 to 0 at this time, due to the existence of the high-threshold transistor T1, the voltage level at the gate terminal of T2 will be slightly higher than GND, making T2 work in the saturation region, and also making T2 and T3 form a P-stack structure. Thus, node n7 is in a weak "1" state, and finally, the state of n9, n10, and n12 will remain. For other DNU cases, the tolerance principle is similar.

B. Hardening Method in Follower Latch

We proposed a novel feedback cut-off hardening method in the follower latch. The idea of hardening circuit by cutting off feedback was initially originated from [13]. However, it is limited to the double-phase clocking circuit and SNU tolerance. In order to be more suitable for a single-phase clocking circuit by applying feedback cut-off technology, we have proposed some new circuits in the follower latch to tolerate soft errors. As can be seen from the green part of Fig. 3, T3 and T4 are kept "off" in the holding phase to cut off the feedback and is connected to the input terminal of the two split-output inverters separately. It should be noted that transmission gate T6 is a high-threshold transistor to reduce the impact of m5 flipping on node Q, moreover, T4 and T5 are low-threshold transistors to increase the sub-threshold current, thereby enhancing the ability to store charge.

Since the PMOS transmission gate is turned on during the holding phase, the sensitive nodes in the follower latch are nodes m1~m5 and Q. Note that there is a fact that a particle hit induces a current which always flows from the n-type diffusion to the p-type diffusion, through a junction. It means that a radiation particle can only result in logic 0→1 (1→0) for only PMOS (NMOS) transistors. Therefore, when holding "1", the sensitive nodes are nodes m1, m2, m3, m5, and, Q. And when holding "0", the sensitive nodes are nodes m4, m5, and Q. In addition, we place node m1 and m2 far apart physically to prevent mutual influence. Therefore, the sensitive pairs are <m1, m3>, <m2, m3>, <m3, m5>, <m5, Q> for holding "1" and <m4, m5>, <m5, Q> for holding "0". In the "1" phase, when node m2 or m3 is hit (1→0), the other node will help it to recover. As long as one or two of m3, m4, m5, or Q flip at the same time, the charge stored at m1 or m2 will correct it/them to their original state.

In summary, we have made improvements in both the leader and follower latch, embedding the CROUT structure in the leader latch and proposing a new feedback cut-off structure in the follower latch. Moreover, from the perspective of Design For Testability (DFT), TRIGON can also be made into a scan Flip-Flop by connecting a multiplexer to input D, such that these two inputs of the multiplexer serve as the functional input signal from the combinational logic and the scan-in signal from the outside.

IV. Experimental Results

In this section, we will show the experimental results, including the radiation tolerance verification in Sec. IV. A and the performance analysis in Sec. IV.B and IV.C. All the results are based on TSMC 40nm process and generated by Cadence Spectre. For every reference circuit, we took the minimum transistor size on the premise of the intact function.

A. Radiation Tolerance Analysis

To assess the SNU and DNU tolerance results, a double-exponential current source was injected into the sensitive nodes in both leader latch and follower latch. The rise time and fall time were set to 10ps and 200ps respectively and the injected charge was 75fC.

Firstly, let's see the effect of SNU and DNU tolerance for the leader latch after injecting the current source in Fig. 5 and Fig.6 respectively. Take the case of D=0 as an example, in this case, as described in Sec. III.A, the sensitive nodes are nodes n11, n8, n9, and n12. It can be seen that after the current is injected into the four sensitive nodes, the output Qm can be restored to the original state or there is even no change.

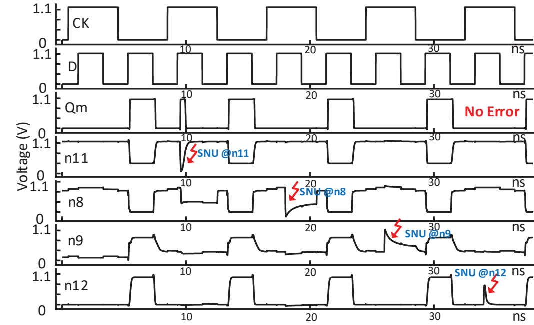


Fig. 5. Waveforms for the SNU tolerance in the leader latch.

For the DNU tolerance, in this case, the sensitive pairs are <n8, n11>, and <n9, n12>. Fig.6 shows that after the current is injected into two sensitive nodes at the same time during the holding phase, the output Qm will also not change. Similarly, in the case of D=1, the sensitive nodes, n7, n10, n11, and n12, can also be restored to the original state when the current is injected.

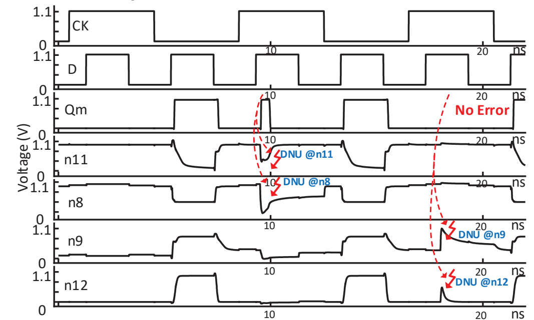


Fig. 6. Waveforms for the DNU tolerance in the leader latch.

For the follower latch, Fig. 7 and Fig. 8 show the SNU and DNU tolerance waveforms separately. As shown in Fig.7, when holding different states, its internal sensitive nodes are also different. When holding the state "1", the sensitive nodes are m1, m2, m3, m5, and Q (red arrows). Similarly, the sensitive nodes are m4, m5, and Q (orange arrows)when holding the state "0". After injecting the current source, the output Q can be restored to the original state.

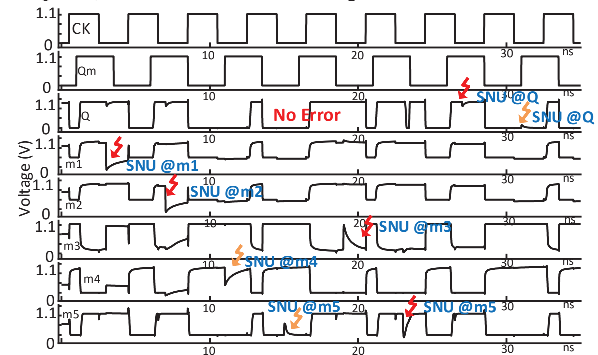


Fig. 7. Waveforms for the SNU tolerance in the follower latch.

For the DNU tolerance, when holding the "1" state, the sensitive pairs are <m1, m3>, <m2, m3>, <m3, m5>, <m5, Q>, <m1, Q>, and <m2, Q> (red arrows). When holding the "1" state, the sensitive pairs are <m4, m5> and <m5, Q> (orange arrows). Fig. 8 shows that after injecting the simulanteous current into the sensitive pairs, the output Q can also be restored to its original state.

TABLE I. PERFORMANCE COMPARSION UNDER DIFFERENT SUPPLY VOLTAGES

FF Type	Work as FF				SNU Tolerant				DNU Tolerant				Power (μW)			
	1.0V	*0.9V*	*0.8V*	*0.7V*	*1.0V*	*0.9V*	*0.8V*	*0.7V*	*1.0V*	*0.9V*	*0.8V*	*0.7V*	*1.0V*	*0.9V*	*0.8V*	*0.7V*
HPST	√	√	√	√	×	×	×	×	×	×	×	×	3.4	2.7	2.1	1.6
DONUT	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×
Delta-DICE	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×
CROUT	√	√	√	√	√	√	√	√	√	√	√	√	5.2	4.1	3.1	2.1
DNURHL	√	√	√	√	√	√	√	√	×	×	×	×	3.4	2.7	2.1	1.5
TRIGON (leader)	√	√	√	√	√	√	√	√	√	√	√	√	**3.2**	**2.4**	**1.8**	**1.2**
TRIGON (follower)					√	√	√	√	√	√	√	√				

FF Type	Delay(ps)				Energy-per-cycle (fJ)			
	1.0 V	*0.9 V*	*0.8V*	*0.7V*	*1.0V*	*0.9V*	*0.8V*	*0.7V*
HPST	20	30	49	99	14	11	8	6
DONUT	×	×	×	×	×	×	×	×
Delta-DICE	×	×	×	×	×	×	×	×
CROUT	19	28	46	104	21	16	12	8
DNURHL	61	86	137	261	13	11	8	6
TRIGON	**7.5**	**54**	**96**	**212**	**12**	**9**	**7**	**5**

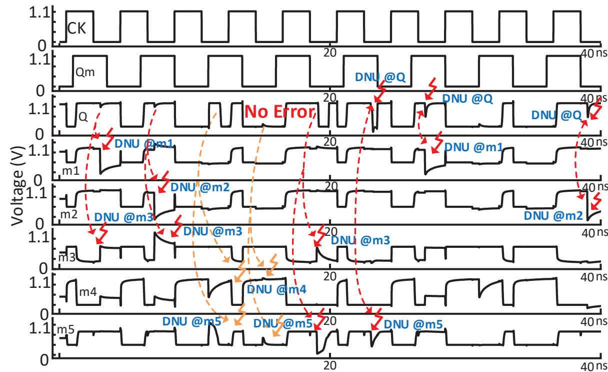


Fig. 8. Waveforms for the DNU tolerance in the follower latch

B. *Energy Efficiency Analysis*

As we discussed before, the obvious feature of our proposed design is that its single-phase clocking technology reduces energy consumption. Therefore, under different input data activities, we compared the proposed circuit with other reference works. As can be seen in Fig. 9, the proposed TRIGON achieves the smallest energy consumption under all data activities, 0%, 25%, and 50% separately.

In particular, when the input is static, TRIGON consumes only 1/8 of the energy of other reference circuits. The main reason is that under the static input, the power consumption of the circuit mainly depends on the dynamic power of the local clock buffer, which can also be explained by the phenomenon that the power consumptions of the other five reference circuits are similar. In other words, the low-power advantage of the proposed TRIGON based on a single-phase clock structure will be more obvious under the static input.

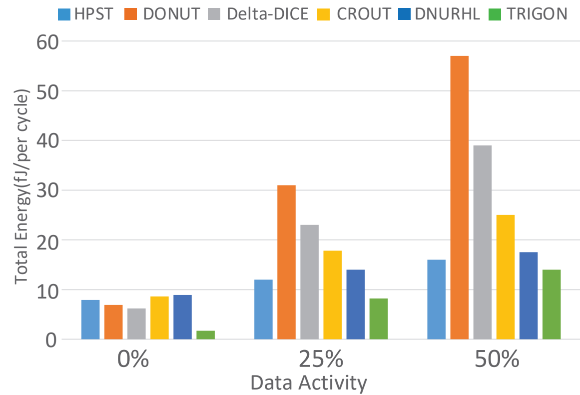


Fig. 9. Comparison of energy consumption under different data activities.

C. *Performance Comparison with other works*

Reducing the supply voltage is usually also a common method to reduce power consumption. Therefore, we selected four voltages under the standard supply voltage (1.1V) as the voltage reference voltage values. As shown in TABLE I, we compared whether the FF is still functional and also the SNU (DNU) tolerance capabilities are still present. We have also evaluated the power consumption, delay, and energy per cycle under these supply voltages. Different types of FF are marked with different colors. As described before, HPST is an SNU tolerant circuit, DONUT and Delta-DICE are normal DNU tolerant circuits, and CROUT and DNURHL are low-power hardened circuits.

It is clear that although HPST can hold its basic FF functionality under all voltages, it also loses the ability to tolerate SNU. In addition, for the two normal DNU tolerant circuits, they cannot even work normally as FF under lower voltages, let alone the capacity of soft error tolerance. In terms of the two low-power hardened circuits, except that DNURHL no longer has the ability to tolerate DNU, other functional indicators are the same as the proposed TRIGON. However, TRIGON obviously shows the superiority as it can function reliability as a DNU tolerant FF at low voltages and providing even lower power consumption.

In addition, we have compared the performance of all DNU tolerant circuits under the standard supply voltage (1.1V) in TABLE II. It can be seen that except for the delay indicator, which is worse than CROUT, TRIGON is in a leading position in other indicators. Especially, for the Power-Delay-Area-Product, TRIGON achieves a 56% reduction compared with the other four DNU tolerant references.

TABLE II. PERFORMANCE COMPARISON UNDER THE STANDARD SUPPLY VOLTAGE

FF Type	Comparison Parameter (under the standard supply voltage 1.1V)			
	Delay(ps)	***Power(μW)***	***Area (# of transistor)***	***PDAP ($\times 10^3$)***
DONUT	96(55%)	11.8(65%)	70(27%)	79.5(89%)
Delta-DICE	64(33%)	8.7(53%)	78(35%)	43.6(80%)
CROUT	25(-72%)	6.7(39%)	54(6%)	9(1%)
DNURHL	47(8.5%)	4.12(0.04%)	100(49%)	19.4(54%)
TRIGON	**43**	**4.1**	**51**	**8.9**

It should be noted that compared with other reference circuits, the delay of TRIGON is not the smallest, which is larger than CROUT in Table II. This is mainly because whether TRIGON is in the leader latch or follower latch, the output is not directly driven by the transmission gate connected to the input signal, while CROUT has this structure.

V. CONCLUSION

This paper proposes a low-power radiation-hardened Flip-Flop named TRIGON featuring the single-phase clocking structure. By eliminating the power consumption of the local clock buffer, TRIGON has achieved an 80% reduction in energy consumption compared with other reference circuits in the case of static input. Meanwhile, the leader latch and follower latch of TRIGON adopt different hardening methods according to their own characteristics. In the leader latch, we improved a hardening method based on the Schmidt trigger coupling structure. In the follower latch, a novel feedback cut-off structure was proposed. The current injection experiments showed that DNU can be tolerated in both leader and follower latches. Meanwhile, unlike most other existing solutions, TRIGON can reliably work at lower supply voltages, which can further reduce power consumption on the basis of single-phase clock technology.

VI. ACKNOWLEDGMENT

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