University Booth at DATE 2021

The University Booth is a long-standing tradition at DATE. This year, the UBooth will be located in **dedicated virtual rooms**. All demonstrations will take place from **Tuesday, February 2nd to Thursday, February 4th, 2021** during DATE virtual coffee breaks. Universities and public research institutes have been invited to submit hardware or software demonstrators, and we are happy to offer to DATE participants a compelling agenda.
The University Booth programme is composed of **23 demonstrations** from **10 countries**, presenting software and hardware solutions in the following main topics:

- **Electronic Design Automation Prototypes**
- **Hardware Design and Test Prototypes**
- **Embedded Artificial Intelligence**

The University Booth at DATE 2021 invites you to find out more about the latest trends in software and hardware from the international research community through actual demonstrators and prototypes.

DATE 2021 virtual edition features the University Booth at two levels:

1. **23 interactive sessions.** Exhibitors present their prototype to online attendees in 30-minutes interactive sessions spread over the three conference days.
2. **Demonstration videos.** Attendees can follow the exhibitors' presentations of the prototypes offline and asynchronously interact with authors through questions and answers.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this exciting programme for their involvement.

A “best demo” award will be granted during the Exhibition Coffee Break on Thursday, 04 February 2021 15:30:00 AoE. Every conference delegate will be able to vote a the demonstrator.
More information is available online at https://www.date-conference.com/exhibition/university-booth. The University Booth programme is available online at https://www.date-conference.com/programme. The following demonstrators will be presented at the University Booth.

JOINTER: JOINING FLEXIBLE MONITORS WITH HETEROGENEOUS ARCHITECTURES

Authors:
Giacomo Valente[1], Tiziana Fanni[2], Carlo Sau[3], Claudio Rubattu[2], Francesca Palumbo[2] and Luigi Pomante[1]
[1]Università degli Studi dell'Aquila, IT; [2]Università degli Studi di Sassari, IT; [3]Università degli Studi di Cagliari, IT

Timeslot: UB.1 (Tuesday, 02 February 2021 09:50 - 10:20)

Abstract*: As embedded systems grow more complex and shift toward heterogeneous architectures, understanding workload performance characteristics becomes increasingly difficult. In this regard, runtime monitoring systems can support on obtaining the desired visibility to characterize a system. This demo presents a framework that allows to develop complex heterogeneous architectures composed of programmable processors and dedicated accelerators on FPGA, together with customizable monitoring systems, keeping under control the introduced overhead. The whole development flow (and related prototypal EDA tools), that starts with the accelerators creation using a dataflow model, in*

parallel with the monitoring system customization using a library of elements, showing also the final joining, will be shown. Moreover, a comparison among different monitoring systems functionalities on different architectures developed on Zynq7000 SoC will be illustrated.

TAPASCO: THE OPEN-SOURCE TASK-PARALLEL SYSTEM COMPOSER FRAMEWORK

Authors:
Carsten Heinz, Lukas Sommer, Lukas Weber, Johannes Wirth and Andreas Koch, Embedded Systems & Applications, TU Darmstadt, DE

Timeslot: UB.2 (Tuesday, 02 February 2021 09:50 - 10:20)

***Abstract**: Field-programmable gate arrays (FPGA) are an established platform for highly specialized accelerators, but in a heterogeneous setup, the accelerator still needs to be integrated into the overall system. The open-source TaPaSCo (Task-Parallel System Composer) framework was created to serve this purpose: The fast integration of FPGA-based accelerators into compute platforms or systems-on-chip (SoC) and their connection to relevant components on the FPGA board. TaPaSCo can support developers in all steps of the development process: from cores resulting from High-Level Synthesis or cores written in an HDL, a complete FPGA-design can be created. TaPaSCo will automatically connect all processing elements to the memory- and host-interface and generate a complete bitstream. The TaPaSCo Runtime API allows to interface with accelerators from software and supports operations such as transferring data to the FPGA memory, passing values and controlling the execution of the accelerators.*

3D-MEM-THERM: A FAST, ACCURATE 3D MEMORY THERMAL SIMULATOR

Authors:
Lokesh Siddhu, Rajesh Kedia, Hameedah Sultan and Preeti Ranjan Panda, IIT Delhi, IN

Timeslot: UB.3 (Tuesday, 02 February 2021 17:00 - 17:30)

***Abstract**: Thermal issues have limited the widespread adoption of 3D memories. Fast and accurate thermal simulation can help in designing appropriate thermal management policies. Temperature-dependent leakage power, which causes significant heating in 3D memories, is not modeled accurately in existing thermal simulators like HotSpot. These simulators also do not account for the effect of process variations on leakage power. We augment HotSpot to address these challenges and propose a fast trace-based thermal simulator, namely 3D-Mem-Therm. 3D-Mem-Therm integrates several other novel features, such as support for evaluating thermal management policies, choosing memory layout from predefined 3D memory floorplans, etc. 3D-Mem-Therm is significantly faster than industry-standard simulators and estimates temperature accurately within one-degree centigrade. We plan to demonstrate these features of 3D-Mem-Therm for the rapid design of thermal management policies for 3D memories.*

MODULAR HARDWARE AND SOFTWARE PLATFORM FOR THE RAPID IMPLEMENTATION OF ASIC-BASED BIOANALYTICAL TEST SYSTEMS

Authors:
Alexander Hofmann, Peggy Reich, Marco Götze, Alexander Rolapp, Sebastian Uziel, Thomas Elste, Bianca Leistritz, Wolfram Kattanek and Björn Bieske, IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH), DE.

Timeslot: UB.4 (Tuesday, 02 February 2021 17:00 - 17:30)

***Abstract**: To support the complex and lengthy development of sensor ASICs for point-of-care diagnostics, there is a need for modular, flexible and powerful test systems, which are mainly needed for the test and characterization of sensor ASICs and for the prototypical realization of bioanalytical measurements. At IMMS, a modular hardware and software platform has been developed, which includes functional modules for power supply, electrical signal processing, digital signal processing, and modules for the control of fluidics, light sources, and heating elements. The platform software covers the control of the hardware modules as well as the acquisition and processing of measurement data. In addition, it enables the automated execution of measurement sequences. This contribution demonstrates the use of the platform with the example of an optoelectronic sensor ASIC for highly sensitive measurements of light absorption in liquids where the sensor detects small signal changes in a wide dynamic range.*

ELSA: FORMAL ABSTRACTION AND VERIFICATION OF ANALOG CIRCUITS

Authors:
Ahmad Tarraf and Lars Hedrich, University of Frankfurt, DE

Timeslot: UB.5 (Tuesday, 02 February 2021 17:00 - 17:30)

***Abstract**: The demonstration presents a recently published methodology that automatically generates accurate abstract models suited for verification and simulation routines with significant speed up factors. The abstraction methodology is based on sampling a Spice netlist at transistor level with full Spice BSIM accuracy. The approach generates a hybrid automaton (HA) that exhibits a linear behavior described by a state space representation in each of its locations, thereby modeling the nonlinear behavior of the netlist via multiple locations. Hence, due to the linearity of the obtained model, the approach is easily scalable. As the eigenvalues of the linearized system play a significant role in the abstraction process, the tool was named Elsa: eigenvalue-based hybrid linear system abstraction. The HAs can be deployed in various output languages: Matlab, Verilog-A, and SystemC-AMS*

LEARNV: A RISC-V BASED EMBEDDED SYSTEM DESIGN FRAMEWORK FOR EDUCATION AND RESEARCH DEVELOPMENT

Authors:
Noureddine Ait Said and Mounir Benabdenbi, TIMA Laboratory, FR

Timeslot: UB.6 (Tuesday, 02 February 2021 17:00 - 17:30)

***Abstract**: Designing a modern System on a Chip is based on the joint design of hardware and software (co-design). However, understanding the tight relationship between hardware and software is not*

straightforward. Moreover to validate new concepts in SoC design from the idea to the hardware implementation is time-consuming and often slowed by legacy issues (intellectual property of hardware blocks and expensive commercial tools). To overcome these issues we propose to use the open-source Rocket Chip environment for educational purposes, combined with the open-source LowRisc architecture to implement a custom SoC design on an FPGA board. The demonstration will present how students and engineers can take benefit from the environment to deepen their knowledge in HW and SW co-design. Using the LowRisC architecture, an image classification application based on the use of CNNs will serve as a demonstrator of the whole open-source hardware and software flow and will be mapped on a Nexys A7 FPGA board.

DEFACTO: DESIGN AUTOMATION FOR SMART FACTORIES

Authors:
Michele Lora[1], Pierluigi Nuzzo[2] and Franco Fummi[1]
[1]University of Verona, IT; [2]University of Southern California, US

Timeslot: UB.8 (Tuesday, 02 February 2021 18:30 - 19:00)

***Abstract**: The DeFacto project develops modeling paradigms, algorithms, and tools for the design of advanced manufacturing systems. Central to the project is the CHASE framework, combining a pattern-based specification language with a rigorous synthesis and verification back-end based on assume-guarantee contracts. The front-end supports automatic translation of requirements to low-level mathematical languages. The synthesis and verification back-end uses the mathematical formalism of contracts to reason about the design from specification to implementation. The demonstration shows the application of CHASE to the design of the control software governing a set of manufacturing tasks. Components and operations are specified in CHASE and formalized using contracts. CHASE coordinates its back-end tools to validate systems requirements, generate and validate implementations, highlighting the effectiveness of the decomposition mechanisms provided by contracts in the design of complex systems.*

GREYHOUND: DEEP FUZZING IOT WIRELESS PROTOCOLS

Authors:
Sudipta Chattopadhyay and Matheus E. Garbelini, Singapore University of Technology and Design, SG

Timeslot: UB.9 (Tuesday, 02 February 2021 18:30 - 19:00)

***Abstract**: In this booth, we present our recent works on automatically discovering (IoT) wireless protocol vulnerabilities. We discuss how well understood IoT wireless protocol features can go wrong at the design or implementation phase and contribute to the latest and relevant Wi-Fi and Bluetooth vulnerabilities that challenge our current trust in IoT technologies. We also dive deep on state-of-the-art wireless testing, which currently lacks proper tools when compared to common software testing, and present a unique insight of how to apply over the air testing to discover wireless vulnerabilities using off-the-shelf hardware. Lastly, we display our core ideas of Fuzzing (nicknamed "Greyhound") that made the discovery of SweynTooth possible (set of Bluetooth Low Energy vulnerabilities challenging millions of IoT products) and discuss why related vulnerabilities can be present under the nose of wireless system-on-chip vendors for many years without notice.*

SRAM-PUF: PLATFORM FOR ACQUISITION OF SRAM-BASED PUFS FROM MICRO-CONTROLLERS

Authors:
Sergio Vinagrero[1], Honorio Martin[2], Ioana Vatajelu[3] and Giorgio Di Natale[3]
[1]University of Grenoble Alpes, FR; [2]University Carlos III of Madrid, ES; [3]TIMA-CNRS, FR

Timeslot: UB.10 (Tuesday, 02 February 2021 18:30 - 19:00)

***Abstract**: This demonstration shows a versatile platform for the acquisition of the content of SRAM memories embedded in microcontrollers at power-up. The platform is able to power-off and -on hundreds of microcontrollers and to retrieve the content of their SRAMs thanks to a scan chain connecting all boards. The data collected is then stored in a database to enable reliability analysis.*

CATANIS: CAD TOOL FOR AUTOMATIC NETWORK SYNTHESIS

Authors:
Davide Quaglia and Enrico Fraccaroli, University of Verona, IT

Timeslot: UB.11 (Wednesday, 03 February 2021 09:00 - 09:30)

***Abstract**: The proliferation of communication technologies for embedded systems opened the way for new applications, e.g., Smart Cities and Industry 4.0. In such applications hundreds or thousands of smart devices interact together through different types of channels and protocols. This increasing communication complexity forces computer-aided design methodologies to scale up from embedded systems in isolation to the global inter-connected system. This booth will demonstrate the functionality of a graphic tool for automatic network synthesis developed in Python and QT to be lightweight and cross-platform. It allows to graphically specify the communication requirements of the application as a set of interacting tasks, the constraints of the environment (e.g., its map can be considered) together with a library of node types and communication protocols to be used.*

HARDBLOCK: DEMONSTRATOR OF PHYSICALLY BINDING AN IOT DEVICE TO A NON-FUNGIBLE TOKEN IN ETHEREUM BLOCKCHAIN

Authors:
Javier Arcenegui[1], Rosario Arjona[1] and Iluminada Baturone[2]
[1]Universidad de Sevilla - CSIC, ES; [2]Universidad de Sevilla -CSIC, ES

Timeslot: UB.12 (Wednesday, 03 February 2021 10:30 - 11:00)

***Abstract**: Nowadays, blockchain is a growing technology in the Internet of Thing (IoT) ecosystem. In this work, we show a demonstrator of an IoT device bound to a Non-Fungible Token (NFT) based on the ERC-721 standard of Ethereum blockchain. The advantages of our solution is that IoT devices can be controlled securely by events from the blockchain and authenticated users, besides being able to carry out blockchain transactions. The IoT device generates its own Blockchain Account (BCA) using a secret*

seed firstly generated by a True Random Number Generator (TRNG) and then reconstructed by a Physical Unclonable Function (PUF). A Pycom Wipy 3.0 board with the ESP32 microcontroller is employed as IoT device. The internal SRAM of the microcontroller acts as PUF and TRNG. The SRAM is controlled by a firmware developed in ESP-IDF. A smart contract developed in Solidity using Remix IDE creates the token. Kovan testnet and a Graphical User Interface programmed in Python are employed to show the results.

EUCLID-NIR GPU: AN ON-BOARD PROCESSING GPU-ACCELERATED SPACE CASE STUDY DEMONSTRATOR

Authors:
Ivan Rodriguez and Leonidas Kosmidis, BSC / UPC, ES

Timeslot: UB.13 (Wednesday, 03 February 2021 10:30 - 11:00)

***Abstract**: Embedded Graphics Processing Units (GPUs) are very attractive candidates for on-board payload processing of future space systems, thanks to their high performance and low-power consumption. Although there is significant interest from both academia and industry, there is no open and publicly available case study showing their capabilities, yet. In this master thesis project, which was performed within the GPU4S (GPU for Space) ESA-funded project, we have parallelised and ported the Euclid NIR (Near Infrared) image processing algorithm used in the European Space Agency's (ESA) mission to be launched in 2022, to an automotive GPU platform, the NVIDIA Xavier. In the demo we will present in real-time its significantly higher performance achieved compared to the original sequential implementation. In addition, visitors will have the opportunity to examine the images on which the algorithm operates, as well as to inspect the algorithm parallelisation through profiling and code inspection.*

BROOK SC: HIGH-LEVEL CERTIFICATION-FRIENDLY PROGRAMMING FOR GPU-POWERED SAFETY CRITICAL SYSTEMS

Authors:
Leonidas Kosmidis[1], Marc Benito[1], Matina Maria Trompouki[2] and Leonidas Kosmidis[1]
[1]Barcelona Supercomputing Center (BSC) and Universitat Politècnica de Catalunya (UPC), ES; [2]Universitat Politècnica de Catalunya (UPC), ES

Timeslot: UB.14 (Wednesday, 03 February 2021 17:00 - 17:30)

***Abstract**: GPUs can provide the increased performance required in future critical systems. However, their programming models, e.g. CUDA or OpenCL, cannot be used in such systems as they violate safety critical programming guidelines. Brook SC (https://github.com/lkosmid/brook) was developed in UPC/BSC to allow safety-critical applications to be programmed in a CUDA-like GPU language, Brook, which enables the certification while increasing productivity. In our demo, an avionics application running on a realistic safety critical GPU software stack and hardware is show cased. In this Bachelor's thesis project, which was awarded a 2019 HiPEAC Technology Transfer Award and a bronze medal at the ACM SRC at ICCAD 2020, an Airbus prototype application performing general-purpose computations with a safety-critical graphics API was ported to Brook SC in record time, achieving an order of*

magnitude reduction in the lines of code to implement the same functionality without performance penalty.

MAEVE: 3D HUMAN MOTION ANALYSIS EVALUATION FROM VIDEO AT THE EDGE

Authors:
Michele Boldo, Enrico Martini, Stefano Aldegheri, Nicola Valè, Matteo Bertucco, Alessandro Picelli, and Nicola Bombieri, University of Verona, IT

Timeslot: UB.15 (Wednesday, 03 February 2021 17:00 - 17:30)

Abstract*: In the last years, Human Pose Estimation has become a trend topic for human motion analysis. The fields of application are in continuous growth, such as diagnostic use for functional rehabilitation. Until now, IMUs and marker-based systems were used to estimate the pose, with the drawback of being invasive and expensive. This project presents the implementation of a ROS2-based approach that allows a single RGB-D camera applied to a low-power device with a GPU to estimate the 3D human pose through a CNN-based inference application without using external equipment in addition to the device. This allows for a flexible, modular architecture that is independent from the CNN model used to obtain the pose. Compared to the state-of-the-art solutions that rely on 2D pose estimation and that requires high performance computers or that provide only 2D support at the edge, our approach allows for 3D pose estimation on a low-power and low-cost embedded device while meeting real time constraints.*

MICRORV32: A SPINALHDL BASED RISC-V IMPLEMENTATION FOR FPGAS

Authors:
Sallar Ahmadi-Pour[1], Vladimir Herdt[2] and Rolf Drechsler[2]
[1]University of Bremen, DE; [2]University of Bremen / DFKI, DE

Timeslot: UB.16 (Wednesday, 03 February 2021 17:00 - 17:30)

Abstract*: We propose a demonstration of a lightweight RISC-V implementation called MicroRV32 that is suitable for FPGAs. The entire design flow is based on open source tools. The core itself is implemented in the modern Scala-based SpinalHDL hardware description language. For the FPGA flow, the IceStorm suite is utilized. On the iCE40 HX8K FPGA the design requires about 50% of the resources and can be run at a maximum clock frequency of 34.02 MHz. Beside the core, the design also includes basic peripherals and software examples. MicroRV32 is particularly suitable as a lightweight implementation for research and education. The complete design flow can be executed on a Linux system by means of open source tools which makes the platform very accessible.*

MELODI: A MASS E-LEARNING SYSTEM FOR DESIGN, TEST, AND PROTOTYPING OF DIGITAL HARDWARE

Authors:
Daniel Hauer, Friedrich Bauer, Felix Braun, Axel Jantsch, Markus D. Kobelrausch, Martin Mosbeck, Nima TaheriNejad and Philipp-Sebastian Vogt, TU Wien, AT

Timeslot: UB.17 (Wednesday, 03 February 2021 18:30 - 19:00)

Abstract*: Teaching and learning design, test, and prototyping of digital hardware requires substantial resources from both students (tool-chains, licenses, and FPGA development kits) and universities (laboratories, licenses, and substantial human resources). Mass E-Learning Of design, test, and prototyping DIgital hardware (MELODI) provides an efficient and economical full-stack solution to reduce these requirements and enables an effective online learning platform. MELODI is based on our previous experience with E-Learning (open-source system VELS) and communicates with students via email. It automatically generates randomized tasks (designed by teachers) for the students, evaluates their submissions and provides feedback to students and teachers. Lastly, it uses partial reconfiguration for efficient resource allocation on a FPGA with which students can interact remotely using a web interface and video stream. Our demonstrator shows MELODI from a task request to the interactive web page.*

NEUROMUSCULAR SYNERGIES BASED CYBER-PHYSICAL PLATFORM FOR THE FAST LACK OF BALANCE RECOGNITION

Authors:
Giovanni Mezzina, Sardar Mehboob Hussain and Daniela De Venuto, Politecnico di Bari, IT

Timeslot: UB.18 (Wednesday, 03 February 2021 18:30 - 19:00)

Abstract*: This demonstration proposes the preliminary version of a novel pre-impact fall detection (PIFD) strategy. The multi-sensing architecture jointly analyzes the muscular and cortical activity, from 10 EMG electrodes on the lower limbs and 13 EEG sites all along the scalp. Recorded data are numerically treated by an algorithm composed of two main units: the EMG computation branch and the EEG one. The first one has two main roles: (i) it treats the EMGs, translating them into binary signals (ii) it uses these signals to enable the EEG branch. The EEG computation branch evaluates the rate of variation of the EEG power spectrum density, named m, to describe the cortical responsiveness in five bands of interest. The proposed architecture has been validated on five tasks: walking steps, curves, Timed Up&Go (TUG) test, obstacle avoidance and slip. Experimental validation on 9 subjects showed that the system can identify a potential fall in 370.62 ms, with a sensitivity of the 93.33%.*

NYUZI: AN OPEN SOURCE GPGPU FOR GRAPHICS, ENHANCED WITH OPENCL COMPILER FOR CALCULATIONS

Authors:
Nima TaheriNejad, Edwin Willegger, Mariusz Wojcik, Markus Kessler, Johannes Blatnik, Ioannis Daktylidis, Jonas Ferdig and Daniel Haslauer, TU Wien, AT

Timeslot: UB.19 (Wednesday, 03 February 2021 18:30 - 19:00)

***Abstract**: Nyuzi is an open source processor designed for highly parallel, computationally intensive tasks and GPGPU applications. It was inspired by Intel's Larrabee, although the instruction set and the micro architecture are different. Among fully open source GPUs (with soft IPs), Nyuzi provides the most complete tool set. It is the only open source GPGPU with proven support for graphic applications. Moreover, we have recently added OpenCL compilation capabilities to it, enabling it to perform scientific calculations too. Hence, Nyuzi can be used to experiment with microarchitectural and instruction set design trade-offs for both graphic and scientific applications. The project includes a synthesizable hardware design written in System Verilog, an instruction set emulator, an LLVM based C/C++/OpenCL compiler, software libraries, and tests. In this demo, you will see Nyuzi in action: rendering graphics on FPGA and running OpenCL codes.*

SKELETOR: AN OPEN SOURCE EDA TOOL FLOW FROM HIERARCHY SPECIFICATION TO HDL DEVELOPMENT

Authors:
Ivan Rodriguez Ferrandez, Guillem Cabo, Javier Barrera, Jeremy Giesen, Alvaro Jover and Leonidas Kosmidis, BSC / UPC, ES

Timeslot: UB.20 (Thursday, 04 February 2021 17:00 - 17:30)

***Abstract**: Large hardware design projects have high overhead for project bootstrapping, requiring significant effort for translating hardware specifications to hardware design language (HDL) files and setting up their corresponding development and verification infrastructure. Skeletor (https://github.com/jaquerinte/Skeletor) is an open source EDA tool developed as a student project at UPC/BSC, which simplifies this process, by increasing developer's productivity and reducing typing errors, while at the same time lowers the bar for entry in hardware development. Skeletor uses a C/verilog-like language for the specification of the modules in a hardware project hierarchy and their connections, which is used to generate automatically the require skeleton of source files, verification testbenches and simulation scripts. Also we recently added support easy creation of pipeline design that also integrates with the already existing integration with KiCad schematics*

SHM-LSNN: DEMONSTRATION OF A BRAIN-INSPIRED STRUCTURAL HEALTH MONITORING SYSTEM

Authors:
Luca Zanatta, Emanuele Parisi, Francesco Barchi, Andrea Bartolini and Andrea Acquaviva, Università di Bologna, IT

Timeslot: UB.21 (Thursday, 04 February 2021 17:00 - 17:30)

***Abstract**: In this booth, we will demonstrate a data acquisition and processing system for Structural Health Monitoring (SHM) applications. SHM is a promising research field to provide reliable, effective and low-cost solutions for early detection of anomalies and ageing in civil structures. Energy*

consumption in such an application is of crucial importance to ensure long monitoring lifetime without human intervention. The booth will show a demo exploiting MEMS accelerometers and low-power deeply embedded microcontrollers to build a brain-inspired, event-based framework. Being inspired by the functionality of the brain, the pipeline uses spike events to process and classify structure health status in an energy-efficient way. The demo will show how the brain-inspired framework works and as well as the real-time power consumption of its main components. The demo will also demonstrate a potential implementation of the spike processing on a neuromorphic chip.

FPGA ACCELERATION OF APACHE SPARK SQL USING APACHE ARROW AND FLETCHER

Authors:
Zaid Al-Ars, Joost Hoozemans, Johan Peltenburg, Fabian Nonnenmacher and Ákos Hadnagy, Delft University of Technology, NL

Timeslot: UB.22 (Thursday, 04 February 2021 18:30 - 19:00)

***Abstract**: Apache Spark is one of the most widely used big data analytics frameworks due to its user-friendly API. However, the high level of abstraction in Spark introduces large overheads when accessing modern high-performance heterogeneous hardware accelerators such as FPGAs. This demo discusses solutions to accelerate Spark SQL queries using FPGAs to offload these computations transparently with little user configuration. In order to achieve this, we use the Apache Arrow in-memory format and the Fletcher hardware interface generator to exchange data efficiently with the accelerators. The performance of the proposed approach was benchmarked on a Power9 system with OpenCAPI, where our proof-of-concept accelerator was able to achieve more than 10x speedup for a filter-reduce query use case compared to a CPU-based Apache Spark implementation.*

MDD2FPGA: ROS-BASED EXPERIMENTAL ENVIRONMENT TOWARDS MODEL-DRIVEN-DEVELOPMENT WITH FPGA

Authors:
Hiroki Hashimoto, Harumi Watanabe and Takeshi Ohkawa, Tokai University, JP

Timeslot: UB.23 (Thursday, 04 February 2021 18:30 - 19:00)

***Abstract**: Performing complex calculation processing for the action planning of multiple robots with FPGA accelerates the process and contributes to the realization of MDD in a multiple robot system. By using the ROS environment to develop systems, it becomes possible to implement the calculation process in the FPGA and reduce the action planning latency for the entire multiple robot system. The problem is that the system's processing time increases when a high computational cost is required for the planning process to control multiple robots using ROS. To solve the problem, we implement the planning process by using FPGA as a ROS node in the ROS system to build an environment that accelerates the systems process. In this poster, the shortest path problem is adopted for the system's planning process. We evaluate the usefulness of the proposed environment by conducting processing experiments in the pilot environment.*

DESIGN AUTOMATION FOR EXTENDED BURST-MODE AUTOMATA IN WORKCRAFT

Authors:
Alex Chan, Danil Sokolov, Victor Khomenko and Alex Yakovlev, Newcastle University, GB

Timeslot: UB.24 (Thursday, 04 February 2021 18:30 - 19:00)

***Abstract**: Asynchronous circuits are known for their low-latency, robustness and low power consumption, which are particularly beneficial for the area of so-called "little digital" controllers. Finite State Machines (FSMs), such as Extended Burst-Mode (XBM), offers a simple design entry to specify asynchronous circuits. However, they are limited by outdated synthesis tools, and there are no dedicated tools for the formal verification of XBMs. On the other hand, Signal Transition Graphs (STGs) are an alternative to FSMs, offering access to sophisticated synthesis and verification tools. In this demo, we show the automation of XBMs in the Workcraft toolkit (https://workcraft.org) including its support for all features of the XBM model. Formal verification and logic synthesis of XBMs is also implemented via conversion to the established STG model, allowing XBMs to use existing methods and CAD tools.*

See you at the University Booth!
University Booth Co-Chairs
Frédéric Pétrot, IMAG, FR and
Nicola Bombieri, University of Verona, IT
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