

DATE Best Paper Awards

Each year the Design, Automation and Test in Europe Conference presents awards to the authors of the best papers. The selection is performed by the award committee composed of the Track Chairs Ian O'Connor , Theocharis Theocharides, Ilia Polian and Valeria Bertacco and the following members: Lorena Anghel, David Atienza, Koen Bertels, Christos-Savvas Bouganis , Luca Carloni, Stefano Di Carlo, Jose Flich, Pierre-Emmanuel Gaillardon , Tsung-Yi Ho, Artur Jutman, Huichu Liu, Jan Madsen, Maria K. Michael, Francesco Regazzoni, Johanna Sepulveda, Muhammad Shafique, Haralampos Stratigopoulos, Lionel Torres, Jiang Xu, Chengmo Yang.

The **DATE 2021** best papers are:

D Track

Leveraging Processor Modeling and Verification for General Hardware Modules

*Yue Xing, Huaxi Lu, Aarti Gupta, Sharad Malik
Princeton University*

A Track

A GPU-accelerated Deep Stereo-LiDAR Fusion for Real-time High-precision Dense Depth Sensing

*Haitao Meng, Chonghao Zho, Jianfeng Gu, Gang Chen
Sun Yat-sen University*

T Track

Microarchitectural Timing Channels and their Prevention on an Open-Source 64-bit RISC-V Core

*Nils Wistoff¹, Moritz Schneider¹, Frank Gurkaynak¹, Luca Benini², Gernot Heiser³
1 ETH Zurich, 2 Università di Bologna and ETH Zurich, 3 UNSW and Data61, CSIRO*

E Track

Adaptive Design of Real-Time Control Systems subject to Sporadic Overruns

*Paolo Pazzaglia¹, Anne Hamann², Dirk Ziegenbein², Martina Maggio³
1 Universität des Saarlandes, 2 Robert Bosch GmbH, 3 Lund University*

Best Paper Award Nominations

D Track

Correlated Multi-objective Multi-fidelity Optimization for HLS Directives Design

Qi Sun¹, Tinghuan Chen¹, Siting Liu¹, Jin Miao², Jianli Chen³, Hao Yu⁴, Bei Yu¹

*1 The Chinese University of Hong Kong, 2 Cadence Design Systems, 3 Fudan University,
4 Southern University of Science and Technology*

Leveraging Processor Modeling and Verification for General Hardware Modules

Yue Xing, Huaxi Lu, Aarti Gupta, Sharad Malik

Princeton University

3D Heterogeneous ReRAM Architecture for Training Graph Neural Networks

Aqeeb Iqbal Arka¹, Biresh Kumar Joardar¹, Jana Doppa¹,

Partha Pratim Pande¹, Krishnendu Chakrabarty²

1 Washington State University, 2 Duke University

LSP: Collective Cross-Page Prefetching for NVM

Haiyang Pan, Yuhang Liu, Tianyue Lu, Mingyu Chen

Chinese Academy of Sciences

Efficient Resource Management of Clustered Multi-Processor Systems
Through Formal Property Exploration

Ourania Spantidi¹, Iraklis Anagnostopoulos¹, Georgios Fainekos²

1 Southern Illinois University Carbondale, 2 Arizona State University

Margin-Maximization in Binarized Neural Networks for Optimizing Bit Error Tolerance

Sebastian Buschjäger, Jian-Jia Chen, Kuan-Hsun Chen, Mario Günzel, Christian Hakert,

Katharina Morik, Rodion Novkin, Lukas Pfahler, Mikail Yayla

Technical University of Dortmund

FPGA Architectures for Approximate Dense SLAM Computing

Maria-Rafaela Gkeka, Alexandros Patras, Christos D. Antonopoulos,

Spyros Lalis, Nikolaos Bellas

University of Thessaly

Technology Lookup Table based Default Timing Assertions
for Hierarchical Timing Closure

Ravi Ledalla, Chaobo Li, Debjit Sinha, Adil Bhanji,

Gregory Schaeffer, Hemlata Gupta, Jennifer Basile

IBM Corporation

COMPACT: Flow-Based Computing on Nanoscale Crossbars
with Minimal Semiperimeter

Sven Thijssen¹, Sumit Kumar Jha², Rickard Ewetz¹

1 University of Central Florida, 2 University of Texas at San Antonio

In-Memory Nearest Neighbor Search with FeFET Multi-Bit Content-Addressable Memories

Arman Kazemi¹, Mohammad Mehdi Sharifi¹, Ann Franchesca Laguna¹, Franz Mueller²,

Ramin Rajaei¹, Ricardo Olivo², Thomas Kaempfe², Michael Niemier¹, X. Sharon Hu¹

1 University of Notre Dame, 2 Fraunhofer IPMS-CNT

A Track

Origin: Enabling On-Device Intelligence for Human Activity Recognition

Using Energy Harvesting Wireless Sensor Networks

Cyan Subhra Mishra, John (Jack) Sampson, Mahmut Kandemir, Vijaykrishnan Narayanan

The Pennsylvania State University

A GPU-accelerated Deep Stereo-LiDAR Fusion for

Real-time High-precision Dense Depth Sensing

Haitao Meng, Chonghao Zho, Jianfeng Gu, Gang Chen

Sun Yat-sen University

Exploiting Secrets by Leveraging Dynamic Cache Partitioning of Last Level Cache

Anurag Agarwal, Jaspinder Kaur, Shirshendu Das

Indian Institute of Technology Ropar

As Accurate as Needed, as Efficient as Possible:

Approximations in DD-based Quantum Circuit Simulation

Stefan Hillmich¹, Richard Kueng¹, Igor L. Markov², Robert Willie¹

1 Johannes Kepler University Linz, 2 University of Michigan

T Track

Characterization and Fault Modeling of Intermediate State Defect in STT-MRAMs

Lizhou Wu¹, Siddharth Rao², Mottaqiallah Taouil¹, Erik Jan Marinissen²,

Gouri Sankar Kar², Said Hamdioui¹

1 Delft University of Technology, 2 IMEC

Device- and Temperature Dependency of Systematic Fault Injection Results
in Artix-7 and iCE40 FPGAs

Christian Fibich¹, Martin Horauer¹, Roman Obermaisser²

1 University of Applied Sciences Technikum Wien, 2 University of Siegen

DNN-Life: An Energy-Efficient Aging Mitigation Framework for Improving the Lifetime of On-Chip Weight Memories in Deep Neural Network Hardware Architectures

Muhammad Abdullah Hanif¹, Muhammad Shafique²

1 Vienna University of Technology, 2 New York University Abu Dhabi

Digital test of ZigBee transmitters: Validation in industrial test environment

Thibault Vayssade¹, Florence Azais¹, Laurent Latorre¹, François Lefevre²

1 Université de Montpellier, 2 NXP Semiconductors

Making Obfuscated PUFs Secure Against Power Side-Channel Based Modeling Attacks

Trevor Kroeger¹, Wei Cheng², Sylvain Guilley², Jean-Luc Danger², Naghmeh Karimi¹

1 University of Maryland, 2 Institut Polytechnique de Paris

Microarchitectural Timing Channels and their Prevention
on an Open-Source 64-bit RISC-V Core

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E Track

TinyADC: Peripheral Circuit-aware Weight Pruning Framework
for Mixed-signal DNN Accelerators

*Geng Yuan¹, Payman Benham², Yuxuan Cai¹, Ali Shafiee³, Jingyan Fu⁴,
Zhiheng Liao⁴, Zhengang Li¹, Xiaolong Ma¹, Jieren Deng⁵, Jinhui Wang⁶,
Mahdi Bojnordi², Yanzhi Wang¹, Caiwen Ding⁵*

*1 Northeastern University, 2 University of Utah, 3 Samsung, 4 North Dakota State University,
5 University of Connecticut, 6 University of South Alabama*

Adaptive Design of Real-Time Control Systems subject to Sporadic Overruns

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