DATE PhD Forum 2021

Date: Monday, 01 February 2021
Time: 17:00 - 19:00

The PhD Forum of the DATE Conference is a poster session hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

To this end, the forum takes place in two parts:

- First, everybody is invited to an opening session of the PhD Forum, where all presenters will present their work by means of a 1min pitch.
- After that (at approx. 17:30), all presenters will present their work within a 1.5 hour "poster" presentation in separate rooms. Within this timeframe, everyone can enter and leave the respective rooms and engage in corresponding discussions.

Furthermore, for each presentation, a poster (in pdf) summarizing the presentation will be provided.

Robert Wille, Johannes Kepler University Linz (Chair, DATE PhD Forum 2021)

PhD Forum Committee
Juergen Alt, Intel Germany
Armin Biere, Johannes Kepler University Linz
Philip Brisk, University of California, Riverside
Luigi Carro, UFRGS
Anupam Chattopadhyay, Nanyang Technological University
Rolf Drechsler, University of Bremen/DFKI
Marco Grossi, Università di Bologna
Ian Harris, University of California Irvine
Tsung-Yi Ho, National Tsing Hua University
Oliver Keszocze, Friedrich-Alexander University Erlangen
Martin Omana, DEI - University of Bologna
Graziano Pravadelli, University of Verona
Felipe Rocha da Rosa, UFRGS
Andreas Steininger, Vienna University of Technology
Sander Stuijk, Eindhoven University
Daniel Tille, Infineon Technologies
Shigeru Yamashita, Ritsumeikan University

Admitted Presentations

FM01.1.1 EXPLOITING ERROR RESILIENCE OF ITERATIVE AND ACCUMULATION BASED ALGORITHMS FOR HARDWARE EFFICIENCY
Dr. G.A. Gillani, University of Twente, NL

FM01.1.2 IMPROVING ENERGY EFFICIENCY OF NEURAL NETWORKS
Seongsik Park, Seoul National University, KR

FM01.1.3 DESIGN, IMPLEMENTATION AND ANALYSIS OF EFFICIENT HARDWARE-BASED SECURITY PRIMITIVES
Nalla Anandakumar Nachimuthu, Society for Electronic Transactions and Security (SETS), IN

FM01.1.4 FORMAL ABSTRACTION AND VERIFICATION OF ANALOG CIRCUITS
Ahmad Tarraf, research assistant uni frankfurt, DE

FM01.1.5 OPTIMIZATION TOOLS FOR CONVNETS ON THE EDGE
Valentino Peluso, Politecnico di Torino, IT

FM01.1.6 DESIGN SPACE EXPLORATION IN HIGH LEVEL SYNTHESIS
Lorenzo Ferretti, Università della Svizzera italiana, CH

FM01.1.7 RELIABILITY IMPROVEMENT OF STT-MRAM CACHE MEMORIES IN DATA STORAGE SYSTEMS
Elham Cheshmikhani, Sharif University of Technology, IR

FM01.1.8 ENABLING LOGIC-MEMORY SYNERGY USING INTEGRATED NON-VOLATILE TRANSISTOR TECHNOLOGIES FOR ENERGY-EFFICIENT COMPUTING
Sandeep Krishna Thirumala, Purdue University, US

FM01.1.9 HARDWARE SECURITY IN DRAMS AND PROCESSOR CACHES
Wenjie Xiong, Facebook AI Research, US

FM01.1.10 REAL-TIME HIGH-PERFORMANCE COMPUTING FOR EMBEDDED CONTROL SYSTEMS
Alejandro J. Calderón, Ikerlan Technology Research Centre, ES

FM01.1.11 LESS IS MORE: EFFICIENT HARDWARE DESIGN THROUGH APPROXIMATE LOGIC SYNTHESIS
Ilaria Scarabottolo, USI Lugano, CH

FM01.1.12 LONGLIVENOC: WEAR LEVELLING, WRITE REDUCTION AND SELECTIVE VC ALLOCATION FOR LONG LASTING DARK SILICON AWARE NOC INTERCONNECTS
Khushboo Rani, IIT Guwahati, IN

FM01.1.13 ENERGY EFFICIENT AND RUNTIME BASED APPROXIMATE COMPUTING TECHNIQUES FOR IMAGE COMPRESSION APPLICATION: AN INTEGRATED APPROACH COVERING CIRCUIT TO ALGORITHMIC LEVEL
Junqi Huang, University of Nottingham Malaysia, MY

FM01.1.14 THESIS: PERFORMANCE AND PHYSICAL ATTACK SECURITY OF LATTICE-BASED CRYPTOGRAPHY
Felipe Valencia, Univesità della Svizzera Italiana, CH

FM01.1.15 AMOEBA-INSPIRED SYSTEM CONTROLLER ON IOT EDGE
Anh Nguyen, Tokyo Institute of Technology, JP

FM01.1.16 MONITORING AND CONTROLLING INTERCONNECT CONTENTION IN CRITICAL REAL-TIME SYSTEMS
Jordi Cardona, Barcelona Supercomputing Center and Universitat Politecnica de Catalunya, ES

FM01.1.17 RELIABILITY CONSIDERATIONS IN THE USE OF HIGH-PERFORMANCE PROCESSORS IN SAFETY-CRITICAL SYSTEMS
Sergi Alcaide, Universitat Politècnica de Catalunya - Barcelona Supercomputing Center (BSC), ES

FM01.1.18 HARDWARE SECURITY EVALUATION OF IOT EMBEDDED APPLICATIONS
Zahra Kazemi, PhD. Candidate, FR

FM01.1.19 A COMPUTER-AIDED DESIGN SPACE EXPLORATION FOR DEPENDABLE CIRCUITS
Stefan Scharoba, Brandenburg University of Technology, DE

FM01.1.20 ROBUST AND ENERGY-EFFICIENT DEEP LEARNING SYSTEMS
Muhammad Abdullah Hanif, Institute of Computer Engineering, Vienna University of Technology, AT

FM01.1.21 AUTOMATED DESIGN OF APPROXIMATE ACCELERATORS
Jorge Castro-Godínez, Karlsruhe Institute of Technology (KIT), DE

FM01.1.22 NEXT GENERATION DESIGN FOR TESTABILITY, DEBUG AND RELIABILITY USING FORMAL TECHNIQUES
Sebastian Huhn, University of Bremen, DE

FM01.1.23 DESIGN AUTOMATION FOR FIELD-COUPLED NANOTECHNOLOGIES
Marcel Walter, University of Bremen, DE

FM01.1.24 HARDWARE AND SOFTWARE TECHNIQUES FOR SECURING INTELLIGENT CYBER-PHYSICAL SYSTEMS
Faiq Khalid, TU Wien, AT