Wafer-Level Test Path Pattern Recognition and Test Characteristics for Test-Induced Defect Diagnosis

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***Abstract*—Wafer defect maps provide precious information of fabrication and test process defects, so they can be used as valuable sources to improve fabrication and test yield. This paper applies artificial intelligence based pattern recognition techniques to distinguish fab-induced defects from test-induced ones. As a result, test quality, reliability and yield could be improved accordingly. Wafer test data contain site-dependent information regarding test configurations in automatic test equipment, including effective load push force, gap between probe and load-board, probe tip size, probe-cleaning stress, etc. Our method analyzes both the test paths and site-dependent test characteristics to identify test-induced defects. Experimental results achieve 96.83% prediction accuracy of six NXP products, which show that our methods are both effective and efficient.**

Keywords—wafer test, wafer defect map, test-induced defects, test path recognition, test yield.

I. Introduction

The most serious problem of manufacturing test is that it may induce defects to good dies produced in the fabrication process. *Test-induced defects* will lead to extreme test economics problem and thus process engineers and test engineers take long time to dig them out. This paper focuses on one of the most significant and frequent test-induced defects: *Test Site Dependent problem*.

II. Problem Definition

In order to improve test quality and to identify if a defect is introduced in the fabrication or test processes, we will define *Test Characteristics of Site-Dependent Defects* in this section. Site-dependent defects are the most significant category in test-induced defects, especially for wafer test related issues [1]-[6].

Site Dependence in Fig. 1(a) is that there exists some continuous fail dies caused by specific site problem in wafer test. Thus, fail dies will lead to specific test path patterns, which match the corresponding *Site Dependent Tracks* in Fig. 1(c).

A. Definition of Site-Dependent Defects

Site-Dependent Defects have the following two features.

Condition 1: Fail dies are highly correlated to the Test Paths.

Condition 2: Fail dies concentrate on some specific site(s).

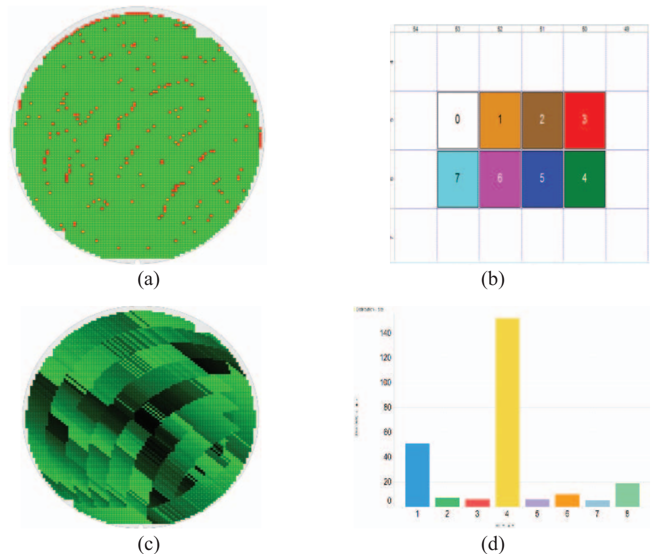


Fig. 1. Site Dependence, (a) a test-site-dependent wafer defect pattern, (b) 8-site test site/probing configuration, (c) test probing order, (d) number of defect dies scanned by 8 test sites/probes.

Due to test standardization in automatic test equipment (ATE), all wafers of the same product will have the same test configuration. That is, all test path setup in Fig. 1(c) and site configuration in Fig. 1(b) are the same.

In Fig. 1(d), the definition of Site Dependent Defects holds since the number of fail dies concentrates on Sites 1 and 4. In Fig. 1(d), *x*-axis gives site number, and *y*-axis gives the number of fail dies. The *extraordinary number of fail dies* associated with some specific sites defines the 2nd condition above.

B. Demonstrative Example of Site Dependence

Three typical cases of defects are shown in Fig. 2:

- Case 1: Typical **Site Dependence** in Test-induced wafer-level defects, which complies with both conditions.
- Case 2: Typical Fab-induced wafer-level defects: **Local/ Clustering** type, which fails in both conditions.
- Case 3: Typical Fab-induced wafer-level defects: **Scratch** type, which fails in both conditions.

Examples of the three cases are given in Fig. 2. According to the above three typical cases, we observe that the disparity of fail dies in sites is a very significant feature in test-induced site-dependent defects. Thus, Case 1 is test-induced, while both Cases 2 and 3 are fab-induced. The disparity of fail dies among all sites is the most significant test feature that can be used to distinguish between fab- and test-induced defects.

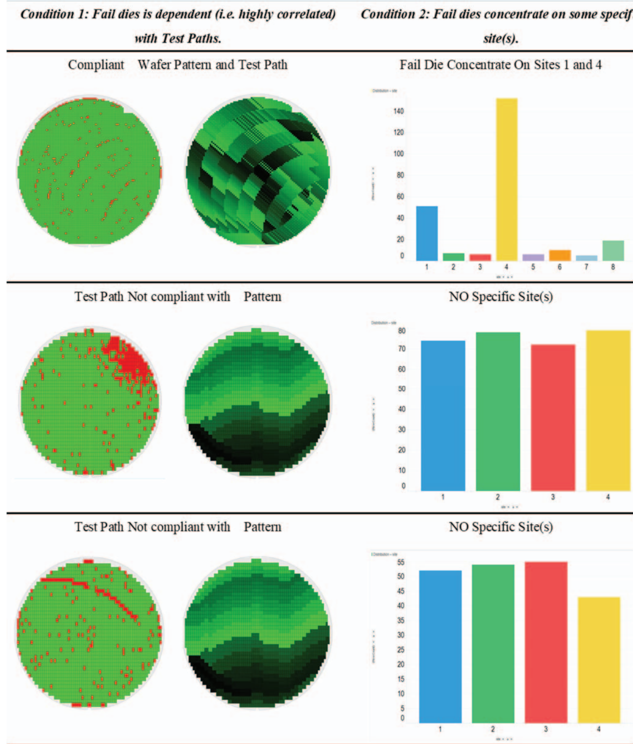


Fig. 2. Demonstrative Examples of site-dependent defects.

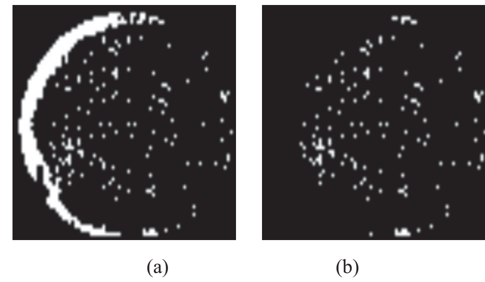
III. Identifying Site Dependent Test-Induced Defects

First, we need to filter out the conventional fab-induced defects. We apply the Unsupervised Learning model DBSCAN (Density-based spatial clustering of applications with noise) to select non-clustered dies, as shown in Fig. 3. Then, we will conduct Edge Filtering as shown in Fig. 4. The processed wafer maps are then analyzed using machine learning techniques, including Multilayer Perceptron (MLP), to determine whether the remaining defects are test-induced.

IV. Experiment Results

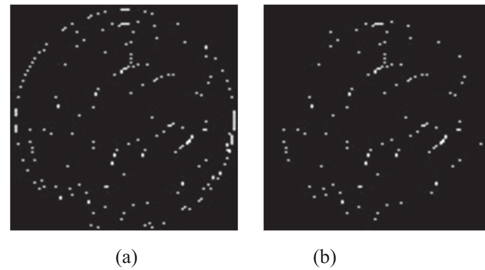
The proposed method is validated using six NXP products. The experimental setups and results are summarized in Table I, including the number of training wafers, the number of test wafers, prediction accuracy, and the corresponding confusion matrix.

Please note that the prediction accuracy accounts for true positives and true negatives (i.e. whether test-induced defects or not). Experimental results show that the prediction accuracy is higher than 94% in every case. On average the proposed method achieves 96.83% prediction accuracy.



(a) (b)

Fig. 3. An illustrative example of wafer map: (a) original wafer map, (b) after applying DBSCAN Clustering scheme.



(a) (b)

Fig. 4. Wafer map (a) original, (b) after Edge Filtering.

TABLE I. Prediction Accuracy

Product	Training Wafers	Test Wafers	Accuracy	Confusion Matrix
P-1	1006	252	98.02%	[163 3] [2 84]
P-2	4314	1079	97.22%	[408 18] [12 641]
P-3	1132	284	94.01%	[226 6] [11 41]
P-4	4744	1186	98.23%	[283 14] [7 882]
P-5	4116	1029	95.34%	[843 22] [26 138]
P-6	7486	1872	98.18%	[991 10] [24 847]

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