DATE Best Paper Awards

Each year the Design, Automation and Test in Europe Conference presents awards to the authors of the best papers. The selection is performed by the award committee composed of the Track Chairs Cristiana Bolchini, Theocharis Theocharides, Jaume Abella and Valeria Bertacco and the following members:Borzoo Bonakdarpour,Andrea Calimera, Ramon Canal, Luca Carloni, Alessandro Cimatti, Ayse Coskun, Nikil Dutt, Ioannis Papaefstathiou, Dionisios Pnevmatikatos, Davide Quaglia,Muhammad Shafique, Olivier Sentieys, Luis Miguel Silveira, Juergen Teich, Vasileios Tenentes, Jerzy Tyszer, Arnaud Virazel.

The **DATE 2020** best papers are:

D Track

Impact of Magnetic Coupling and Density on STT-MRAM Performance

Lizhou Wu[1]; Siddharth Rao[2]; Mottaqiallah Taouil[1]; Erik Jan Marinissen[2];
Gouri Sankar Kar[2]; Said Hamdioui[1]
1 *Delft University of Technology, 2 IMEC*

A Track

A Flexible and Scalable NTT Hardware:
Applications from Homomorphically Encrypted Deep Learning to Post-Quantum Cryptography

Ahmet Can Mert[1]; Emre Karabulut[2]; Erdinc Ozturk[1]; Erkay Savas[1];
Michela Becchi[2]; Aydin Aysu[2]
1 Sabanci University, 2 North Carolina State University

T Track

DEFCON: Generating and Detecting Failure-prone Instruction Sequences via Stochastic Search

Ioannis Tsiokanos[1]; Lev Mukhanov[2]; Giorgis Georgakoudis[3];
Dimitrios S. Nikolopoulos[4]; Georgios Karakonstantis[1]
1 Queen's University Belfast, 2 QUB, 3 Lawrence Livermore National Laboratory,
4 Virginia Tech

E Track

Statistical Time-based Intrusion Detection in Embedded Systems

Nadir Carreon Rascon; Allison Gilbreath; Roman Lysecky
University of Arizona

Best Paper Award Nominations

D Track

Fast and Accurate DRAM Simulation: Can we Further Accelerate it?
Johannes Feldmann[1]; Matthias Jung[2]; Kira Kraft[1]; Lukas Steiner[1]; Norbert Wehn[1]
1 TU Kaiserslautern, 2 Fraunhofer IESE

ESP4ML: Platform-Based Design of Systems-on-Chip for Embedded Machine Learning
Davide Giri; Kuan-Lin Chiu; Giuseppe Di Guglielmo; Paolo Mantovani; Luca Carloni
Columbia University

Verification Runtime Analysis: Get the Most Out of Partial Verification
Martin Ring[1]; Fritjof Bornebebusch[1]; ChristophLüth[1,2]; Robert Wille[3]; Rolf Drechsler[1,2]
1 DFKI, 2 University of Bremen, 3 Johannes Kepler University Linz

Gap-free Processor Verification by S²QED and Property Generation
Keerthikumara Devarajegowda[1]; Mohammad Rahmani Fadiheh[2]; Eshan Singh[3]; Clark Barrett[3]; Subhasish Mitra[3]; Wolfgang Ecker[1]; Dominik Stoffel[2]; Wolfgang Kunz[2]
1 Infineon Technologies, 2 TU Kaiserslautern, 3 Stanford University

GANA: Graph Convolutional Network Based Automated Netlist Annotation for Analog Circuits
Kishor Kunal[1]; Tonmoy Dhar[1]; Meghna Madhusudan[1]; Jitesh Poojary[1]; Arvind Sharma[1]; Wenbin Xu[2]; Steven Burns[3]; Jiang Hu[2]; Ramesh Harjani[1]; Sachin S. Sapatnekar[1]
1 University of Minnesota, 2 Texas A&M University, 3 Intel Corporation

Backtracking Search for Optimal Parameters of a PLL-based True Random Number Generator
Brice Colombier; Nathalie Bochard; Florent Bernard; Lilian Bossuet
University of Lyon

GRAMARCH: A GPU-ReRAM based Heterogeneous Architecture for Neural Image Segmentation
Biresh Kumar Joardar[1]; Nitthilan Kannappan Jayakodi[1]; Jana Doppa[1]; Partha Pratim Pande[1]; Hai (Helen) Li[2]; Krishnendu Chakrabarty[3]
1 Washington State University, 2 Duke University/TUM-IAS, 3 Duke University

PSB-RNN: A Processing-in-Memory Systolic ArrayArchitecture using Block Circulant Matrices for Recurrent Neural Networks
Nagadastagiri[1]; Sahithi Rampalli[1]; Makesh Tarun Chandran[1]; Gurpreet Singh Kalsi[2]; John (Jack) Sampson[1]; Sreenivas Subramoney[2]; Vijaykrishnan Narayanan[1]
1 The Pennsylvania State University, 2 Processor Architecture Research Lab, Intel Labs

A Learning-Based Thermal Simulation Framework
for Emerging Two-Phase Cooling Technologies
Zihao Yuan[1]; Geoffrey Vaartstra[2]; Prachi Shukla[1]; Zhengmao Lu[2]; Evelyn Wang[2]; Sherief Reda[3]; Ayse Coskun[1]
1 Boston University, 2 Massachusetts Institute of Technology, 3 Brown University

ProxSim: Simulation Framework for Cross-Layer Approximate DNN Optimization
Cecilia De la Parra[1]; Andre Guntoro[1]; Akash Kumar[2]
1 Robert Bosch GmbH, 2 TU Dresden

A Framework for Adding Low-Overhead, Fine-Grained Power Domains to CGRAs
Ankita Nayak; Keyi Zhang; Raj Setaluri; Alex Carsello; Makai Mann; Stephen Richardson; Rick Bahr; Pat Hanrahan; Mark Horowitz; Priyanka Raina
Stanford University

Floating Random Walk Based Capacitance Solver for VLSI Structures
with Non-Stratified Dielectrics
Mingye Song; Ming Yang; Wenjian Yu
Tsinghua University

Ternary Compute-Enabled Memory based on Ferroelectric Transistors
for Accelerating Deep Neural Networks
Sandeep Krishna Thirumala; Shubham Jain; Sumeet Gupta; Anand Raghunathan
Purdue University

Impact of Magnetic Coupling and Density on STT-MRAM Performance
Lizhou Wu[1]; Siddharth Rao[2]; Mottaqiallah Taouil[1]; Erik Jan Marinissen[2]; Gouri Sankar Kar[2]; Said Hamdioui[1]
1 *Delft University of Technology, 2 IMEC*

A Track

GenieHD: Efficient DNA Pattern Matching Accelerator Using Hyperdimensional Computing
Yeseong Kim; Mohsen Imani; Niema Moshiri;Tajana Rosing
University of California San Diego

Achieving Determinism in Adaptive AUTOSAR
Christian Menard[1]; Andres Goens[1]; Marten Lohstroh[2]; Jeronimo Castrillon[1]
1 TU Dresden, 2 University of California, Berkeley

A Flexible and Scalable NTT Hardware: Applications from Homomorphically Encrypted Deep Learning to Post-Quantum Cryptography
Ahmet Can Mert[1]; Emre Karabulut[2]; Erdinc Ozturk[1]; Erkay Savas[1]; Michela Becchi[2]; Aydin Aysu[2]
1 Sabanci University, 2 North Carolina State University

AntiDOte: Attention-based Dynamic Optimization for Neural Network Runtime Efficiency
Fuxun Yu[1]; Chenchen Liu[2]; Di Wang[3]; Yanzhi Wang[1]; Xiang Chen[1]
1 George Mason University, 2 University of Maryland, 3 Microsoft

Go Unary: A Novel Synapse Coding and Mapping Scheme
for Reliable ReRAM-based Neuromorphic Computing
Chang Ma; Yanan Sun; Weikang Qian; Ziqi Meng; Rui Yang; Li Jiang
Shanghai Jiao Tong University

T Track

On Improving Fault Tolerance of Memristor Crossbar Based Neural Network Designs
by Target Sparsifying
Song Jin[1]; Songwei Pei[2]; Yu Wang[1]
1 North China Electric Power University,
2 Beijing University of Posts and Telecommunications

Synthesis of Fault-Tolerant Reconfigurable Scan Networks
Sebastian Brandhofer; Michael Kochte; Hans-Joachim Wunderlich
University of Stuttgart

DEFCON: Generating and Detecting Failure-prone Instruction Sequences
via Stochastic Search
Ioannis Tsiokanos[1]; Lev Mukhanov[2]; Giorgis Georgakoudis[3];
Dimitrios S. Nikolopoulos[4]; Georgios Karakonstantis[1]
1 Queen's University Belfast, 2 QUB, 3 Lawrence Livermore National Laboratory,
4 Virginia Tech

Thermal-Cycling-aware Dynamic Reliability Management in Many-Core System-on-Chip
Mohammad-Hashem Haghbayan[1]; Antonio Miele[2]; Zhuo Zou[3];
Hannu Tenhunen[1]; Juha Plosila[1]
1 University of Turku, 2 Politecnico di Milano,
3 Nanjing University of Computer Science and Technology

E Track

Deeper Weight Pruning without Accuracy Loss in Deep Neural Networks
Byungmin Ahn; Taewhan Kim
Seoul National University

ACOUSTIC: Accelerating Convolutional Neural Networks
through Or-Unipolar Skipped Stochastic Computing
Wojciech Romaszkan; Tianmu Li; Tristan Melton; Sudhakar Pamarti; Puneet Gupta
University of California Los Angeles

Statistical Time-based Intrusion Detection in Embedded Systems
Nadir Carreon Rascon; Allison Gilbreath; Roman Lysecky
University of Arizona

Energy-efficient runtime resource management for adaptable multi-application mapping
Robert Khasanov; Jeronimo Castrillon
TU Dresden

CPS-oriented Modeling and Control of Traffic Signals Using Adaptive Back Pressure
Wanli Chang[1]; Debayan Roy[2]; Shuai Zhao[1]; Anuradha Annaswamy[3]; Samarjit Chakraborty[2]
1 University of York, 2 Technical University of Munich,
3 Massachusetts Institute of Technology