Circuit Design and Design Automation for Printed Electronics

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***Abstract*—A Process Design Kit (PDK) for gravure-printed Organic Thin-Film Transistor (OTFT) technology is presented in this paper. The transistor model developed in the PDK enables an accurate prediction of static, dynamic and noise performance of complex organic circuits. The developed Electronic Design Automation (EDA) tools exploit an adaptive strategy to improve the versatility of the PDK in relation to the advancements of the manufacturing process. The design and experimental characterization of a Charge Sensitive Amplifier is used to demonstrate the effectiveness of the PDK. The availability of a versatile and accurate Process Design Kit is expected to enable a reliable design process for complex circuits based on an organic printed technology.**

Keywords—Process Development Kit (PDK), design automation, printed organic electronics, OTFTs.

I. Introduction

It is estimated that by 2020 the Internet of Things (IoT) will connect about 30 billion of devices to the existing internet infrastructure [1]. Smart sensors, wearables and disposable RFID are just a few example of solutions that will be intensively used in markets like home automation, automotive, healthcare and retail. In this scenario, Printed organic Electronics (PE) could provide a valid alternative to mainstream Si-technologies for massive production of ultra-low cost electronic devices. Indeed, PE can be manufactured at low-cost and with high-throughput exploiting fully-additive processes [2][3]. Furthermore PE enables the production of fully flexible circuits for application that demand large-area and/or flexible form factors, like large-area sensors

Despite the potential benefits, organic electronics did not appear on the market of IoT and wearables yet. Several technologic challenges must still be addressed before printed organic electronics will be mature for a broad use in commercial products.

Printed organic transistors typically suffer from limited yield, large parameter spread and some reliability issues. The yield problems, which originate from the high process throughput and the imperfect control of the actual printing conditions, limit the achievable circuit complexity in terms of device count. At the state of the art, only circuits with about 100 organic Thin-Film Transistors (OTFTs) can be printed with acceptable yield. This means that great care must be taken to simplify the printed circuitry as much as possible. Furthermore, specific circuit architectures must be designed to mitigate the sensitivity to OTFT parameter variability, preventing circuit failures. Additional OTFT instabilities such as bias stress, operational and shelf aging may further impact circuit performance and lifetime.

These are only some of the reasons that have limited the development of PE towards commercial exploitation. Another important factor that negatively affects the evolution of PE is the fact that Electronic Design Automation (EDA) tools for the design of complex systems based on PE technologies are still in their infancy. Only few Process Design Kits (PDKs) are reported in literature to-date [4][5][6]. Indeed, the constant evolution of the manufacturing steps during the technology advancement require regular adjustments of the PDK, reducing its effectiveness. In addition, the development of reliable transistor model remains still challenging due to the large variability of the devices.

In this context, we propose here a novel PDK specifically developed for a gravure-printed organic technology [2]. The primary objective of the work is to provide a versatile set of EDA tools to enable reliable design of complex circuit architectures using this PE process. To this aim, an exhaustive model of the OTFT (static, dynamic and noise) has been developed. Besides, a new approach based on the definition of a reduced set of technological key parameters is proposed to enable rapid adaptation of the PDK to the advancements of the manufacturing process. The complete PDK has been integrated in the commercial EDA software Cadence Virtuoso®.

The paper is further organized as follows: the detailed description of the proposed PDK is provided in Section II. The comparison between simulations and measurement results of a designed Charge Sensitive Amplifier (CSA) are presented in Section III, and used to demonstrate the efficacy of the PDK. Finally, conclusions are drawn in Section IV.

II. Proposed Process Design Kit

The PDK is developed for a unipolar p-type organic transistor technology [2] processed on 320 x 320 mm^2 PEN foils. The OTFTs are top-gate staggered bottom contacts. Gold source and drain contacts are patterned with a large-area photolithography process. The amorphous polymer semiconductor is gravure-printed and exhibits a mobility of 2.2 cm^2/Vs. A 550 nm thick organic dielectric is also printed using gravure technique. The OTFT stack is finished with a conductive ink-based screen-printed gate electrode. The source drain layer is used as reference for the alignment of the printed layers.

The description of the PDK is organized in two main parts. First, the transistor model (static, dynamic and noise) is presented. Next, the EDA tools developed to assist the circuit design flow are described.

A. Static transistor model

The electrical characteristics of the fabricated organic Thin-Film Transistors (OTFTs) are reproduced by means of a physical-based analytical model. The OTFT model accounts for both charge transport and charge injection. The charge transport in the channel is based on a variable range hopping transport in a Density of States (DOS) [7]. The DOS is described by a double-exponential function accounting for

both deep and tail states [8][9]. In the case of p-type OTFTs, the tail states are located at energies close to the Highest Unoccupied Molecular Orbital energy level (HOMO) and define the strong accumulation region of operation, while the deep states are located at energies far from the HOMO level and define the subthreshold operation. Since in OTFTs the gate voltage controls the position of the Fermi energy level through the DOS, it is important to account for both deep and tail states in order to provide a unified and accurate OTFT description in all regimes of operation. Following the same approach proposed in [9], the drain current expression due to the charge transport into the channel reads (1):

$$I_D = \frac{W}{L} K_0 (\psi_{GS}{}^{\gamma} - \psi_{GD}{}^{\gamma}) \quad (1)$$

where W and L are the OTFT channel width and length, respectively, K_0 is a pre-factor dependent on physical and geometrical parameters (temperature, energetic disorder, charge spatial localization, and gate-insulator capacitance), $\gamma = 2T_t/T$ is the normalized tail-states energy disorder, and Ψ_{GX} is defined as (2):

$$\psi_{GX} = \xi V_T F\left[\frac{V_G - V_{th} - V_X}{\xi V_T}\right] \quad (2)$$

where $F[.] = \log[1+\exp(.)]$, $\xi = \gamma^2(1+qN_d/C_i)/(\gamma-1)$, C_i is the gate insulator capacitance per unit area, N_d is the total density of deep states per unit surface, V_G, V_D, and V_S are the gate, drain, and source voltages, respectively, V_{th} is the threshold voltage, $V_T = k_B T/q$ is the thermal voltage, K_B is the Boltzmann constant, and q is the elementary charge. Then, according to [7], the channel length modulation and the off-current are included in the drain current model as follows (3):

$$I_D = \frac{W}{L}\left[K_0 (\psi_{GS}{}^{\gamma} - \psi_{GD}{}^{\gamma})\left(1 + \frac{\psi_{GS} - \psi_{GD}}{L E_{sat}}\right) + \frac{\psi_{GS} - \psi_{GD}}{W^2 R_{off}}\right] \quad (3)$$

where E_{sat} is the maximum electric field at the drain side when the OTFT is operated in saturation (i.e. $V_D > V_G - V_{th}$), and R_{off} accounts for the bulk current due to unintentional doping of the organic semiconductor (OSC). The model parameters are calculated by fitting the measured transfer characteristic of long-channel OTFT (L = 800 µm) at V_D = 0.1 V with the method reported in [8][9]. The extracted channel model parameters are listed in TABLE I.

TABLE I. EXTRACTED CHANNEL MODEL PARAMETERS

Parameter	***Symbol***	***Value***
Temperature	T	295 K
Dielectric capacitance per unit area	C_i	3.7 nF/cm^2
Normalized tail-states energy disorder	γ	2.07
Threshold voltage	V_{th}	3.04 V
Total density of deep states per unit area	N_d	2 x 10^{11} cm^{-2}/eV
Current pre-factor	K_0	1.66 x 10^{-9} A/V$^{\gamma}$
Off-resistance per unit area	R_{off}	1 x 10^6 Ω/µm^2
Max. electric field at drain in sat. regime	E_{sat}	3.6 V/µm

Moreover, transistors with channel length ranging from 800 µm to 5 µm are evaluated. The model accurately reproduces the measurements for channel lengths down to 40 µm, while a significant error occurs for shorter channel lengths. This can be ascribed to contact effects [11][12] as confirmed by plotting the L-normalized drain current as a function of channel length. Indeed, the normalized current of short channel transistors is lower than for long-channel devices. According to the analysis presented in [11][12][13], the contact resistance can be ascribed to the limited charge injection at the source contact due to a reversed biased Schottky barrier. At low drain voltages the energy barrier at the metal-semiconductor interface results in a reduced charge accumulation close to the contact region (defined by a length $L_c \approx 1$ µm) while at large V_D a full depletion region from the source edge to the channel is obtained. This behavior resembles a transistor operated in saturation. Therefore, we model the contact effects as a transistor with a channel length equal to the contact region L_c, a threshold voltage V_{tc} and electric field E_{sc} that accounts for the gate-dependent Schottky barrier lowering (4-5):

$$I_C = \frac{W}{L_c} K_c (\varphi_{GS}{}^{\gamma} - \varphi_{GC}{}^{\gamma})\left(1 + \frac{\varphi_{GS} - \varphi_{GC}}{L_c E_{sc}}\right) \quad (4)$$

$$\varphi_{GX} = \xi V_T F\left[\frac{V_G - V_{tc} - V_X}{\xi V_T}\right] \quad (5)$$

where V_C is the voltage drop at the injecting contact. The electrical characteristics of the OTFTs are modeled as the series of the channel model (2-3) and contact model (4-5). In order to obtain the contact model parameters (i.e. K_c, V_{tc}, E_{sc}) we calculate the contact characteristics by solving, for each set of I_D, V_G and V_D the equation (6):

$$I_D^{meas}(V_G, V_D, V_S) - I_D^{Eq.1}(V_G, V_D, V_S') = 0 \quad (6)$$

where $V_{S'} = V_S + V_C$, and V_C can be calculated by numerically solving (6). By fitting the extracted contact characteristics with the contact model (4-5) we found that V_{tc} can be described with a second-order polynomial function $V_{tc} = 4.5\ 10^{-3}\ F[V_G^2] + 0.71\ F[V_G] + 0.96$, $E_{sc} = 4.25\ \max(F[V_G])/F[V_G]$, and $K_c = 1.1\ 10^{-8}$ A/(V$^{\gamma}$).
The overall model, i.e. the channel model combined with the contact model, is validated in Fig. 1 and Fig. 2. It accurately predicts the transfer and output characteristics of short-channel (L = 5 µm) as well as long channel (L = 800 µm) OTFTs with the very same set of physical parameters.

The transistor model has been coded in VerilogA language and integrated in the PDK. In addition, Monte Carlo simulations have been enabled to assess the circuit performance in presence of process variations and device-to-device mismatch. These have been represented here as mobility and threshold voltage statistical variations and therefore affect the model parameters K_0 and V_{th}, respectively. One should note that all equations in this Section II.A have been written for an n-type TFT, to improve readability.

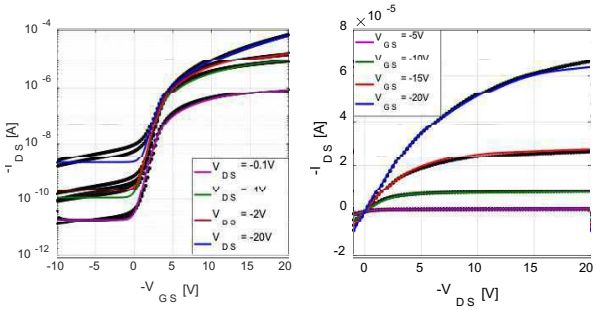

Fig. 1 : Measured (black points) and modelled (lines) transfer and output characteristics of an OTFT featuring W = 1000 µm, L = 5 µm.

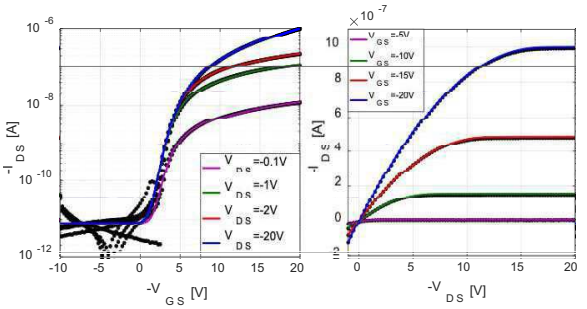

Fig. 2 : Measured (black points) and modelled (lines) transfer and output characteristics of an OTFT featuring W = 1000 µm, L = 800 µm.

B. *Dynamic transistor model*

The dynamic performance of the transistor is a fundamental design constraint in analog and digital circuits. The achievable speed in a circuit is mainly limited by the device parasitic capacitances. These capacitances become even more relevant in the case of printed organic transistors. Indeed, the printing resolution and the control of the overlay are typically in the order of ~µm [2], thus comparable with the OTFT feature size, leading to large parasitics.

For this reason, the intrinsic capacitances of the devices have been experimentally characterized. The measurement setup consists of an OTFT connected with probe needles and coax cables to a discrete Si transimpedance amplifier (TIA). The DC and AC currents provided by the organic transistor are translated into voltage by the TIA (Fig. 3) and fed to the HP35670A Dynamic Signal Analyzer in order to measure the frequency response. A 10 pF ± 0.01% discrete capacitor C_{cal} has been introduced to reduce the frequency span of the analysis. In order to investigate the bias dependency of the parasitic capacitances, multiple frequency sweeps have been recorded at different polarization conditions.

This current approach has been preferred to a direct admittance measurement employed in [14], due to the sensitivity of the results to the stray capacitances associated to the measurement setup.

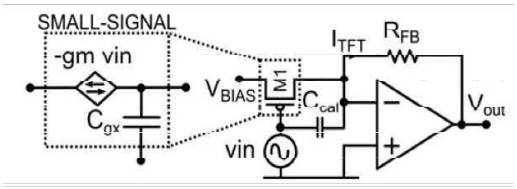

Fig. 3 : Simplified schematic of the measurement setup.

The frequency response of the circuit is analytically derived from the inspection of the small-signal circuit model in Fig. 3.

$$\frac{I_{TFT}}{vin} = -gm + j\omega(C_{gx} + C_{cal}) \quad (7)$$

Where gm is the small-signal transconductance and C_{gx} is the parasitic capacitance between gate and drain (or source according to the bias condition of the transistor). Next, the measured frequency sweep has been approximated with a first-order polynomial fitting and the parasitic capacitance value estimated from the fit. The extracted C-V curves for both C_{gd} and C_{gs} are shown in Fig. 4.

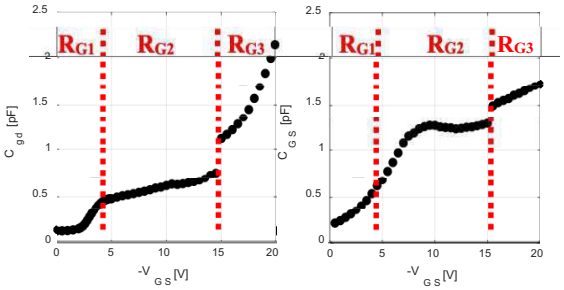

Fig. 4 : Extracted C_{gs} and C_{gd} C-V of a transistor featuring W=500µm and L=80µm. The measurements are performed at V_{DS}=-10V. The different operation regions of the OTFT are indicated with R_{G1} (off and subthreshold), R_{G2} (saturation) and R_{G3} (linear).

A numerical approach based on data fitting has been used to approximate the parasitic capacitance trends for the different bias conditions, and to scale the parasitics with the device size, leading to Equations 8(a-d):

$$C_{gx} = C_{gx1} + C_{gx2} + C_{gx3} \quad (8a)$$

$$C_{gx1} = 0.5WL_{ov}C_i \quad (8b)$$

$$C_{gx2} = \alpha_1 WLC_i\left(\frac{2}{\pi}\text{atan}([V_S - V_G + V_{th}]\alpha_2) + 1\right) \quad (8c)$$

$$C_{gx3} = \alpha_3 A_{OSC} C_i\left(\frac{2}{\pi}\text{atan}([-V_G + V_{th} - V_D]\alpha_4) + 1\right) \quad (8d)$$

Where L_{ov} is the overlap per unit length between drain (source) and gate electrodes, A_{OSC} is the total semiconductor area and α_1, α_2, α_3, α_4 are fitting parameters.

C. *Transistor noise model*

The noise behavior of field effect transistors is generally modelled with two current contributions, which are related to the thermal and flicker noise. According to [15] the Power Spectral Density associated to the thermal noise contribution is given by (9)

$$S_{TID} = 4k_B T(2/3gm) \quad (9)$$

Where k_B is the Boltzmann constant, T is the temperature, and gm is the transconductance of the transistor.

Low-frequency noise (flicker noise) in polymer thin-film transistor can be described by the mobility fluctuation theory [16]. Its PSD can be expressed by (10):

$$S_{FID} = \frac{\alpha_H q I_D^2}{fWLC_i(V_S - V_G + V_{th})} \quad (10)$$

Where f is the frequency, q is the elementary charge and α_H is the Hooge parameter. Noise measurements performed on different circuit architectures have been used to empirically estimate the value of α_H, which is equal to 0.05.

D. Design Rule Manual (DRM)

The design rules are geometrical restrictions used to guide the correct implementation of the circuit layout. These are typically derived from the manufacturing constraints of the technology, and therefore are process dependent. Indeed, the use of new inks or improvements in the printing process often require a redefinition of the design rules.

The reduction of fabrication costs is one of the main concerns in PE. This can be achieved by employing more aggressive design rules which maximize the device integration density, thus minimizing the circuit area occupation. This strategy typically leads as well to the reduction of the parasitic effects, which positively impacts transistor speed. However, these benefits might be obtained at the expenses of a lower device yield. Therefore, a trade-off between integration density/speed and yield performance is typically observed.

For these reasons, the formalization of the design rules has a crucial role in the development of the PDK. In this perspective, a reduced set of technological constraints C are used here to derive the design rules manual. The very same set of parameters is evaluated for each printed layer of the stack with the respect to the source/drain metal layers assumed here as reference.

1) C1 – Layer resolution: defined by the printing capability of the process. In gravure-printed process this value is related to the resolution of the engraved cells [2].

2) C2 – Layer registration: describes the capability of controlling the overlay during fabrication.

3) C3 – Pattern overflow: provides an estimation of ink displacement from the nominal feature definition.

4) C4 – Safety margin: this parameter is expressed in multiples of C1 and can be used to obtain more conservative design rules.

Similarly to the approach proposed in [17] the formalization of the design rules is further organized according to the three following categories:

1) Single-layer rules: define geometrical restrictions limited to shapes belonging to the same layer. Minimum width and minimum spacing rules (Fig. 5) are part of this category.

2) Two-layer rules: regulate the interaction between shapes placed on two different layers. Distance, overlap and enclosure rules (Fig. 5) belong to this group.

3) Multi-layer rules: are two-layer rules only valid within a restricted area, which is obtained as logical combination of several layers. Multi-layer rules are used to define transistors and Metal-Semiconductor-Insulator-Metal (MSIM) capacitors.

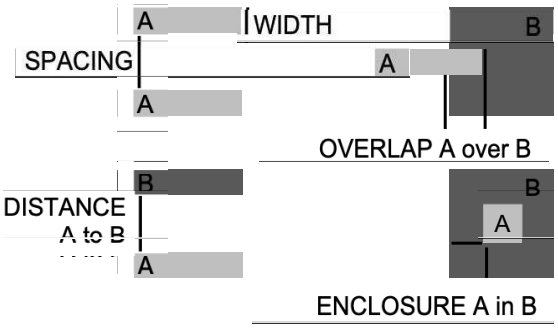

Fig. 5 : Set of geometrical restrictions used to define design rules.

E. Parametrized Cells (PCells)

Parametrized cells have been designed to automatically generate the layout geometry of resistors, capacitors and transistors according to a set of given parameters. This facilitates the design process during the layout stage, reducing the development time and the risk of design rule violations. Furthermore, the layouts of the PCells are fully adaptive with respect to the C1-C4 parameters. All the PCells have been integrated in the CAD framework with SKILL® scripts.

The high-resolution photolithography process used to develop the source/drain metal layer can be exploited for the fabrication of resistors with compact footprints. However, only resistance values in the order of kΩ can be achieved with reasonable yield, due to the relatively low sheet resistance of the layer (~1Ω/sq). The proposed PCell enables the generation of a serpentine fashion layout according to four parameters: resistance value, segment width W_R, length L_R and spacing S_R. Metal-Insulator-Metal (MIM) capacitors can be obtained from the overlap of the two metal layers. Metal-Semiconductor-Insulator-Metal (MSIM) non-linear capacitors are also available. The PCells enable the automatic generation of the layout geometry, given the nominal capacitance value. The OTFT layout, finally, is parametrized according to the channel size (W and L) and the number of fingers NF.

F. Design Rule Checking (DRC)

The DRC is an interactive EDA tool used to automatically highlight potential violations of the design rules at the circuit layout stage. The proposed PDK exploits the design rule checker provided in the DIVA® software, part of the Cadence® framework. However, the verifications rule file is here required. This has been created by implementing in SKILL® language the design rules already formalized in the DRM.

G. Layout Versus Schematic (LVS)

The Layout Versus Schematic tool provided in the DIVA® software, has been utilized here for logic comparison between netlists. Given the schematic and layout netlists, the program provides the results of the comparison, according to the directives specified in the LVS rules file. For the scope of the proposed PDK, several features have been included in this file.

The logical matching of the two netlists is not sufficient to prevent errors in the layout design phase. Indeed, device

properties must be also checked. This is applied here only on devices such as resistors, capacitors and transistors, for which their respective parameters (resistance, capacitance, W and L) are compared. In case of parameter mismatch between the netlists, a warning message is provided. During the layout phase the use of the series/parallel interconnection of multiple instances of the same device could be preferred to the placement of a single equivalent components. However, if the same approach is not adopted in the schematic, the netlist comparison fails. A specific functionality has been implemented here to reduce multiple interconnected instances (resistors, capacitors and OTFTs) into a single equivalent component in which the related parameters (Resistance, capacitance, W and L) are adjusted accordingly.

Before an LVS comparison can take place, both the schematic and layout netlists need to be generated. While the former can be automatically generated from the circuit schematic, the latter needs to be extracted from the layout. In order to enable this, a specific EXT rule file has been developed and provided to the software.

H. Layout Parasitic Extraction

The layout parasitic extraction is performed using the LPE and PRE tools, also provided by DIVA®. Similarly to the layout netlist extraction procedure, an additional rule file is here required. The devices defined in the layout with intentional masks (on the virtual layers) are not recognized as potential parasitics and therefore extracted as regular components. A parasitic capacitor is instead extracted each time that an overlap between the two metal layers occurs. The capacitance value is estimated as $A_{OV}\,C_i$, where A_{OV} is the area of the overlap and C_i the capacitance per unit area. Fringing effects are neglected. Parasitic resistors account for the resistive effects introduced by the routing lines.

The availability of parasitic devices in the extracted netlist enables the possibility to perform post-layout simulations. Indeed, parasitic effects become more and more relevant as PE circuits are manufactured over larger areas.

III. PDK VALIDATION

The characterization of a single-ended Charge Sensitive Amplifier is used here to demonstrate the efficacy of the PDK. A CSA is often used for the readout of high impedance transducers such as piezoelectric sensors, pyroelectric sensors, and photodiodes, to give some examples. The possibility to integrate sensors and active frontend electronics on the same foil, both manufactured with organic materials, could enable inexpensive solutions for large-area sensing applications.

The proposed CSA architecture exploits an inverter-based single-ended amplifier as main gain stage and, a capacitive feedback network (Fig. 6). The pseudo-resistor R_{FB} is placed in parallel with the feedback capacitance C_{FB}=5pF, to provide a DC path for the input bias current avoiding saturation of the amplifier. This functionality is implemented with an OTFT biased in off-region, which allows also tuning the dominant pole of the CSA. For the correct functionality of the CSA, a high gain amplifier is typically required. However, high-gain amplifiers with unipolar transistor only are challenging to design, due the lack of the complementary device. The core of the amplifier proposed in this work, makes use of the architecture described in [2] to achieve impedance boosting of the output transistor. An additional inverter (M1-M2) is introduced at the input of the amplification chain. This separates the Miller capacitance of the main gain stage from the input of the amplifier, allowing the use of a broader range of feedback capacitance values, and thus increasing the versatility of the CSA. In addition, the inverter further improves the DC gain of the amplification chain.

In order to use the amplifier in a closed-loop configuration with the pseudo-resistor without loading the output stage, matching of the DC input-output bias points must be guaranteed. The main amplification stage, intrinsically provides this feature [2]. Therefore, only the aspect ratios of the transistors M1-M2 must be designed to ensure DC compatibility between input and output. Finally, the unity–gain inverter (M9-M10) is used as output buffer stage, to decouple the CSA from the measurement setup.

The circuit performance has been evaluated by means of simulations, performed using the transistor model implemented in the PDK. Next, the circuit has been laid-out (Fig. 7(a)) exploiting the device PCells and according to the design rules of the technology. DRC, LVS comparison and post-layout simulations have been used to validate the design. The designed CSA has been successfully fabricated (Fig. 7(b)) and experimentally characterized.

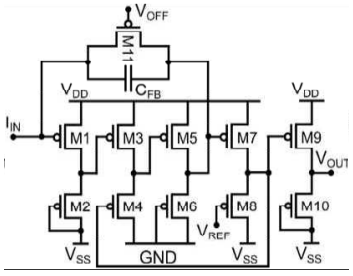

Fig. 6: Transistor-level schematic of the proposed Charge Sensing Amplifier.

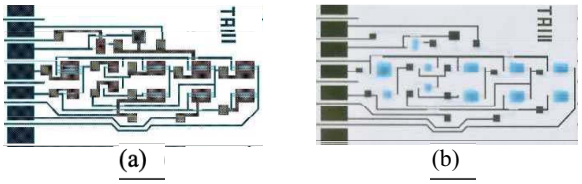

Fig. 7 : (a) Layout of the designed CSA. (b) Micrograph of the printed circuit.

The frequency response of the CSA has been measured by means of the HP35670 Dynamic Signal Analyzer. The source signal provided by the analyzer is fed to the circuit under test through a discrete series capacitance of C_I=69pF (Fig. 8(a)). This allows to measure the CSA as voltage amplifier, using the instrument. The frequency response of the CSA (H_{CSA}) shown in Fig. 8(b), can be derived from the transfer function measured in the voltage-amplifier configuration (H_{MEAS} - Fig. 8(a)), according to (11):

$$H_{CSA} \cong H_{MEAS} \cdot \frac{R_I}{j\omega C_I R_I + 1} \qquad (11)$$

Where R_I is the leakage resistance of the capacitor C_I. To perform the measurement, the output of the organic circuit is connected to a discrete Si voltage buffer amplifier, and then fed to the Dynamic Signal Analyzer. The comparison between the measured and simulated H_{MEAS} is presented in Fig. 9.

H_{MEAS} exhibits a band-pass behavior, with an in-band gain of 23 dB or 14.1 V/V. The upper and lower cut-off frequencies are at 28 Hz and 5 Hz, respectively. The simulation accurately reproduces the behavior of the circuit over a large span of frequencies. The estimation becomes less accurate at low frequency, due to the large variability associated to the pseudo-resistor.

A good agreement between the simulation and measurement results is obtained in the output spectrum provided in Fig. 10. This result further proves the effectiveness of the transistor model implemented in the PDK. This measurement shows a Signal-to-Noise-Ratio (SNR) of 25.7 dB in the bandwidth 5 Hz - 28 Hz, obtained with a current consumption of 17µA. In terms of linearity performance, the CSA achieves a Spurious-Free Dynamic Range (SFDR) of 22dB.

The circuit requires a dual supply voltage of ±15 V, and two additional bias voltages V_{REF}=-7.5 V and V_{OFF}=13 V to control the pseudo-resistor.

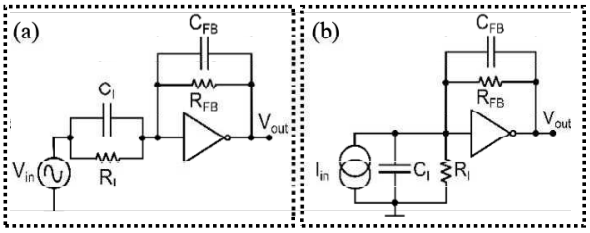

Fig. 8: (a) Proposed approach for the characterization of the CSA as voltage amplifier. (b) Typical application scenario of the CSA with an input current source.

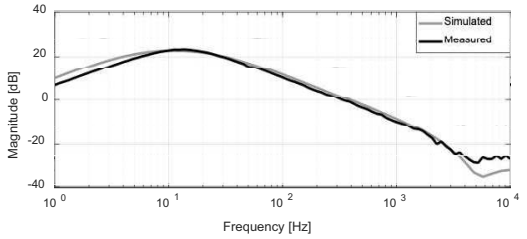

Fig. 9 : Measured (black) and simulated (gray) H_{MEAS} frequency response.

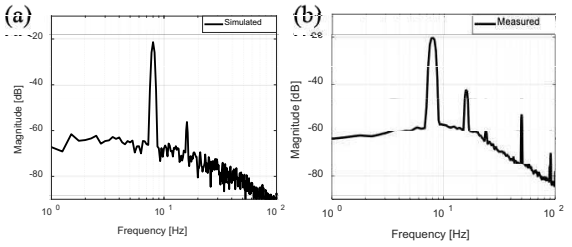

Fig. 10 : Simulated (a) and measured (b) output spectral performance of the CSA with an input 5mV_{RMS} sine wave signal at the frequency of 8Hz. Both FFT feature a frequency resolution of 0.25 Hz.

IV. Conclusions

In this work we have developed a PDK specifically suited for a gravure-printed organic technology. An accurate model capable to reproduce static, dynamic and noise behaviour of the transistors has been included. A new approach based on the use of 4 technological parameters is proposed for the design rule formalisations. This further enables a rapid adaptation of the PDK to the advancements of the manufacturing process including future device downscaling. PCells have been developed to automatically generate the layout of transistors, capacitors and resistors. The PDK has been integrated in Cadence Virtuoso®. In addition, design rule checking, layout versus schematic comparison and layout parasitic extraction functionalities have been also added using the DIVA® EDA tools. Finally, the efficacy of the PDK has been demonstated with the design and the charaterisation of a charge sensitive amplifier.

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