Process Design Kit and Design Automation for Flexible Hybrid Electronics

Tsung-Ching Huang*, Ting Lei†¶, Leilai Shao‡, Sridhar Sivapurapu§, Madhavan Swaminathan§, Sicheng Li*, Zhenan Bao†, Kwang-Ting Cheng‡‖, Raymond Beausoleil*
*Hewlett Packard Labs, Palo Alto, USA
†Department of Chemical Engineering, Stanford University, USA
‡Department of Electrical and Computer Engineering, University of California, Santa Barbara, USA
§School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA
¶Department of Materials Science and Engineering, Peking University, Beijing, China
‖Department of Electric and Computer Engineering, The Hong Kong University of Science and Technology, China

***Abstract*—High-performance low-cost flexible hybrid electronics (FHE) are desirable for internet of things (IoT). Carbon-nanotube (CNT) thin-film transistor (TFT) is a promising candidate for high-performance FHE because of its high carrier mobility (25cm$^2/V.s$), superior mechanical flexibility/stretchability, and material compatibility with low-cost printing and solution processes. Flexible sensors and peripheral CNT-TFT circuits, such as decoders, drivers and sense amplifiers, can be printed and integrated with thinned (<50μm) silicon chips on soft, thin, and flexible substrates for appealing product designs and form factors. Here we report: 1) process design kit (PDK) to enable FHE design automation, from device modeling to physical verification, and 2) open-source and solution-process proven intellectual property (IP) blocks, including *Pseudo-CMOS* [1] digital logic and analog amplifiers on flexible substrates, as shown in Figure 1. The proposed FHE-PDK and circuit design IP are fully compatible with silicon design EDA tools, and can be readily used for co-design with both CNT-TFT circuits and silicon chips.**

***Index Terms*—Flexible hybrid electronics, thin-film transistors, carbon-nanotube, thinned silicon chips**

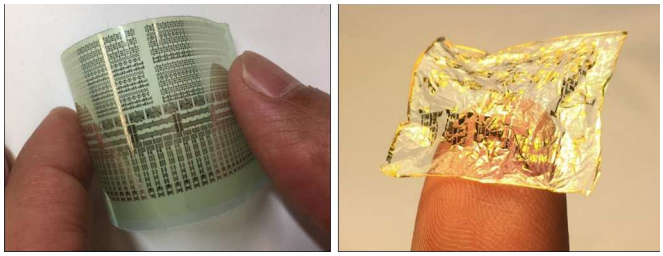

Fig. 1: Open-source circuit design IP, including *Pseudo-CMOS* [1] digital logic, analog amplifies, and passive elements. (Left) solution-processed circuit design IP blocks on a 10μm flexible substrate for bending test, and (right) design IP blocks on a 1μm flexible substrate.

I. Introduction

Flexible and printable TFTs have exponential growth in performance and cost reduction in recent years, which enables new applications such as disposable sensors, RFID tags, and low-cost internet of things (IoT) [2], [3]. To design a large-scale (>1,000 transistor count) TFT circuitry that is manufacturable with low-cost printing or solution processes, however, is another story. Due to large printing process variations as well as the lack of complementary and reliable TFTs, large-scale TFT circuits often suffer from higher power consumption and low circuit yields, particularly in low supply voltages. These limitations make TFT circuits targeting IoT or wearable applications a significant challenge.

On the other hand, the hybrid-integration of thinned silicon chips and printable TFTs on the same flexible substrate emerges as a viable solution. The printable sensors and TFT circuits that benefit from low manufacturing cost and conformal form factors can be an ideal complement to rigid silicon chips for designing a flexible IoT or wearable device. We have previously reported our progress of developing FHE-PDK and simple circuits with CNT-TFTs [4], [5]. We imagine that an ideal FHE-PDK should include: 1) simulation models of printable passive and active devices, such as TFTs, resistors, inductors, and capacitors, 2) design rules of printable devices given the limitations of specific printing or solution process capability, 3) multi-physics simulation models that can capture the interaction among electrical-thermal-mechanical performance, and 4) co-design capability with silicon chips, ideally using the same design environment or EDA tools.

Based on these requirements, in this paper, we report the following progress regarding FHE-PDK: i) simulation models of TFTs, CNT resistors, and parallel-plate capacitors as shown in Figure 2, ii) physical design verification capability, including design rule checking (DRC), layout-versus-schematics (LVS) checking, and layout-parasitics extraction (LPE), based on design rules and material properties derived from solution-processed test samples, and iii) low-voltage (3V) operable open-source circuit design IP. The technologies files, simulation models (SPICE and Verilog-A), and parameterized cells (p-cell) are based on mainstream EDA tools for silicon design, which makes FHE-PDK fully capable of co-design, co-simulate, and co-verify the FHE design using both TFTs and silicon chips.

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TABLE I: Comparison between different TFT technologies

Device Type (TFT)	Amorphous Si	Metal-Oxide	SAM Organic	Polymer Organic	Carbon Nanotube
Process Temperature	$\sim 250°C$	$\sim 150°C$	$\sim 100°C$	Room temperature	Room temperature
Process Technology	Lithography	Roll-to-roll	Shadow mask	Ink-jet	Lithography & shadow mask & roll-to-roll
Feature Size (μm)	8	5	50	50	25
Substrates	Glass/foil	Glass/foil	Foil	Foil	Foil
Device Type	N-type only	N-type only	Complementary	Complementary	Complementary
Supply Voltage (V)	20	10	2	40	3
Mobility (cm^2/Vs)	1	10	0.5	0.05	25

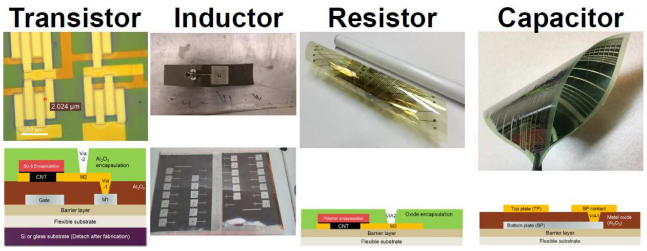

Fig. 2: The printed or solution-processed active and passive elements on flexible substrates, including CNT-TFTs, inductors, resistors, and capacitors.

II. Device Modeling

Several TFT compact models targeting specific technologies [6] have been developed in the past, which may not be generalized for other technologies. Some studies focus only on modeling the DC behavior [7], which doesn't support transient simulations. In this paper, we present a unified compact model of TFTs covering DC, AC and technology scaling factor for supporting FHE design, and validate the model using three TFT technologies: carbon-nanotube (CNT) TFTs, indium-gallium-zinc-oxide (IGZO) TFTs and organic TFTs. The comparison of TFT technologies is listed in Table I. Based on this model, we further perform circuit level validation based on fabricated *Pseudo-CMOS* inverters, sequence generators and ring-oscillators. The proposed model is implemented in Verilog-A, which is compatible with SPICE simulation with silicon CMOS circuitry, thus enables FHE designers to explore TFT based flexible hybrid circuits and evaluate their performance [8].

A. Compact TFT Models

To investigate the effective mobility of fabricated TFTs, we observed that the effective mobility μ_{eff} is enhanced as the $|V_{GS}|$ increases for both CNT-TFT and IGZO-TFT, when $|V_{GS}|$ is relative small [8]. Similar mobility dependency phenomenon has been observed in OTFT and a-Si TFT [6], and the commonly accepted theories are based on charge drift in the presence of tail-distributed traps (TDTs) and variable range hopping (VRH) [6]. This common phenomenon among different TFT technologies encourages us to build a unified model to capture fundamental behaviors of different TFTs based on TDTs and VRH assumptions.

1) Mobility Enhancement: Both theories indicate the field enhancement of the mobility :

$$\mu = \begin{cases} \mu_0(V_G - V_{th})^{\gamma}, & \text{N-type TFT} \\ \mu_0(V_{th} - V_G)^{\gamma}, & \text{P-type TFT} \end{cases} \quad (1)$$

, where V_{th} is the threshold voltage, γ is the field enhancement factor for mobility and μ_0 is defined as the effective mobility when $|V_G - V_{th}| = 1$. This mobility enhancement assumption explains the increase of the effective mobility at a low $|V_{GS}|$.

2) Contact Effect: The degeneration of mobility at high $|V_{GS}|$ can be explained partially by the contact resistance R_S and R_D at source/drain terminals. These resistances result in effective gate-source/drain-source voltage drops: $\tilde{V}_{GS} = V_{GS} - R_S\tilde{I}_{DS}$, $\tilde{V}_{DS} = V_{DS} - (R_S + R_D)\tilde{I}_{DS} = V_{DS} - R_C\tilde{I}_{DS}$, where $R_C = R_S + R_D$ and the current with contact effect is denoted as $\tilde{I}_{DS}$. The derivations are not presented here for simplicity and the contact effect can be illustrated as follows:

$$\tilde{I}_{DS} \approx \frac{WC_{ox}\mu}{L\{1 + kR_C(V_{GS} - V_{th})\}}\{(V_{GS} - V_{th}) - \frac{1}{2}V_{DS}\}V_{DS} \quad (2)$$

$$\frac{\tilde{I}_{DS}}{I_{DS}} \approx \frac{\tilde{\mu}}{\mu} = \frac{1}{1 + kR_C(V_{GS} - V_{th})};\ k = \frac{W}{L}C_{ox}\mu \quad (3)$$

We can conclude that contact resistances lead to mobility reduction with a factor of $1/(1 + kR_C(V_{GS} - V_{th}))$ and it becomes more significant as $|V_{GS}|$ increases, which explains the degeneration of the effective mobility with a high $|V_{GS}|$. CNT-TFT has relative larger k comparing to IGZO-TFT $k_{CNT} \approx 25k_{IGZO}$, thus leading to more obvious mobility degeneration [8].

3) Surface Roughness Effect: As gate voltage increases, electrons tend to flow closer the channel surface. Due to the low-cost fabrication process of TFTs, interface traps and surface roughness lead to degeneration of the effective mobility [9]:

$$\frac{\tilde{\mu}}{\mu} = \frac{1}{1 + \theta(V_{GS} - V_{th})}; \quad (4)$$

Here, $\theta \propto 1/t_{ox}$ is a parameter related to the thickness of the gate oxide. This phenomenon combining with the contact effect leads to an overall mobility drop with a factor of $\approx 1/(1 + (\theta + kR_C)(V_{GS} - V_{th}))$. Although, surface roughness and contact effect have identical formula with a term $V_{GS} - V_{th}$, their physical explanations are different. The experimentally-extracted model parameters for CNT, IGZO, and organic TFTs are shown in Table II. More details regarding the unified TFT model can be found in [8].

TABLE II: Extracted parameters for CNT, IGZO and Organic TFTs

Notation (Unit)	CNT-TFT [μ, σ]	IGZO-TFT [μ]	OTFT [μ]
L (um)	[25, -]	20	10
W (um)	[125, -]	30	5000
L_{ov} (um)	[10, -]	10	20
C_{ox} (nF/cm^2)	[200, -]	70	15
V_{th} (V)	[0.5, 0.102]	1.9	-4.2
SS (V/dec)	[0.28, 0.0388]	0.8	0.6
μ_0 (cm^2/Vs)	[25.69, 0.19]	1.6	0.02
R_C (Ω)	[1531, 291]	2500	80000
λ (V^{-1})	[0.064, 0.0185]	0.002	0.028
γ (-)	[0.20, 0.116]	0.3	0.5
θ (V^{-1})	[0.01, 0.002]	0.005	0.002

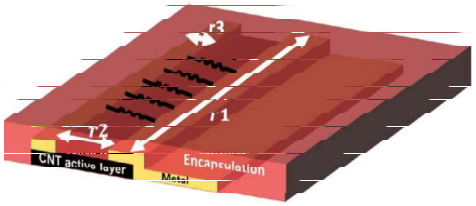

Fig. 3: Conceptual representation of a CNT resistor using width (r1) and legnth (r2) to define the resistance.

Field effect mobility extracted based on an idealized MOSFET current model has been widely used for TFT performance benchmarking. With the field-dependent properties, the extracted mobility could vary significantly at different effective gate voltages. Therefore, to better evaluate the TFT performance, the combination of the low field effect mobility (μ_0) and the field-dependent factor (γ) should be used. In this way, the unified compact model can enable accurate SPICE simulations for TFT technology and design benchmarking [8].

B. Resistor Models

In addition to TFTs, the CNT film can also be used to realize a linear resistor and the manufacturing process of a CNT resistor is fully compatible with CNT-TFTs. The CNT resistors have a wide range of applications such as linear and transimpedance amplifiers. Figure 4 shows the

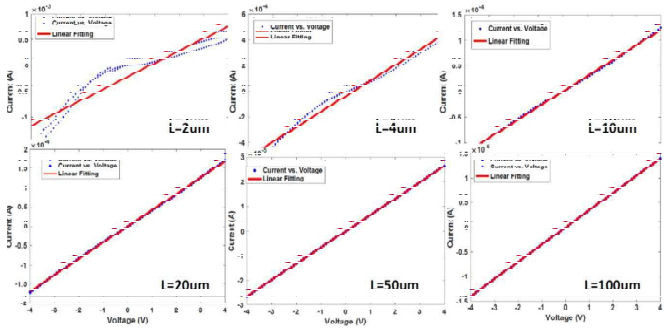

Fig. 4: Measured I-V curves (blue dot) of CNT resistors against linear fitting (red line) for resistor length from 2μm to 100μm and the width is 40μm.

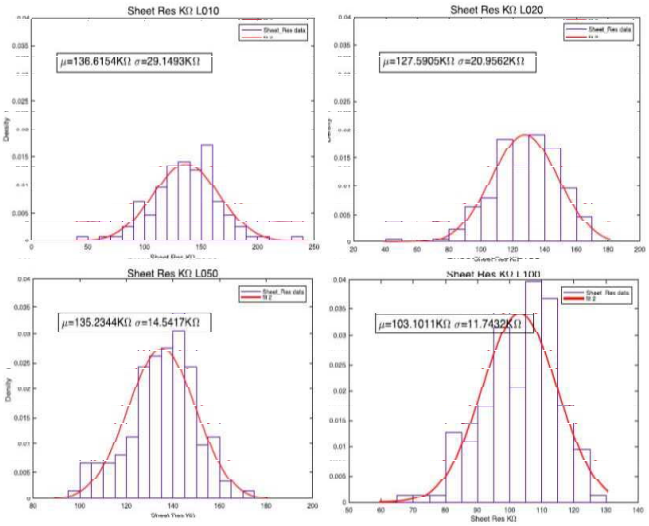

Fig. 5: Measured statistical histograms of CNT resistors for resistor length from 10μm to 100μm and the width is 40μm.

conceptual representation of a CNT resistor structure. The resistance is determined by the width r1 and the length r2. $R = \rho * r2/r1$, where R is the resistance and ρ is the sheet resistance ≈135KΩ. To further study the CNT resistor linearity and process variations, we fabricated and characterized 864 CNT resistors on a flexible substrate shown in Figure 2. With 40μm resistor width, the length is varied from 2μm to 100μm and the measurement results are shown in Figure 4. We can learn that the CNT resistors show a good linearity when the length is greater than 10μm, when compared against a linear fitting curve. Figure 5 further reveals the process variations of the CNT resistors, where 96 test samples are included for each case of the resistor lengths 10μm, 50μm, and 100μm, and 384 samples are included for the case of the length 20μm. While the histograms follow Gaussian distributions, we can learn that the standard variations σ reduces when the resistor length increases. For the resistor modeling, as shown in Fig. 6, the parasitic capacitance and inductance are not included for simplicity. The resistor model contains both the intrinsic resistance as well as the contact resistance between the CNT film and the contact metal. Thus the total resistance R_{total} includes the contact resistance $R_c = R_{cs} + R_{cd}$ for two terminals and the channel resistance R_{ch}. Here, R_{ch} is the sheet resistance of the channel.

$$R_{toal} = \frac{R_c}{W} + \frac{R_{ch}L}{W} \tag{5}$$

From Eq. (5), we can see that the R_{total} is a linear function versus the resistor length L while keeping the resistor width W as a constant. The $R_c/W = 11.6K\Omega$ is the intersection when $L = 0$ and $R_{ch}/W = 2.46K\Omega$ is the slope of the linear fitting curve, as illustrated in Fig. 6.

C. Capacitor Models

In addition to CNT resistors, flexible capacitors can also be realized using CNT-TFT compatible solution process for

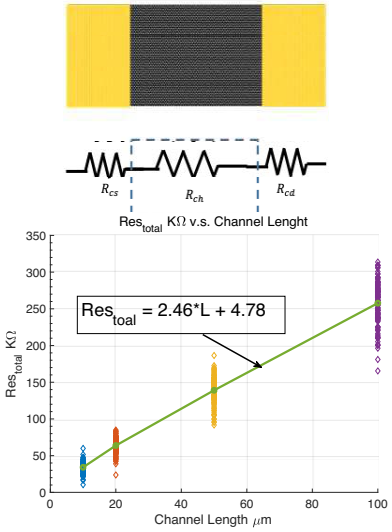

Fig. 6: Measured CNT resistor characteristics against various resistor lengths of 10μm, 20μm, 50μm, and 100μm. The channel width is 40μm.

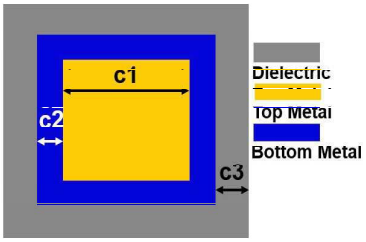

Fig. 7: Conceptual representation of a parallel-plate capacitor using the width (c1) of the top-plate metal to define the capacitance.

applications such as ac-coupled amplifiers or low-pass filters. We use simple parallel-plate top and bottom metals to realize the flexible capacitors as shown in Figure 7, where the width c1 of the top metal is used to define the capacitance and the Al_2O_3 dielectrics thickness is 25nm. To further study the process variations of the capacitance, we designed and characterized 431 parallel-pate capacitors as shown in Figure 2 and the measurement results can be found in Figure 8 for the capacitor width c1 from 45μm to 1415μm. We can learn that while the standard variations σ of the unit capacitance (fF/μm^2) are similar for different capacitor widths, the average unit capacitance decreases with a larger width. We suppose that this phenomenon is due to thinner dielectrics for larger-sized capacitors. The 2D spatial analysis in Figure 9 shows the unit capacitance variations across the same flexible substrate, with which figure we can learn that the unit capacitance is higher at the center of the substrate. This could be attributed to the thinner dielectrics at the center. An equivalent model of a parallel-plate capacitor can be found in Figure 10. The experimentally-extracted values of the series resistance

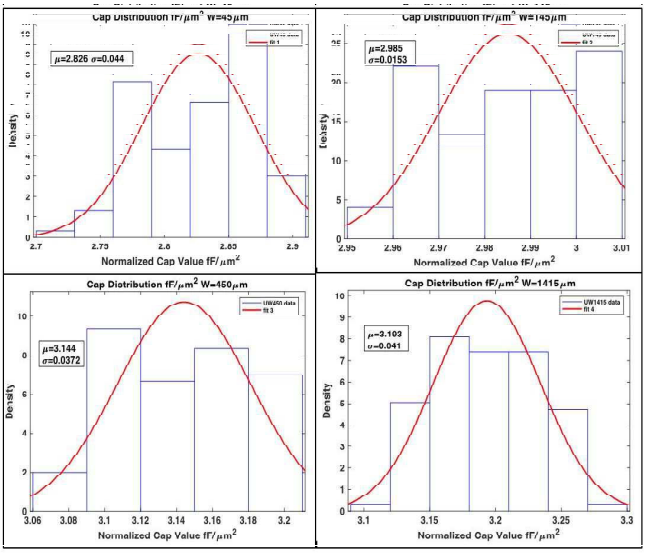

Fig. 8: Measured statistical histograms of the unit capacitance (fF/μm^2) for the capacitor width c1 from 45μm to 445μm.

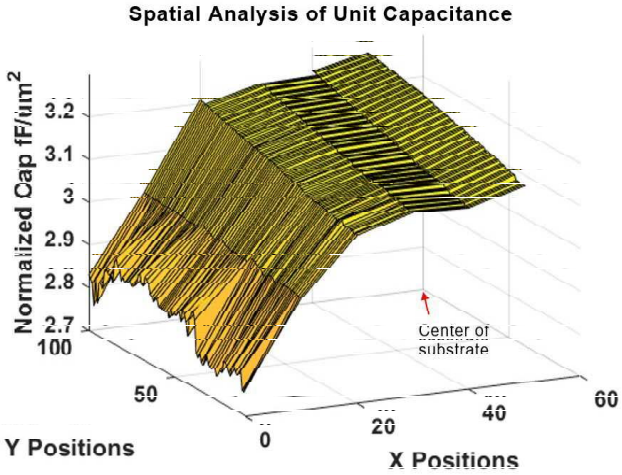

Fig. 9: Measured 2D spatial analysis of the unit capacitance (fF/μm^2) against the substrate dimensions in millimeter (mm).

R_s is around 1.5Ω and the parallel resistance R_p is around 1MΩ. The intrinsic capacitance can be defined as $C_{intrinsic} = C_{unit} * W^2$, where C_{unit} is the unit capacitance around 3 fF/μm^2 and W represents the capacitance width.

III. Physical Design Verification

To enhance the productivity of FHE circuit design, we incorporate mainstream EDA tools for FHE-PDK design verification and create experimentally-proven design rules of CNT-TFTs, CNT resistors, and parallel-plate capacitors, inductors etc using printing or solution processes. Based on these design rules, we create technology files using Standard Verification Rule Format (SVRF), T-cl or Python based formats to perform

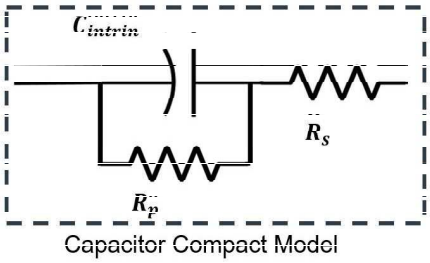

Fig. 10: Equivalent model of a parallel-pate capacitor. R_s is the series resistance due to thin electrode (40nm thick) and through-layer VIAs. The R_p is the parallel resistance due to Al_2O_3 dielectrics.

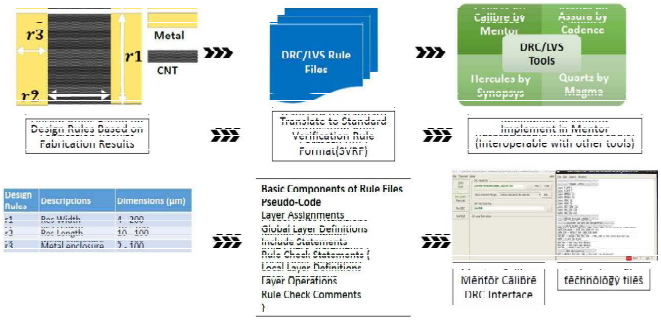

Fig. 11: The physical design verification flow (ex. DRC) for a CNT resistor based on experimentally-derived design rules.

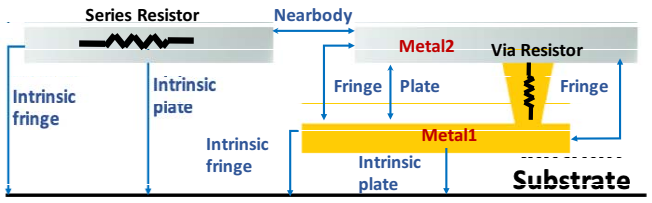

Fig. 12: Different types of parasitic capacitors and resistors

physical verification with mainstream EDA tools such as *Mentor Graphics Calibre*. The physical design verification flow (ex. DRC) is illustrated in Figure 11.

In addition to physical design verification, we also incorporate material properties to create technology files for layout-parasitics extraction (LPE). Layout-related parasitics in flexible circuits can be significant compared with silicon chips, which is due to larger physical footprints. Thus, it is essential to include accurate estimates of layout-related parasitics for post-layout simulations, particularly for high-performance FHE circuits. As shown in Fig. 12, the parasitic capacitance including intrinsic and fringe capacitance can be derived using the mainstream LPE tools with the knowledge of material properties such as dielectric constants and dielectrics thickness etc, as well as the physical design information. Parasitic resistors are mainly attributed to metal layers as well as the layer-to-layer VIAs. After the parasitics extraction and back-annotation to the circuit netlist, post-layout simulations can be performed to include the layout-dependent parasitics for flexible circuits.

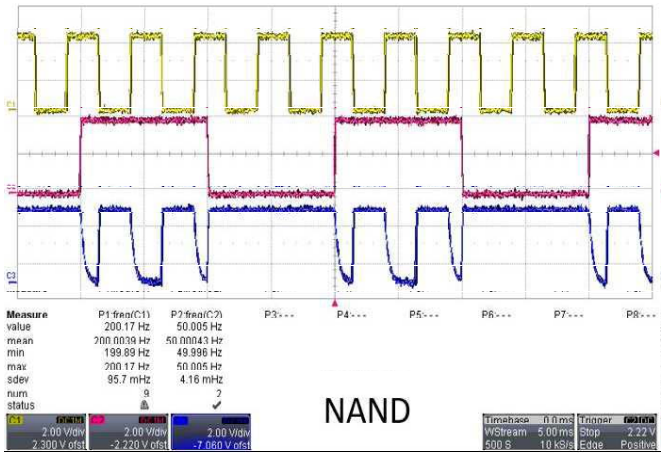

Fig. 13: Measured waveforms of a *Pseudo-CMOS* NAND logic gate. Top and middle rows are input signals and the bottom row is the output signal.

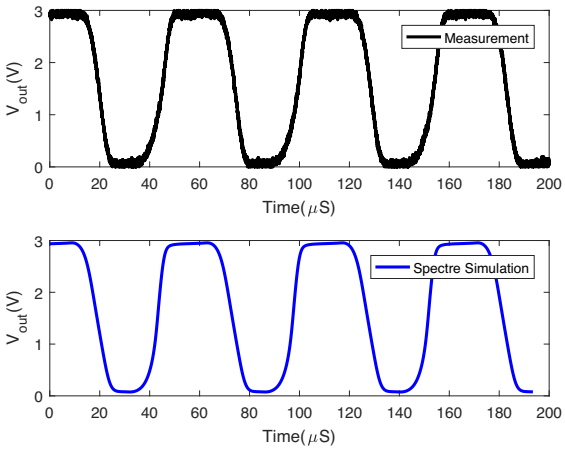

Fig. 14: (Top) Measured waveforms of a *Pseudo-CMOS* ring-oscillator, and (bottom) simulated waveforms of the same ring oscillator using proposed CNT-TFT compact models [8].

IV. Open-Source Circuit Design IP

A. Digital Logic

To overcome the design challenges such as the lack of complementary reliable TFTs as well as large process variations for printed and solution-processed TFT circuits, we have previously reported a robust design style *Pseudo-CMOS* [1]. Based on *Pseudo-CMOS*, we have developed a variety of solution-process proven digital logic circuit IP blocks ranging from a simple inverter, NAND gate (Figure 13), ring oscillators (Figure 14), to shifter registers using CNT-TFTs. With the aid of FHE-PDK, we can now design, simulate, and verify a TFT digital circuit block with hundreds to thousands of

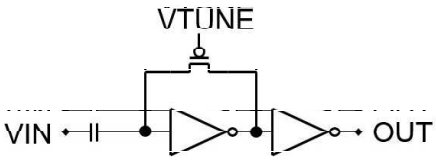

Fig. 15: Schematics of a 9T-1C (9 CNT-TFTs and 1 capacitor) tunable-gain amplifier based on *Pseudo-CMOS* inverters. The total physical size of 350x350 μm^2 and the voltage gain can be adjusted with *VTUNE*.

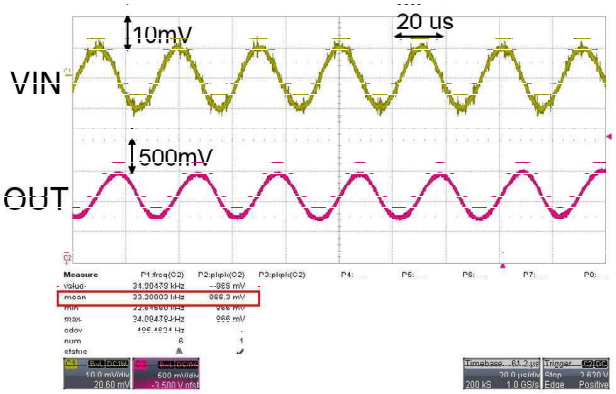

Fig. 16: Measured waveforms of a 9T-1C *Pseudo-CMOS* amplifier based on solution-processed CNT-TFTs.

CNT-TFTs within a short period of time. The simulated CNT-TFT circuit performance and power-consumption also provide a good correlation with the fabricated CNT-TFT circuits. The open-source digital circuit IP blocks are experimentally-proven to be operable at low supply voltages (3V). This benefit can ease the FHE power circuit design for supplying both CNT-TFT circuits and silicon chips on the same substrate.

B. Analog Blocks

In addition to digital TFT logic circuits, we have also developed key analog building blocks for FHE-PDK users, such as a 9T-1C tunable-gain amplifier as shown in Figure 15. The voltage gain can be tuned by varying the gate-bias voltages *VTUNE* of the feedback CNT-TFT. The physical size of the 9T-1C amplifier is only 350x350 μm^2. The input capacitor is used to attenuate low-frequency input noises and block the dc feedback to the input terminal. The measured waveforms can be found in Figure 16 with 32.7dB gain at 33.2 KHz. The input capacitor can also be replaced with a CNT resistor for signal amplification on low-frequency inputs.

V. Conclusion

In this paper, we report our progress in developing a PDK for FHE design and verification. While FHE is emerging as a viable solution for high-performance low-cost IoT and wearable applications, the device models, design rules, and technology files are still missing to enable the co-design and co-simulations of flexible TFT circuits and thinned silicon chips. FHE-PDK fills these gaps by providing open-source device models, design rules, technology files, and circuit design IP blocks. We also benefit from using FHE-PDK to design a variety of digital and analog circuit IP blocks with a good confidence of the fabrication results, using printing or solution processes. We believe that the proposed FHE-PDK will be the must-have toolbox for FHE designers.

VI. Acknowledgment

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