Predictive Modeling and Design Automation of Inorganic Printed Electronics

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***Abstract*—Printed Electronics is perceived to have a major impact in the fields of smart sensors, Internet of Things and wearables. Especially low power printed technologies such as electrolyte gated field effect transistors (EGFETs) using solution-processed inorganic materials and inkjet printing are very promising in such application domains. In this paper, we discuss a modeling approach to describe the variations of printed devices. Incorporating these models and design flows into our previously developed printed design system allows for robust circuit design. Additionally, we propose a reliability-aware routing solution for printed electronics technology based on the technology constraints in printing crossovers. The proposed methodology was validated on multiple benchmark circuits and can be easily integrated with the design automation tools-set.**

***Index Terms*—Additive manufacturing technology, printed electronics, process design kit, variability modeling and routing**

I. Introduction

Trends like ubiquitous electronics require new forms of emerging electronics, many of them being flexible, wearable, transparent and costumizable [1]. Printed electronics holds many of these attributes and hence, is suitable for sensors, Internet of things, smart homes and soft robotics [2], [3]. Especially the low voltage operation capabilities of electrolyte-gated field effect transistor (EGFET) technology based on inorganic material renders it as a very attractive low power technology. EGFETs are developed by replacing the conventional dielectric with an electrolyte which enable them to operate at extremely low-voltages [4].

As most of the attention has been on materials, processes, and devices [5], the standard design flow for inkjet printed electronics technology is currently missing. Additionally, the existing design and automation tools for very-large-scale integration (VLSI) technology need to be modified to support printed electronics process technologies [6]–[9]. However, due to the technology-specific design constraints, a common design flow cannot be followed for all printed electronics technologies.

The inkjet printed electronics technology is a highly customizable process due to its additive-manufacturing feature and drop-on-demand printing. The devices are printed one-by-one where each step of printing vary on its own. This discrete

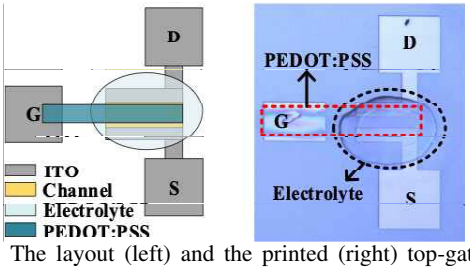

Figure 1: The layout (left) and the printed (right) top-gate EGFET with channel width $W = 200\mu m$ and length $L = 40\mu m$.

printing of devices introduces variability in the electrical characteristics of the devices [5]. Unlike VLSI technologies, where variations are divided in local and global variations, the variation in this technology cannot be naturally divided. These variations should be integrated in the design kit, as a statistical model, to run the variation analysis during the design phase of printed circuits. Due to the additive-manufacturing process, the printed electronics technologies have limited printed metal layers. Unlike VLSI technologies, they are electrically isolated only at the points where the crossover is printed. However, the reliability issues associated with crossovers and increased resistance on the top net, make it challenging to design complex circuits. An efficient reliability-aware placement and routing methodology is required for printed circuits which is missing from the current design flow.

In this paper, we discuss the design flow for EGFET-based additive printed technology. We first discuss how the impacts of variations can automatically be included in the device models based on the empirical measurements. Then, we present physical design techniques for this printed technology, and in particular, we present a reliability-aware routing methodology. The genetic algorithm is used to propose the routing sequence to minimize the number and impact of crossovers on the printed circuit. The routing methodology is validated on multiple benchmark circuits and compared with the industrial standard routing tool.

The rest of the paper is organized as follows. The Section II discusses the design flow for inkjet printed electronics technology and variability models for printed transistors. In Section III, the reliability-aware routing solution is discussed in detail followed by the results for benchmark circuits. Finally

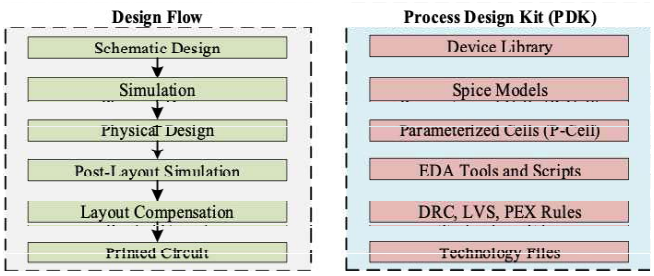

Figure 2: The design flow for printed electronics technology with process design kit components.

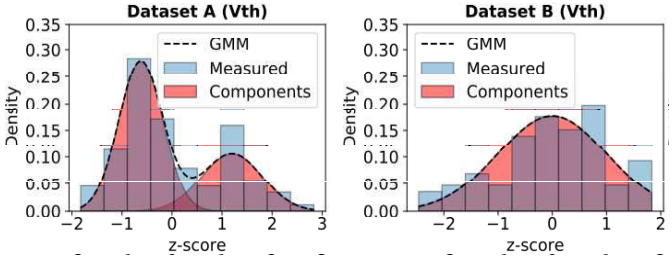

Figure 3: The threshold voltage (V_{th}) z-score distribution estimated using the GMM (a) Dataset A (95 samples) approximated with two gaussian components and (b) Dataset B (88 samples) with a single gaussian component.

the conclusion and future research directions are discussed in Section IV.

II. Inkjet Printed Electronics Design Flow

A. Electrolyte-Gated Field-Effect Transistors (EGFETs)

The EGFETs are developed by replacing the conventional gate dielectric with an electrolyte. The electrolyte-gating provides high-gate capacitance which allow EGFETs to operate at very low supply voltage (<1V) [4], [10]–[12]. The channel material is made of solution processed inorganic oxide semiconductor and finally PEDOT:PSS is used as the top-gate electrode. The layout and printed top-gate EGFET is shown in Figure 1. The EGFETs are prepared on a glass substrate by structuring indium tin oxide (ITO) using e-beam lithography. The indium oxide (In_2O_3) is printed as a channel material and annealed at $400\,^{\circ}\mathrm{C}$. Next, an electrolyte is printed as a dielectric followed by the PEDOT:PSS as a top-gate electrode. The inkjet printed electronics technology is based on customized additive process which lead to technology-specific novel ideas and applications [13]. Moreover, the low threshold voltage (<0.2V) and high field-effect mobility make the EGFETs based circuits suitable for the low-power and high-performance circuit applications.

B. Process Design Kit (PDK) for Printed Electronics

The Process Design Kit (PDK) plays a major role in scaling up the technology to the designers. It serves as a backbone of the design flow, for any process technology, as it provides a bridge between the circuit design and technology. PDK itself is divided into multiple components and has variety of data files. Such data files include physical layers definition, parameterized cells (p-cell), nominal, statistical models and process corner models, a standard cell library, rule decks for design rule check (DRC), layout-versus-schematic (LVS) and parasitic extraction (PEX). The general design flow for printed electronics technology is shown in Figure 2.

The design kit for inorganic inkjet printed electronics technology should be developed in such a way that is compatible with industrial standard design tools. The design kit has SPICE compatible models for the inkjet printed components [14], [15]. Additionally, the physical design components including p-cells, layers definition and design verification rules deck are integrated in it [16]. The p-cells are used to speed up the design process by automatically generating the layout for the devices. The master p-cell has fixed technology or design parameters but it can be accessed and modified during the design phase. The design verification rules deck are used to verify (through DRC) that the design can be printed and fabricated in a specific foundry. These rules restrict the user to be in a certain limit in terms of technology or design parameters. Furthermore, the rules for LVS and PEX are written to verify that the drawn layout is the exact representation of the schematic and to estimate the circuit performance after fabrication, respectively.

Developing the entire design flow for this printed technology is a major endeavor. In this paper, we focus on the activities related to variability modeling in the PDK and the reliability-aware routing. However, there are other important steps, such as placement and optimization of inkjet printed structures through proximity correction, which are in our future directions.

C. Variability-Aware Model for EGFETs

The accurate description of variability in printed components is complex because of the intrinsic properties of the inkjet printed electronics technology. There are multiple sources of variation for printed components which include dispersion of the ink on the substrate, droplet jetting oddness, satellite drops wetting and missing droplets [5]. All of these variations display themselves as non-Gaussian distribution of EGFET model parameters. Such non-Gaussian distribution cannot be estimated with the classical approach where single Gaussian is utilized to estimate model parameters. We proposed a variability modeling approach for printed transistors which is based on a Gaussian Mixture Model (GMM) [15], [17]. The proposed model is the extension of our EGFET DC model [14]. The drain current equation for the EGFET DC model is given by:

$$I_{DS} = I_0(\ln(f_3 + e^{\frac{v_p - v_s}{2}})^{\gamma} - \ln(f_3 + e^{\frac{v_p - v_d}{2}})^{\gamma}) \quad (1)$$

$$\text{where} \quad I_0 = 2nf_1\frac{W}{L}\phi_t^2 \quad v_p \approx \frac{V_{GS} - (V_{th} - f_4 V_{DS})}{\frac{n}{f_2}\phi_t}$$

$$\text{and} \quad n = \frac{1}{SS * \phi_t * ln(10)}$$

The parameters W and L represent channel width and length, respectively, and n is the slope factor. v_p, v_d, and v_s present channel, drain, and source potentials, which are normalized by the thermal voltage ϕ_t. The model has seven parameters, out of which threshold voltage (V_{th}), sub-threshold

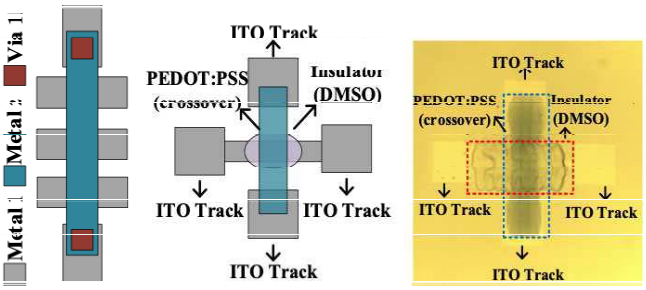

Figure 4: (a) Metal-2 utilization in routing in VLSI technology by placing a via between Metal-1 and Metal-2 (b) The layout of a typical crossover (c) An Inkjet printed crossover connecting the vertical ITO tracks.

slope (SS), and power-law parameter (γ) are empirically extracted from the measurement data of printed transistors. The rest of them are fitting parameters (f_1, f_2, f_3 and f_4).

The EGFET model parameters, that are subjected to variation, are extracted from the measurement data of two batches (Dataset A and B) of the printed transistors. A GMM utilizes a convex combination of K normal distributions ($\mathcal{N}$) and has three sets of parameters $\boldsymbol{\mu}$, $\boldsymbol{\Sigma}$ and $\boldsymbol{\alpha}$, which correspond to expected values, covariances and component weights, respectively. The parameter vectors μ_k and the matrices Σ_k represent the expected value and the covariance matrix of a respective normal distribution. The number of components K is decided by indirect test error estimation using the Bayesian Information Criterion (BIC). As shown in Figure 3, the distribution of the V_{th} for dataset A is non-Gaussian (validated through normality test) while for the dataset B it is a distributed as Gaussian. The proposed method can model such distributions by utilizing multiple Gaussian components where required. The extracted GMM parameters are integrated in the EGFET DC model to run the Monte Carlo simulation for the EGFET based circuits.

III. Reliability-Aware Routing

A. Routing in Printed Electronics

In inkjet printed electronics, and other additive manufacturing technologies with limited (printed) metal layers, circuits with few printed components can be routed with a single metal layer (ITO in our case). However, routing for complex circuits require crossovers to be printed at the intersection of two different routing nets. The crossovers are printed by first printing an insulator, such as DMSO (dimethyl sulfoxide) on the bottom metal, e.g., ITO layer, which will electrically isolate it from the top metal-layer. Then, a conductor such as PEDOT:PSS is printed as a top metal-layer which acts as a crossover at the intersection of two routing nets. The typical crossover layout and a printed crossover are shown in Figure 4b and Figure 4c, respectively.

The crossover printing process involves multiple steps which may cause reliability issues or alter the electrical characteristics of the circuit. For example: the typical resistance of the ITO is lower than the PEDOT:PSS [18], [19] and the printing of crossovers increases the parasitic capacitance between the top and bottom metal-layers. Thus crossover

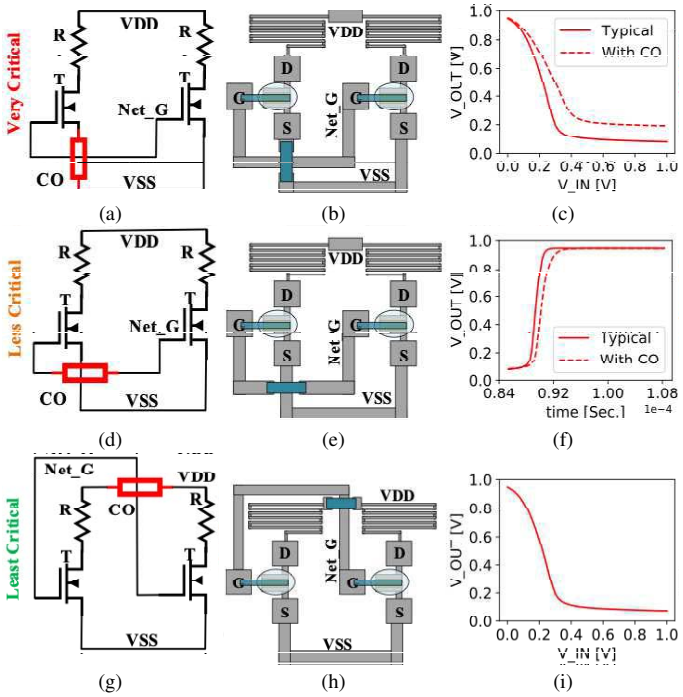

Figure 5: The schematic layout and the simulation for the conditions when the crossover is placed on a path that is connected to a source [(a), (b), (c)], gate [(d), (e), (f)] and resistor [(g), (h), (i)] terminal. The typical behavior in the simulation is the condition without considering the crossover (CO = Crossover).

introduces delay in the signal propagation. Additionally, the proper placement of crossover in a logic circuit is crucial.

There are three different conditions under which the crossover can influence the behavior of the logic circuit. If the crossover is between the source terminal and the ground (VSS) net (as shown in Figure 5a), it behaves as an additional passive component in the logic cell. The voltage drop on crossover would shift the V_{GS} of the transistor and the output logic cannot be completely pulled-down ($V_{OUT} \approx 200\ mV$) (Figure 5c). Thus, any subsequent logic stage would turn on, as $200\ mV > V_{th}$ of the EGFET, and lead to failure of the circuit. This is the most critical situation for the crossover placement. On the other hand, if the crossover is on the path where gate pins are connected, it would introduce extra delay in the signal propagation. The schematic, layout and the transient simulation for this configuration are shown in Figure 5d, 5e and 5f, respectively. However, a crossover on a path where resistor pins are connected (shown in Figure 5g) is not a critical condition as the crossover resistance can be compensated by (subtracted from) the pull-up resistor. Due to such physical design constraints, a reliability-aware routing solution is required for the printed electronics technology.

In general, the routing algorithm involves three steps [20]. In the first step the nets are routed one by one based on their criticality. In the second step, rip-up and re-route methodology is applied to the nets that are failed to route. This process is repeated until all nets are routed. Finally, inefficiencies from the second step are removed by ripping-up and re-routing all nets in the sequence that lead to the successful routing of all nets. In printed electronics technologies the metal layers

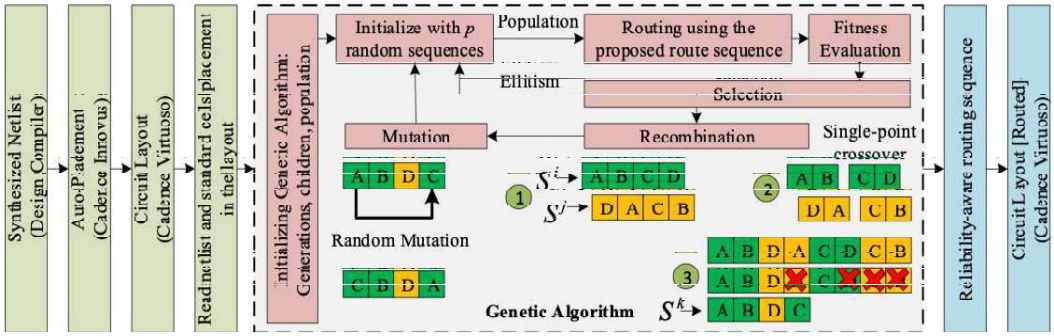

Figure 6: The complete routing flow based on the genetic algorithm, including the design flow steps, to obtain the reliability-aware route sequence for printed circuits. The A, B, C, D represent the pin tuple/pairs as (u, v) where u and v are the start and end pins, respectively.

are only isolated at crossover position and all crossings of metal $i+1$ over metal i are translated as crossovers, as shown in Figure 4a. Hence, utilizing any VLSI router would result in sub-optimal results or even non-functional circuits as it is unaware of the crossovers.

This routing methodology can be adjusted for printed electronics by integrating the crossovers cost and technology-specific design constraints in routing tool. Additionally, the sequence of nets in which they are routed is very important for the reliability. For example: if nets are routed as $[VSS, Net\_G, VDD]$ (or $[(S,S),(G,G),(D,D)]$ in case of pin-to-pin routing) then it would lead to the least critical situation (Figure 5g). However, the sequence $[Net\_G, VDD, VSS]$ would lead to the most critical configuration in routing (Figure 5a). Thus, we propose a crossover aware routing solution which utilizes the genetic algorithm to find the optimized nets routing sequence with minimum number of crossovers. The genetic algorithm based routing solutions, for limited metal layers, were also proposed in the past [21], [22] but such methodologies have ignored the crossovers placement and their reduction.

B. Reliability-Aware Router

Our router is based on the Lee's algorithm [23] with Dijisktra algorithm [24] for the shortest routing path. The routing is preformed in a pin-to-pin routing fashion by dividing nets into pin pairs/tuple. This is because multiple pins could be connected to a net and dividing nets in pin pairs would allow to set high pin costs for a critical path or a path with critical pins (such as source terminal). This will insure that at the intersection of two nets, the crossover is placed on a less critical path. The proposed methodology can be utilized for net sequence (instead of pin pairs sequence) without any modification. The route sequence for pin pairs is generated through the genetic algorithm. Based on the associated routing costs, the sequence would be labeled as a bad or a good sequence. At the end of the generations, the sequence having the lowest total routing cost would be selected as the optimal routing sequence. The router itself is divided into two parts and defined as follows:

The Routing Cost: The quality of the routing is judged by the total routing cost. The typical cost function contains the path, crossover and pins costs.

- *Path Cost* is the length of the routing path from the source pin to target pin.
- *Crossover Cost* is a user defined cost for the crossover. It is added to the respective routing path cost whenever a crossover is placed at the intersection of routing paths.
- *Pin Cost* is used to define the criticality of a pin. Higher the criticality, higher would the pin cost compared to the less critical pins.

The crossover and pin costs are very important in terms of the circuit reliability. The routing path with a crossover has higher cost compared to a path without crossover. Based on the numbers of crossovers in a routing solution, the routing cost is increased. At the intersection of routing paths, the pin cost is always helpful for placing a crossover on a less critical path. For example, comparing the situations like Figure 5a and Figure 5d the latter is always preferred due to less criticality compared to the former. This is achieved by assigning individual pin cost based on their criticality. The sum of these costs for all paths gives the total routing cost and the objective is to minimize this cost by trying different routing sequences. The routing cost guides the genetic algorithm to converge to a valid and optimum routing solution for the given input pin-pairs.

Genetic Algorithm:

Genetic Algorithms (GA) [25] are heuristic optimization methods inspired by natural evolution and can be used to solve very general problems.

To apply GAs to the problem at hand, we need to find suitable mappings from the sequences of pin-to-pin-routing (P2PS) to *individuals* and define *recombination* as well as *mutation* rules creating valid routing sequences. For this, we will utilize rules similar to [21]:

- *Individual* - Is a P2PS $S^i = [s_1^i, s_2^i, \cdots, s_t^i, \cdots, s_n^i]$, where the elements of $s_t^i \in S^i$ are tuples of pins (u, v) that should be routed at time step t, e.g. $S^1 = [(1,2),(2,3),\cdots]$, $S^2 = [(2,3),(1,2),\cdots]$.
- *Population* - Set of P2PS $\mathbb{P} = \{S^1, \cdots, S^p\} \subset \mathbb{S}$, where p is the population size and $\mathbb{S}$ is the set of all valid sequences.
- *Generation* - Population $\mathbb{P}$ at a specific iteration of the GA.
- *Fitness* - Routing costs $C(S^i)$ for a P2PS S^i.
- *(Tournament) Selection* - Selects a P2PS for *recombination* or *mutation* as $\text{argmin}_{S \in \{S^i, S^j\}}\{C(S)\}$ where $S^i, S^j \in \mathbb{P}$ are drawn at random from the population.

TABLE I: The results for the different benchmark circuits generated using the proposed reliability-aware routing method and Virtuoso Auto-router (I = ISCAS'85 and E = The EPFL combinational logic benchmark circuits)

Benchmark Circuit	# of Gates	# of Nets	Virtuoso Auto-router			Proposed Methodology		
			# of Crossovers	# of Violating Paths	Runtime [s]	# of Crossovers	# of Violating Paths	Runtime [s]
c17^I	6	12	4	1	15	1	-	50
$c432^I$	205	241	840	3	7234	556	-	10812
$c499^I$	644	685	2729	17	25237	2038	4	39641
$c880^I$	428	488	1736	7	17760	1417	1	26115
$c1908^I$	519	522	1972	11	21272	1491	2	34308
ALU control unit^E	141	148	570	1	3530	438	-	5103
Int to float converter^E	243	256	1340	4	7980	1219	-	11121
Decoder^E	616	626	2638	25	26185	1974	5	40308
Lookahead XY router^E	169	259	373	1	3927	258	-	5718

- *Recombination* - A function $R : \mathbb{S} \times \mathbb{S} \rightarrow \mathbb{S}$, where a new sequence $S^k \in \mathbb{S}$ is generated as $S^k = R(S^i, S^j) = [s^i_1, \cdots, s^i_t, s^j_{t+1}, \cdots, s^j_n]$, for $t = \lfloor \frac{n}{2} \rfloor$.
- *Mutation* - A function $M : \mathbb{S} \rightarrow \mathbb{S}$, where a new sequence S^k is generated from a sequence $S^i \in \mathbb{P}$ by swapping two random indices s^i_a and s^i_b.

In the first step, the *fitness* of an *individual* is evaluated by routing the pin-to-pin tuples in its specified order using the Dijkstra algorithm [24] and evaluating the total cost of the routing. In the next step, which is refered to as *selection*, we choose *individuals* for *recombination* and *mutation*. For this, we utilize a mechanism called *Tournament Selection*. In *Tournament Selection*, two *individuals* of the current *population* are chosen, their *fitness* values are compared and the *individual* with the better *fitness* value is selected for *recombination*. In the recombination step, *individuals* selected for *recombination* are used to create new *individuals* (*children*) by splitting them in the middle and recombining[1] them according to Figure 6 to create new *individual(s)*. As the combined sequences will contain every tuple twice, only first occurrences are preserved while excess occurrences are deleted. Through this measure either one or two *individuals* can be created. The *individuals* created this way will then be added to a candidate-set for the next *generation*.

As an additional measure to create new *individuals*, *mutation* can be applied with a certain probability to the *individuals* in the candidate-set for the next *generation*. If *mutation* should be applied to an *individual*, two random pin-to-pin tuples are exchanged in the routing sequence representing of the *individual*. An illustration for *mutation* can be seen in Figure 6. Additionally, an *individual* selected for *mutation* can also have its entire sequence reversed. After applying these measures, a unique operator is applied to the candidate set for the next *population* to delete excess *individuals* and ensures that all *individuals* in the *population* are unique. This might lead to *generations* having a different *population* sizes if identical *individuals* were produced. Finally, to preserve the solution quality throughout multiple *generations* we apply a mechanism called *elitism*, which consists of copying the best *individual* i.e. routing sequence with the fewest costs to the next *generation* unconditionally. Generally, several measures to decrease computation costs like memorization of *fitness* values for already evaluated *individuals* and reusing previously computed prefix sequences can be employed.

The genetic algorithm and the crossover-aware router were integrated in a single framework to generate the reliability-aware routing solution. This framework is integrated with the cadence design environment from where it can read the layout information including placement, netlist, logic cells and pins. The detailed routing flow, including the design flow steps, is shown in Figure 6.

C. Evaluation and Discussion

In this work, the benchmark circuits from ISCAS'85 [26] and the EPFL benchmark suite [27] are used to evaluate the proposed methodology. The gate-level netlist is obtained by first characterizing the three basic logic cells (NOT, 2-input NAND and NOR) and then synthesizing the circuit netlist using synopsys design compiler. All cells are automatically placed in the layout using cadence innovus tool and then the layout is imported in Cadence Virtuoso layout environment. Each cell has a spacing of $1mm$ (on each side) to allow enough routing space around cells. The proposed method and the Virtuoso space-based router (with only two valid metal layers) is used to route the layout. The genetic algorithm was run for 1000 generations, with 5 children per iteration and the population size of 50. The results from both routing solutions are compared in Table I. The comparison is based on the number of crossovers in the routing solution, the number of violating paths and run-time. The number of violating paths represent the paths that do not meet the timing requirement of the circuit due to the extra delay introduced by the crossovers in the path.

It can be seen that the proposed methodology solution has fewer number of crossovers than the Virtuoso space-based router solution. On one hand, the fewer of number of crossovers will require fewer process steps, leading to shorter manufacturing time and costs, as well as higher manufacturing yield. On the other hand, it has lower impact on the circuit. To analyze the delay impacts, all crossovers are added as delay elements using buffers in the gate-level netlist. The number of violating paths are obtained by setting an operating clock for each benchmark circuit. As seen in Table I, in most cases, the proposed methodology has no failing paths. But circuits with high number of crossovers (1000+) have multiple failing

[1]This is commonly referred to as *single-point-crossover* in the GA literature but we avoid this terminology here to not confuse the reader by overloading the term crossover.

paths. Contrary to that, the routing solution from virtuoso has at-least one failing path for all benchmark circuits. On average, the proposed methodology solution has 29% less crossovers and 91% less violating paths than the virtuoso auto-router solution. However, the run-time for the proposed methodology is always higher than the virtuoso auto-router. This is because the genetic algorithm tries many route sequences to converge to an optimal routing solution. The run-time can be decreased by utilizing boost libraries which will reduce the execution time and memorizing and reusing the matching prefix, of previously proposed sequences, in the new proposed sequence. Moreover, the number of violating paths can further be reduced by implementing the crossover-aware placement which is in our future direction.

IV. Conclusion and Future Work

With the on-going progress on printable materials and improvement in the printed electronics technologies, the standard design flow and design automation methodologies are equally important to have printed functional devices and circuits. For that purpose, we have developed a Process Design Kit (PDK) for inkjet printed electronics technology. The results from our variability model show that it can capture the variation of EGFETs and can be used to run variability analysis of EGFET based circuits. We also proposed a reliability-ware routing solution for additive manufacturing based circuits using a genetic algorithm. The proposed routing algorithm has been integrated with the industrial standard design flow.

In future, we plan to work on the back-end components of the technology and design kit including the placement of the components and optimized printing of the layout shapes. These steps would further improve the design flow, PDK and process technology which will enable further complex circuits based applications for this technology.

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