

# Dual-gate self-aligned a-InGaZnO transistor model for flexible circuit applications

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**Abstract**—This work elaborates on an amorphous Indium-Gallium-Zinc Oxide thin-film transistor model for a dual-gate self-aligned transistor configuration, enabling the design and realization of complex integrated circuits. The model originates from a mobility-enhanced transistor behavior model, whereby the additional backgate impacts key parameters, such as threshold voltage, mobility and subthreshold slope. The model has been validated for the full design flow and compared to measurement results, from single transistors, to inverters, ring oscillators and RFID transponder chips.

**Keywords**—*InGaZnO*, *mobility-enhancement*, *dual-gate*, *modeling*, *integrated circuits*, *RFID transponder chips*

## I. INTRODUCTION

Thin-film transistor (TFT) technologies are attractive for item-level Internet-of-Things applications requiring ultra-thin, flexible integrated circuits operating at low power to enable seamless integration into objects. Metal-oxide thin-film transistors (TFTs), amongst others Indium-Gallium-Zinc-Oxide or InGaZnO are ideal candidates for these applications, resulting in n-type transistors with an electron mobility around 10-20cm<sup>2</sup>/Vs [1]. Recent developments in this field have demonstrated phone-detectable near field communication (NFC) tags compatible to ISO14443 standard [2]. The realization of such demonstrator requires, besides maturity in technology, also increased maturity in the design flow and its simulation models. The design flow was based on a standard cell place-and-route for the core of the chip and a manual placement for the partition that requires high-speed operation to avoid substantial parasitic overlap due to automatic routing algorithms. The focus of this work will be the InGaZnO transistor model enabling SPICE predictions of the circuits' behavior.

The quality of the prediction of the currents and voltages in between the terminals of the TFT will impact directly the accuracy of the DC simulation parameters. Transient analysis of the circuit requires to additionally model the capacitances of the TFT and parasitic resistances and capacitances of the circuit. A dual-gate transistor has four terminals: gate (G), source (S), drain (D) and backgate (BG). The cross-section of a dual-gate TFT and the different currents and voltages are shown in Fig. 1. Depending on technology, the gate and backgate terminal may be swapped and may differ in symmetry.

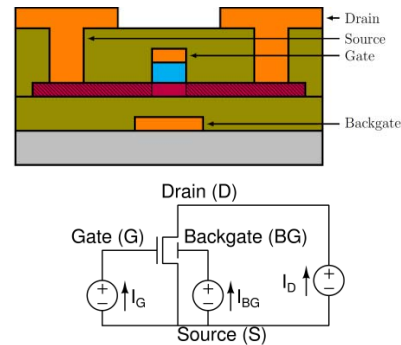


Fig 1: (top) Typical cross-section of a self-aligned dual-gate InGaZnO TFT and (bottom) different currents flowing in a 4-terminal dual-gate TFT

## II. MOBILITY-ENHANCEMENT MODEL

In the simplest case of a single gate device, the saturation current of a transistor can be described by a quadratic equation according to Shichman and Hodges [3]:

$$I_D = \frac{\mu C_{ox} W}{2 L} (V_{GS} - V_T)^2$$

where  $\mu$  defines the mobility and  $C_{ox}$  the gate oxide capacitance.  $W$  and  $L$  are the electrical width and length, and  $V_T$  is the threshold voltage. Similar as many thin-film semiconductors [4], [5], [6], InGaZnO shows a larger mobility for larger values of  $V_{GS}$ . The apparent mobility enhancement effect can be described by a less than linear relation with respect to  $V_{GS}$ :

$$\mu = \mu_0 (V_{GS} - V_T)^\gamma$$

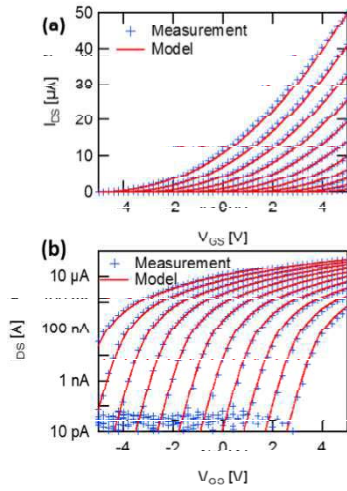


Fig 2: TFT transfer curve comparison between measurement and  $V_T$ -shift only model, when  $V_{BG}$  is varied between -5V and +5V

Here,  $\gamma$  is the mobility enhancement factor,  $\mu_0$  is defined as the mobility at  $V_{GS} - V_T = 0$ , so it does not represent the maximum mobility of the device anymore. The saturation current for a single-gate InGaZnO transistor can therefore be described as [5]:

$$I_D = \frac{\mu_0 C_{ox} W}{2 L} (V_{GS} - V_T)^{2+\gamma}$$

Thin-film devices are intrinsically symmetrical due to the lack of bulk contact, so the transition from saturation to linear regime can best be described by an equation that represents this symmetry. Therefore, the subtraction of two saturation currents can be used: the forward and reverse current. The forward current is determined by  $V_S$ , while the reverse current is determined by  $V_D$ . The total current then is [5]:

$$I_D = \frac{\mu_0 C_{ox} W}{2 L} [(V_G - V_S - V_T)^{2+\gamma} - (V_G - V_D - V_T)^{2+\gamma}]$$

The extension in the subthreshold region for single gate modeling can be found in [5].

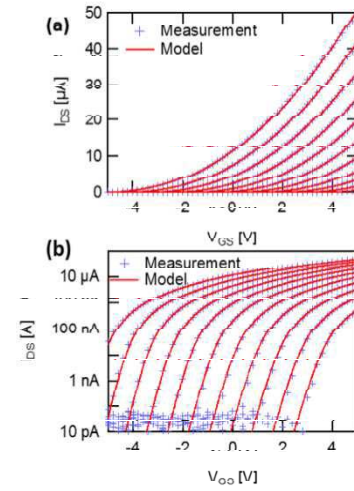


Fig 4: TFT transfer curve comparison between measurements and complete DC model, when  $V_{BG}$  is varied between -5V and +5V

### III. INTRODUCTION OF THE BACKGATE

The technology comprises of a thin-film transistor having an individual controllable backgate per transistor, similar as FD-SOI technologies. This feature is beneficial for TFT-based applications, enabling to tune the threshold voltage of each transistor [7]. Typically, only the  $V_T$ -shift is modeled with the backgate. This limits the prediction accuracy for our TFT measurements, shown in Fig. 2.

A better approximation can be made by extracting the mobility-enhancement model for every value of  $V_{BG}$  and evaluate the change in both mobility and  $\gamma$  depending on the  $V_{BG}$ . The values for  $V_T$ ,  $\gamma$  and subthreshold slope (SS) can be estimated by a linear function.  $\mu_0$  can be estimated as a quadratic function.

$$\begin{aligned} V_T &= V_{T0} - \zeta V_{BG} \\ \gamma &= \gamma_0 + \gamma_1 V_{BG} \\ \mu_0 &= \mu_{00} + \mu_{01} V_{BG} + \mu_{02} V_{BG}^2 \\ SS &= SS_0 + SS_1 V_{BG} \end{aligned}$$

Here,  $\zeta$  is the ratio of capacitive coupling between front and backgate, while  $V_{T0}$ ,  $\mu_{00}$ ,  $\gamma_0$  and  $SS_0$  are the threshold voltage, mobility, mobility enhancement factor and

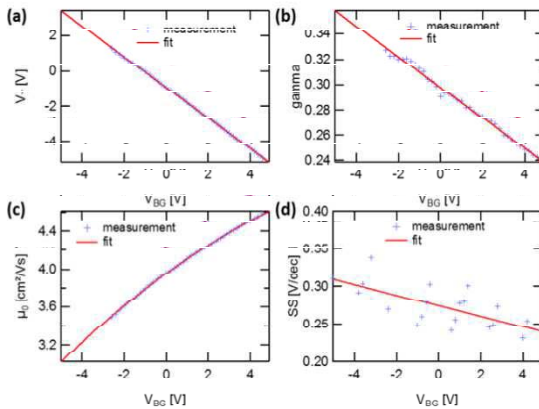


Fig 3: (a)  $V_T$ , (b)  $\gamma$ , (c) mobility and (d) SS model parameters fitted as a function of backgate voltage

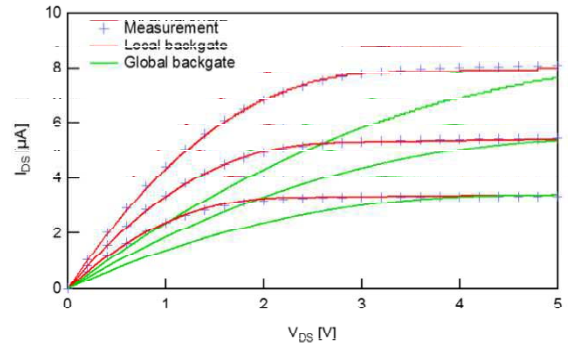


Fig 5: Measurements of a TFT output curve compared to the model with local and global backgate principle

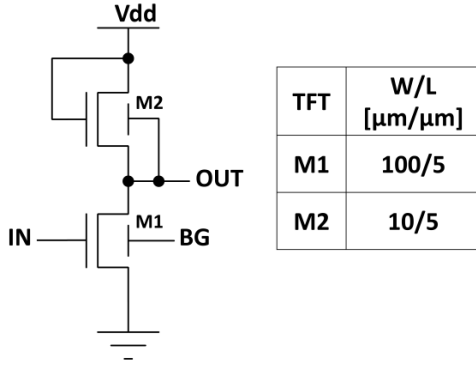


Fig. 6: Schematic of a dual-gate diode-load inverter and the sizes of the TFTs

subthreshold slope for  $V_{BG} = 0$ . The other parameters have no physical meaning and are purely there to improve the quality of the prediction. Fig. 3 shows the fit of all transistor parameters according to these equations. It can be observed that the equations fit very well. Fig. 4 plots the transistor measurements after applying different backgate voltages and compares these to the simulated model after fitting the parameters. A good fit is observed for the on-behavior of the TFT.

In the transition from linear to saturation, the approach where  $V_T$  is only dependent on  $V_{BG}$  is not sufficient. The model above assumes that a change in backgate influences the parameters such as mobility for the forward and backward current identically, as e.g. the mobility is shifted by a fixed value. This is referred to as the global backgate model.

Fig. 5 depicts the output characteristic for the global backgate model and compares it to the measurements. Saturation occurs much sooner on the  $V_{DS}$  axis than predicted by the model. The solution is to adopt a local backgate model. Since the forward current is caused by the overdrive voltage at the source and the reverse current is caused by the overdrive voltage at the drain, also the expressions for the shift in mobility need to be applied depending on the local (source or

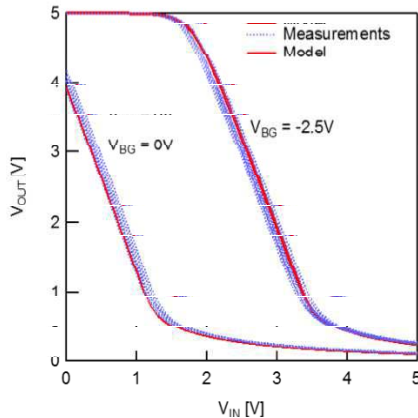


Fig 7: Voltage transfer curves measured for 8 different dual-gate diode-load inverters and compared to the SPICE simulation with the presented model

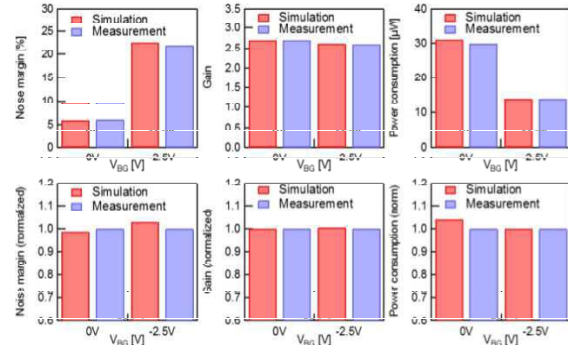


Fig. 8: Comparison of the extracted parameters, gain, noise margin and DC power from the measurements and SPICE simulations of the inverters plotted in Fig. 7 for two different backgate voltages

drain) backgate overdrive voltage  $V_{BGX}$ . The shift in  $V_T$ ,  $\gamma$ ,  $\mu_0$  and SS then depends on this local backgate overdrive voltage, not the global backgate overdrive voltage:

$$V_{BGX} = V_{BG} - V_X$$

Whereby  $V_X$  is  $V_S$  and  $V_D$  for the forward and reverse current respectively. Fig. 5 indicates that the local backgate improves the prediction of earlier saturation. Consequently, the saturation voltage  $V_{DSSat}$  must be calculated differently and occurs when the reverse current becomes 0:

$$V_{DSSat} = \frac{V_G + \zeta V_{BG} - V_{T0}}{1 + \zeta}$$

In addition to the earlier onset of saturation, the output resistance of a dual-gate device is improved compared to a single gate device, due to the enhanced electrostatic control of the channel.

The complete DC model for a dual-gate self-aligned TFT can be found by combining the above-explained equations. This incorporates forward-backward mobility-enhancement current equations, subthreshold behavior and the parameter shift caused by the backgate.

$$I_D = \frac{\mu_{0S} C_{ox} W}{2} V_{GSTe}^{2+\gamma_S} - \frac{\mu_{0D} C_{ox} W}{2} V_{GDTe}^{2+\gamma_D}$$

$$V_{GXTe} = (2 + \gamma_X) SS_X \log_{10} \left( 1 + 10^{\left( \frac{V_G - V_X - V_{TX}}{(2 + \gamma_X) SS_X} \right)} \right)$$

$$V_{TX} = V_{T0} - \zeta (V_{BG} - V_X)$$

$$\gamma_X = \gamma_0 + \gamma_1 (V_{BG} - V_X)$$

$$\mu_{0X} = \mu_{00} + \mu_{01} (V_{BG} - V_X) + \mu_{02} (V_{BG} - V_X)^2$$

$$SS_X = SS_0 + SS_1 (V_{BG} - V_X)$$

#### IV. FROM TFT TO INTEGRATED CIRCUITS

A complex digital integrated chip is built from a standard cell library containing a multitude of simple and complex logic gates. One of the key logic blocks is an inverter gate. The self-aligned dual-gate InGaZnO thin-film transistor technology conducts only electrons, leading to the implementation of a dual-gate diode-connected load inverter gate, detailed in Fig. 6. The drive transistor uses its backgate to shift the voltage transfer curve of the inverter with an external backgate voltage, aiming to maximize noise margin and/or speed.

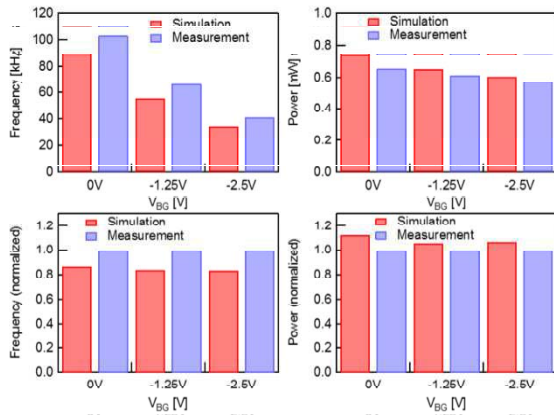


Fig. 9: Comparison of the extracted parameters, frequency and power from the measurements and SPICE simulations of 33-stage ring oscillators

We have measured 8 dual-gate diode-load inverters at two different bias voltages (0V and -2.5V), shown in Fig. 7, fabricated with the self-aligned dual-gate TFT technology. The variability of the curves stems from the presence of transistor parameter variation on the manufactured wafers. The extracted  $V_T$  standard deviation on a 150mm wafer with our lab process is about 250mV. The red solid line in Fig. 7 shows the simulated curve by using the dual-gate model, with a threshold voltage of -575mV. It is observed that the slope of the voltage transfer curve is predicted well with the described model, indicating that the currents are well matched with the measured data. Standard cell library design will require a relevant amount of Monte Carlo simulations of the logic gates, taking into account the intrinsic parameter variation of the technology. As such, important parameters such as gain, noise margin, speed and power will be predicted more accurate.

Fig. 8 shows the extracted gain, noise margin and DC power of the inverter gate for the measurements and the model at 0V and -2.5V  $V_{BG}$ . It is observed that the simulated inverter gate predicts the DC parameters accurately, with an error less than 4%.

Another key parameter, next to robustness and gain, is the stage delay of a logic gate. In order to validate this, we have realized 33-stage ring oscillators based on the dual-gate diode-load inverter topology. 5 ring oscillators have been characterized at a supply voltage of 5V, whereby  $V_{BG}$  is varied between 0V, -1.25V and -2.5V. The average frequency is plotted in Fig. 9. Simulations of the transient behavior is also performed by including a basic gate capacitance behavior and some parasitic overlap capacitors in the layout of the ring oscillator. The ring oscillator frequency of the simulations is observed to be slower than the measurement results. This can have multiple origins, amongst others an overestimation of the parasitic and gate capacitors which requires to be better modeled, or the fact that  $V_T$  may be different for this location on the wafer due to variability. The threshold voltage impacts directly the on-current and off-current, and therefore the stage delay of the inverters.

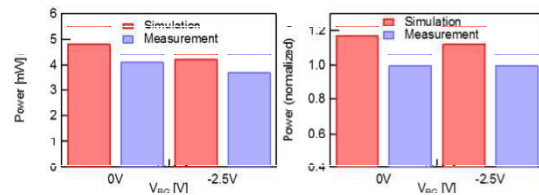


Fig 10: Measurement and SPICE simulation comparison of the power consumption of a 12-bit RFID transponder chip

Finally, many applications for thin-film electronics would benefit from ultra-low power consumption, such as increasing battery life of one-time usable patches or increasing reading distances of thin-film RFID tags. A good prediction of the power consumption will consequently lead to more optimized designs with respect to power consumption. The power consumption of the above-mentioned ring oscillators has been measured and compared to the simulations. The simulated results are relatively close to the measurements, mainly due to static power consumption as a key contributor for unipolar logic gates. These logic gates suffer from a constant leakage current present between supply and ground node.

In addition, the power consumption has also been estimated for a 12-bit RFID transponder chip, employing 494 InGaZnO TFTs. The power consumption has also been characterized on the manufactured transponder chip, with a clock frequency of 100Hz. The comparison between simulation and measured power consumption at  $V_{BG}$  of 0V and -2.5V is plotted in Fig. 10, detailing a good first order prediction of the power consumption for digital integrated circuits. This power consumption combines both the static and dynamic components, whereby the static portion is mostly dominant for these unipolar dual-gate diode-load logic gates.

## V. CONCLUSIONS

This work elaborates on a transistor model of a dual-gate self-aligned thin-film transistor technology based on InGaZnO as semiconductor. The basic idea stems from a mobility-enhanced transistor behavior model. The addition of a backgate in this technology features an extra parameter for the designer to optimize the transistor behavior for its needs. It is found that a threshold voltage shift by the backgate is not sufficient to explain the behavior of the device: in addition, the backgate voltage influences the subthreshold slope, mobility and mobility enhancement. The simulation model has been validated for inverters, ring oscillators and 12-bit RFID transponder chips, fabricated with these dual-gate self-aligned TFTs. A good match between the measurement results of the DC parameters of the circuits with the simulations using the model was found.

## ACKNOWLEDGMENT

This work has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme under grant agreement No 716426 (FLICs project). The described work is partially financed through the Flexlines project within the Interreg V-programme Flanders-The Netherlands, a cross-border cooperation programme with financial support from the European Regional Development Fund.

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