Inkjet-Printed True Random Number Generator based on Additive Resistor Tuning

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***Abstract*—*Printed electronics* (PE) is a fast growing technology with promising applications in wearables, smart sensors and smart cards since it provides mechanical flexibility, low-cost, on-demand and customizable fabrication. To secure the operation of these applications, *True Random Number Generators* (TRNGs) are required to generate unpredictable bits for cryptographic functions and padding. However, since the additive fabrication process of PE circuits results in high intrinsic variation due to the random dispersion of the printed inks on the substrate, constructing a printed TRNG is challenging. In this paper, we exploit the additive customizable fabrication feature of inkjet printing to design a TRNG based on electrolyte-gated field effect transistors (EGFETs). The proposed memory-based TRNG circuit can operate at low voltages ($\leq 1\,V$), it is hence suitable for low-power applications. We also propose a flow which tunes the printed resistors of the TRNG circuit to mitigate the overall process variation of the TRNG so that the generated bits are mostly based on the random noise in the circuit, providing a true random behaviour. The results show that the overall process variation of the TRNGs is mitigated by 110 times, and the simulated TRNGs pass the *National Institute of Standards and Technology Statistical Test Suite*.**

***Index Terms*—inkjet printing, hardware security, printed electronics, true random number generator, customizable fabrication, additive manufacturing**

I. Introduction

Printed electronics (PE) has gained lots of interests since it has the advantages of mechanical flexibility, low-cost, on-demand and customizable fabrication [5]–[7]. This leads to the use of PE in many applications such as IoTs [8], wearables [11], radio frequency identification tags [12], smart cards [13], smart labels [14] and smart sensors [4]. Several organic and inorganic printed transistors have been proposed to construct functional PE circuits fabricated using additive processes [17], [22]. Inorganic Electrolyte-gated Field Effect Transistors (EGFETs), which enable low voltage PE circuits, has been recently used in various circuits showing that it can operate below $1\,V$ [22], [24].

The advancement of PE gives rise to security concerns, specifically authentication and cryptography, since the projected application areas are mostly interconnected, and contain sensitive data. For these purposes, True Random Number Generators (TRNGs) are employed to generate unpredictable keys, the initial vector of Pseudo-Random Number Generators (PRNGs), padding values and random challenge sequences [3].

TRNGs digitize an unpredictable natural phenomena (entropy source) such as thermal noise to random bits while PRNGs use a short initial random bits generated by a TRNG, and generate random-looking longer bitstreams [28]. The entropy source of the TRNG design is the most crucial component since it provides the unpredictability, and the TRNG circuit should harvest the entropy without introducing bias. The bias caused by the entropy source, the process variation of the circuit, or the environmental changes can be masked using a post-processor, although it is not needed in all designs [27], [28].

Additive printing processes including inkjet printing have high intrinsic process variation resulting from the dispersion of the ink printed in multiple steps, where each step varies on its own [2], [23], [29]. Since the high process variation can significantly bias the generated bits of TRNGs, designing an inkjet-printed TRNG, in other word mitigating the high variation, is very challenging. At the same time, inkjet printing enables the customization of each circuit individually, which can be exploited to mitigate the high process variation of the fabricated circuits in the post-fabrication phase [1], [29].

In this paper, we present an inkjet-printed TRNG, which utilizes the customizable fabrication feature of this technology to compensate the high intrinsic process variation. A printed resistor that can be tuned by printing additional layers is presented and utilized in the proposed memory-based circuit to mitigate the overall process variation so that the power-up behaviour of the circuit is highly based on the noise. We propose a flow that tunes the resistors to determine the point where the overall process variation of the circuit is mitigated, and the generated bits are random. Additionally, we optimize the resistor tuning flow to reduce the measurement and tuning efforts. The results show that the mean of the overall process variation of several TRNG instances is reduced by 110 times using the resistor tuning flow, and the optimized tuning flow decreases the tuning time by 10 times. Simulation results for *National Institute of Standards and Technology - Statistical Test Suite* (NIST-STS) show that the proposed TRNG design can provide highly random bitstreams that pass the required tests.

The rest of the paper is organized as follows: the details of PE and EGFET technology are given in Section II. Section III explains the resistor tuning using additive printing based on fabrication data. In Section IV, we present the proposed inkjet-printed TRNG design. In Section V, the proposed resistor tuning flow is elaborated. Section VI presents and discusses the experimental results, and Section VII concludes the paper.

978-3-9819263-2-3/DATE19/©2019 EDAA

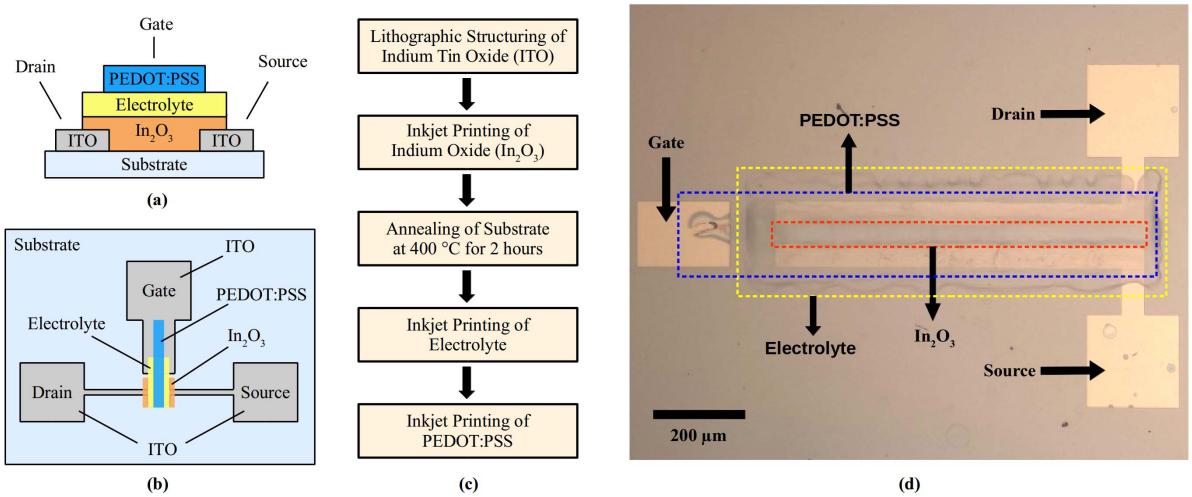

Figure 1. Description of Electrolyte-gated field-effect transistor technology a) Cross-sectional view of EGFET on substrate [22]. b) Top view of EGFET on substrate [22]. c) Flow of fabrication process of EGFET [10]. d) Top view photo of a fabricated EGFET [10].

II. Background on Printed Electronics

Printed Electronics (PE) is a growing market in several current and envisioned applications such as health care diagnosis devices, energy harvesters, smart clothing, dynamic newspapers, smart labels and smart cards [8]. Instead of using complex, expensive and environmentally hazardous photolithographic subtractive processes, PE circuits are fabricated using several additive processes such as offset, screen, flexography, gravure and inkjet printing, resulting in low-cost and on-demand fabrication [8]. PE circuits are fabricated printing several materials on a flexible or a rigid substrate additively using one or multiple printing processes depending on the application requirements. Some of these processes such as inkjet printing have made possible the customizable fabrication which is highly beneficial feature for "Industry 4.0" [1]. The customizable fabrication allows post-fabrication tuning to make custom changes in the fabricated circuits.

Various printed transistors such as p-type organic-based thin film transistors (OTFTs) [15], organic field-effect transistors (OFETs) [16] and n-type organic transistors [17], [18] are presented to form functional PE circuits. However, these transistors mostly suffer from high supply voltage and low field effect mobility making them unsuitable for low-power applications [5]. On the other hand, inorganic semiconductor based transistors combined with an electrolyte gate, called electrolyte-gated field-effect transistors (EGFETs), provide high field effect mobility and require low supply voltage ($\leq$ $1\,V$) since EGFETs have high gate capacitance [10], [19]–[22], [24], [25]. Since there is no equally performed p-type EGFETs available, digital circuits are mostly designed in resistor-transistor logic.

The channel material *indium oxide* (In_2O_3) semiconductor is inkjet-printed between drain and source electrodes which are lithographically structured *indium tin oxide* (ITO). After that, the electrolyte is inkjet-printed on top of the channel instead of a gate dielectric. Finally, *poly(3,4-ethylenedioxythiophene)-polystyrenesulfonic acid* (PEDOT:PSS) is inkjet-printed on top of the electrolyte as a top-gate. The cross-section of the structure, the fabrication process, and the top view photo of the EGFETs are shown in Figure 1.

III. Additive Printing of Resistors

Additive printing processes have several advantages over subtractive processes where sophisticated and/or expensive equipments and infrastructure are required. These advantages are low-cost, on-demand and customizable fabrication. The customizable fabrication can be used to modify/tune the circuits with very little effort, after the manufacturing.

We have examined an inkjet-printed resistor exploiting the customizable fabrication [9]. The resistance of the printed resistor which uses PEDOT:PSS as a material can be modified by printing more layers on top of existing layers. Each layer can be represented as a resistor, and printing a layer on top of the other layers adds another resistor in parallel as illustrated in Figure 2.

The printed resistors containing various number of layers with the width of $50\,\mu m$ are fabricated and characterized at room temperature. The measured effective resistance and the extracted individual resistance of the layers are given in Figure 3. Since the path of each successively printed layer is

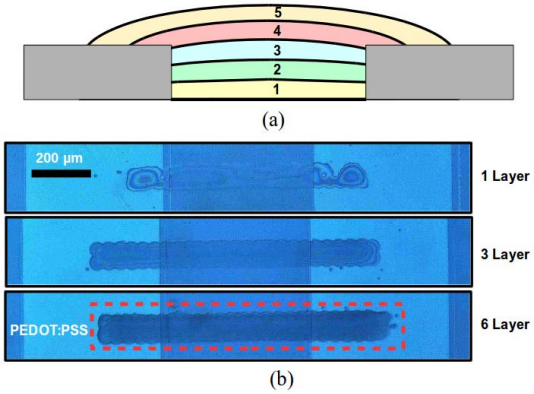

Figure 2. a) Illustration of additively printed layers. b) Top-view photos of fabricated printed resistors.

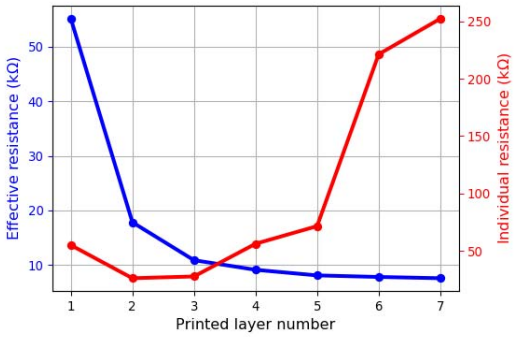

Figure 3. Resistance of printed resistors with different layers.

longer than the previous layers, as illustrated in Figure 2a, the resistance of each layer is larger than the previous layer.

The measurements show that the effective resistance decreases while the total number of layer is increasing, and the individual resistance of layers increases while the number of printed layers is increasing, except the first layer since it does not form a continuous line on the substrate, as shown in Figure 2b. Furthermore, to reduce the effective resistance even faster, additional layers can be printed next to other layers, which adds less resistance in parallel compared to the layer printed on top of other layers. Therefore, we can use this feature of the resistor tuning to compensate the process variation of the proposed TRNG circuit, as discussed in the next sections.

IV. Proposed Inkjet-Printed TRNG Design

The proposed TRNG circuit is a memory-based circuit that contains two cross-coupled inverters and a control transistor enabling/disabling the circuit. The inverters are composed of an n-type EGFET and a resistor. This is done for two reasons. Firstly, the p-type inorganic channel materials usually have very poor characteristics, hence effective p-type transistors are still under investigation. Secondly, the use of resistors in the pull-up network allows to realize the additive tuning. The circuit schematic of the TRNG is given in Figure 4.

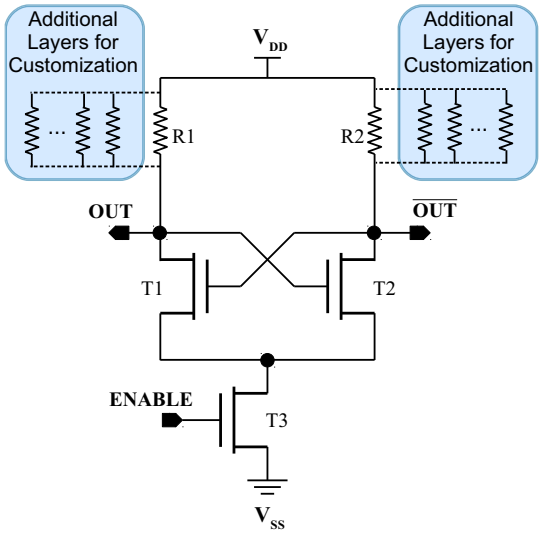

Figure 4. Proposed TRNG circuit with customizable resistors.

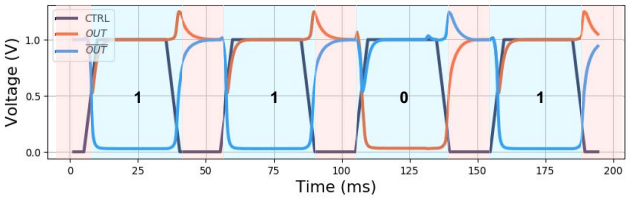

Figure 5. Simulated timing diagram of an inkjet-printed TRNG circuit.

The OUT and $\overline{OUT}$ nodes are equal to V_{DD} when the circuit is not enabled meaning that the $ENABLE$ input is logic-0. Since the symmetrical inverters lead to a metastable state, the feedback amplifies the random noise (thermal noise, shot noise, etc.), and drives the OUT and $\overline{OUT}$ nodes to the stable states, either logic-1 or logic-0 depending on the noise while the $ENABLE$ input is switching to logic-1. Therefore, the noise is digitized to generate true random bits. Figure 5 shows the waveform of the circuit generating the random bits based on the noise.

However, since the fabrication of the circuit is based on inkjet printing, it has high intrinsic process variation deriving from the random dispersion of the ink on the substrate. In addition, contrary to the silicon technology where the process variations are divided into local and global variations, which result in low variation between two close devices, all devices are printed individually by multiple additive steps in inkjet printing, which cause higher variation, even for the two cross-coupled inverters in this circuit.

The process variation cause a skew that forces the circuit to one side which results in the bias at the generated bits. A skewed circuit whose behaviour is illustrated in Figure 6a is biased to logic-1 because of the process variation (Δ_{PV}), while the non-skewed circuit whose behaviour is illustrated in Figure 6b is not biased and generates bits based on the random noise which is essential for a TRNG. Therefore, to construct an inkjet-printed TRNG, its high process variation should be mitigated. For this reason, we propose a resistor tuning flow explained in the following section.

V. Resistor Tuning Flow

It is vital to compensate the skew of the proposed TRNG circuit, which results from the overall process variation. The proposed resistor tuning flow as shown in Figure 7 utilizes the additively-printed resistor, as presented in Section III, to compensate the overall skew shown in Figure 6. The printed

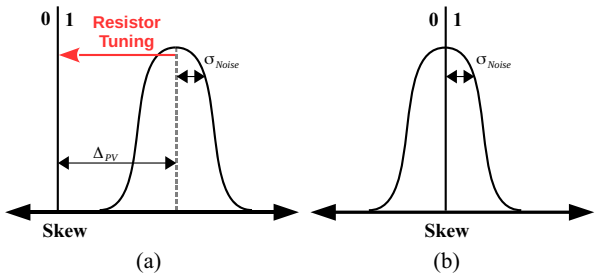

Figure 6. Illustration of behavior of a) skewed, b) non-skewed circuit (Δ_{PV}: skew because of process variation, σ_{Noise}: standard deviation of noise) [3].

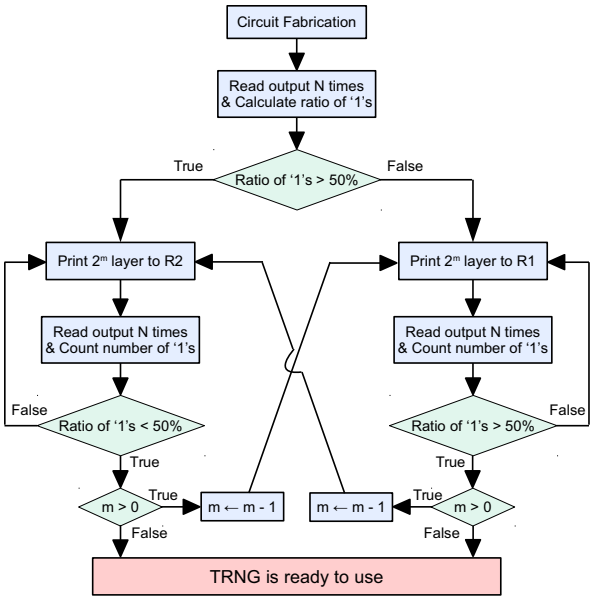

Figure 7. Optimized resistor tuning flow to mitigate process variation of proposed TRNG design.

resistor tuning flow is as follows. After fabricating the circuit, the output has to be read N times, and the number of '1's in N read is counted. If the number of '1's is greater than $N/2$ (50%), which means that the tuned circuit is skewed to logic-1, printing one layer to the $R2$ shifts the skew towards neutral axis. If the number of '1's is less than $N/2$, printing one layer to the $R1$ shifts the skew from logic-0 towards neutral axis. Printing additional layers to the $R1$ or $R2$ is repeated until the number of '1's reaches to $N/2$.

Figure 8a shows the ratio of '1's in the generated bitstream of an inkjet-printed TRNG with respect to the number of additional layers. The simulation flow to obtain the generated bitstream is based on the Monte Carlo simulation of a TRNG instance, which uses the parameters given in Table I and $\pm 10\%$ variation for the resistors and the variation model presented in [2]. In addition, a normal distributed random noise source which has the mean (μ) and sigma (σ) of $0\,V$ and $3\,mV$ is used in simulation. Since the range near to 50% ratio of '1's (non-skewed point) is too short, the additional layers of the resistor are printed one by one to not miss the non-skewed point. However, this leads to very long tuning time (including the number of iterative measurements and printing steps) since, in each step, the circuit output has to be read N times. For this reason, we optimize the resistor tuning flow to reduce the tuning time. In the improved flow as illustrated in Figure 7, if the ratio of '1's is greater (smaller) than 50%, 2^m layers are printed on top of $R2$ ($R1$) in each step, and then the measurements are done, until the ratio of '1's is less (greater) than 50%. When it is less (greater) than 50%, 2^{m-1} layers are printed on top of the resistor of the opposite branch, in this case $R1$ ($R2$) vice versa, and it continues until the number of printed layers reaches one. Therefore, the overall tuning time is significantly reduced.

In addition to these improvements for the resistor tuning flow, the TRNG output voltage level can be used to further improve the tuning efforts. The change of the TRNG output voltage level with each successive printed resistor layer can give an insight about the skewness of the TRNG so that the step size can be adjusted more effectively. Figure 8b shows the output voltage level of a TRNG circuit at different successive printing layers generated from the same setup described above. The more the circuit is skewed, the output voltage levels are closer to V_{DD} (or GND). As the skewness decreases, the output voltage level degrades more. This information could be used to further optimize the tuning flow. However, utilizing such information requires more precise, costly, and sophisticated measurements at the tuning steps, unlike the fast and low-cost binary readouts used in the proposed tuning flow.

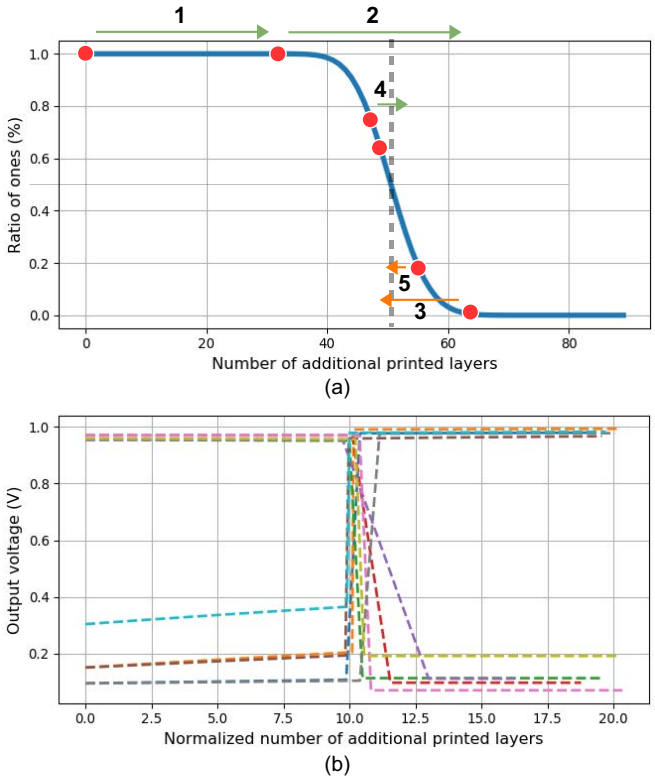

Figure 8. a) Ratio of '1's vs. number of additionally printed layers of a TRNG instance under noise ($\mu = 0\,V, \sigma = 3\,mV$). Red dots indicate TRNG state and orange and green arrows represent change of TRNG state by printing additional layers to $R1$ and $R2$ respectively, based on the tuning flow presented in Figure 7. b) Output voltage level vs. normalized number of additionally printed layers of 10 TRNG instances (layer numbers where output is flipped are normalized to 10.).

VI. Simulation Results

In order to evaluate the characteristics of the printed TRNG and the impact of the resistor tuning flow, we have used a combination of empirical and simulation analyses. The design parameter details are given in Table I. We have assumed that the printed resistors are composed of one hundred layers resulting in $60\,k\Omega$ effective resistance, and we extrapolated the effective resistance for each additional printed layer. In addition, the process variation of the resistors is considered as

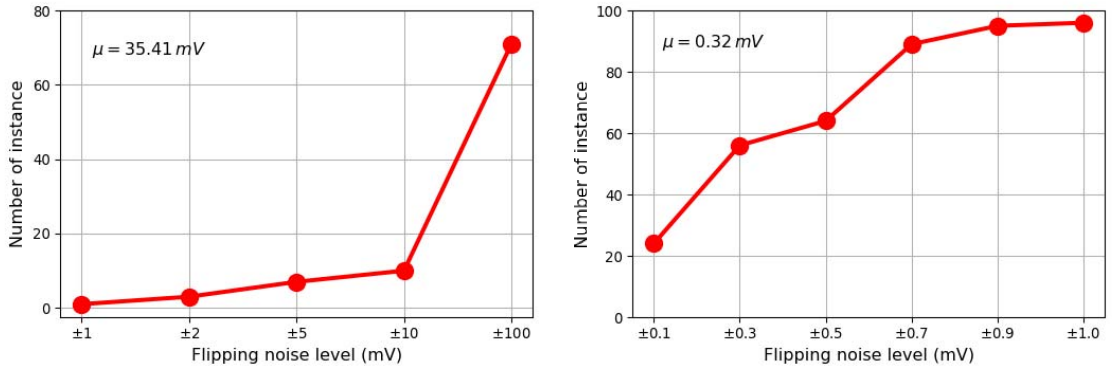

Figure 9. Number of TRNG instances between various flipping noise levels a) before, b) after resistor tuning.

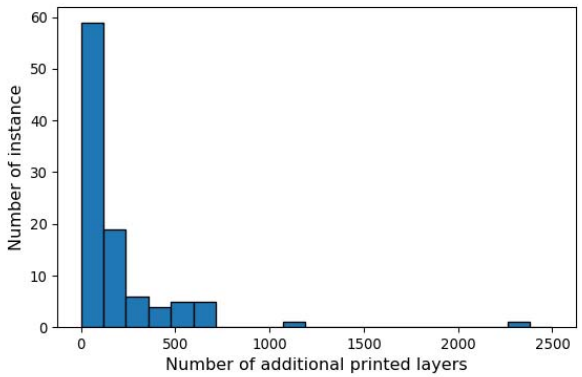

Figure 10. Number of printed layers to tune resistors using baseline flow (one by one layer printing).

$\pm 10\%$ of resistances based on the experiments. For EGFETs, we have employed the variation model of EGFET presented in [2]. We have used 100 Monte Carlo instances of printed TRNG, and a normal distributed noise source which has the mean (μ) and sigma (σ) of $0\,V$ and $3\,mV$ respectively, is introduced between inverters as an overall noise in the circuit to extract the results.

Resistor Tuning Flow Results. The minimum noise level to flip the output, which is called *flipping noise level* in this paper, is used to quantify the overall skewness of the TRNG instances. To extract the flipping noise level of the instances,

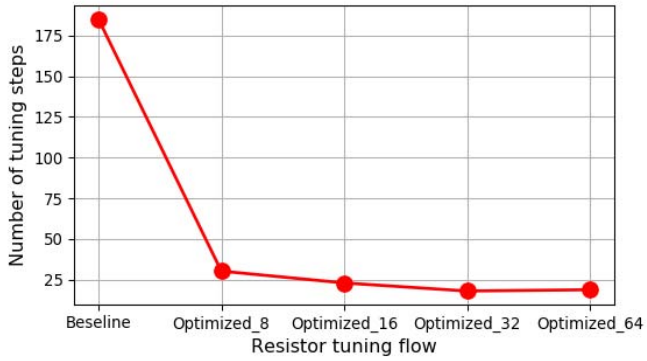

Figure 11. Mean number of tuning steps of 100 TRNG instances for baseline (one by one layer printing) and optimized tuning flows (2^m layer printing). Baseline denotes one by one additional layer printing flow. 8, 16, 32 and 64 denote initial $2^m value$.

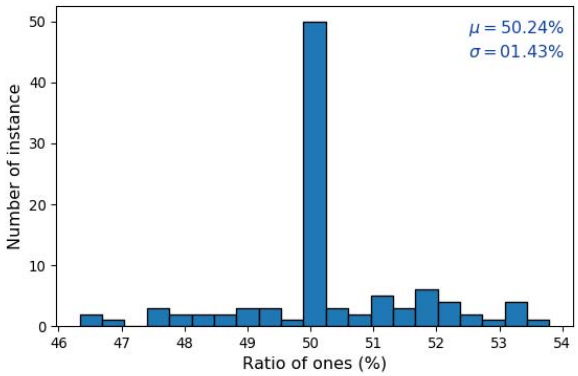

Figure 12. Distribution of ratio of '1's of generated bits of 100 TRNG instances.

instead of a normal distributed noise, a DC voltage was swept between $-100\,mV$ and $+100\,mV$. The number of TRNG instances based on their flipping noise levels, before and after the resistor tuning, is depicted in Figure 9. The mean values of the absolute flipping noise level before and after the tuning are $35.41\,mV$ and $0.32\,mV$ respectively, showing that the tuning flow reduces the mean variation by more than 110 times. In addition, the percentage of TRNG instances with the flipping noise level between $\pm 1\,mV$, resulting in less bias at the generated bits, increases from 1% to 96% after the tuning.

As described in Section III, the resistors are tuned by printing additional layers in two ways which we name "Baseline" (one by one, printing only one resistor) and "Optimized_m" where 2^m is the step size (2^m steps and tuning both resistors) for convenience. The distribution of the number of additional printed layers to tune the resistors for the Baseline flow, and the average trials to tune the instances are given in Figures 10 and 11. The average number of tuning steps for the baseline flow is 185.15 while with step size of 32 (m=5), the average number of tuning steps is minimized to 17.98. Therefore, the number of tuning steps is reduced by more than 10 times using our proposed method.

TABLE I
DESIGN PARAMETERS OF TRANSISTORS AND RESISTORS IN TRNG DESIGN.

	T1	T2	T3			R1	R2
Width	200 μm		400 μm		Resistance	60 $k\Omega$	
Length	40 μm						

TABLE II
NIST TEST RESULTS. GENERATED BITSTREAM INCLUDES 1096 BITS FROM 100 SIMULATED TRNG INSTANCES. (A TEST REQUIRES THE P-VALUE GREATER THAN 0.001 AND THE PROPORTION GREATED THAN 96/100 TO PASS.)

Statistical Test	P-value	Proportion	Result
frequency	0.202268	97/100	Pass
block frequency	0.759756	99/100	Pass
cumulative sums	0.504566	96/100	Pass
runs	0.719747	98/100	Pass
longest run of ones	0.455937	99/100	Pass
FFT	0.025193	99/100	Pass
serial	0.4557635	99/100	Pass

The generated bits of the circuits after the resistor tuning are slightly biased, compared to the true random bits because of the remained skewness of the process variation, due to the process variation of the additional printed resistor layers as well as the discrete nature of tuning. The effect of the remained skewness on the bits can be quantified as the sigma (σ) of the distribution of the '1's ratio in the generated bits, which is 1.03% as shown in Figure 12.

NIST Test Results. *National Institute of Standards and Technology - Statistical Test Suite* (NIST-STS) contains several tests explained in [26] to evaluate the randomness of the generated bits. We have used NIST-STS to evaluate the 1096 bits generated from each tuned TRNG instance. A P-value greater than 0.001 and a proportion greater than 96/100 are required to pass NIST tests. The results given in Table II show that the generated bits satisfy the requirements, and therefore, the proposed TRNG design pass the NIST-STS tests.

VII. CONCLUSION

Printed electronics is paving its way in many application domains. These applications may require random keys generated by TRNGs to secure their operations. Since PE circuits have high intrinsic process variation, designing a proper TRNG requires the mitigation of the process variation. In this work, we have presented an inkjet-printed TRNG design that exploits the customizable fabrication feature of the PE to tune the circuit to mitigate the process variation impact. The proposed resistor tuning flow reduces the effect of the overall process variation by 110 times such that the tuned TRNGs can pass the NIST randomness test.

ACKNOWLEDGMENT

This work was supported by the Ministry of Science, Research and Arts of the state of Baden-Württemberg in form of the MERAGEM doctoral program.

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