CoDAPT: A Concurrent Data And Power Transceiver for Fully Wireless 3D-ICs

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***Abstract*—Three dimensional system integration is a promising enabling technology for realising heterogeneous ICs, facilitating stacking of disparate elements such as MEMS, sensors, analogue components, memories and digital processing. Recently, research has looked to *contactless* 3D integration using inductive coupling links (ICLs) to provide a low-cost alternative to conventional contact-based approaches (*e.g.* through silicon vias) for 3D integration. In this paper, we present a novel, fully wireless, ICL architecture for Concurrent Data and Power Transfer (CoDAPT) between tiers of a 3D-IC. The proposed CoDAPT architecture uses only a single inductor for simultaneous *power* transmission and *data* communication, resulting in high area efficiency, whilst facilitating low-cost, straightforward die stacking. The proposed design is experimentally validated through full wave EM and SPICE simulation and demonstrates capability to communicate data vertically at a rate of 1.3Gbps/channel (utilising an area of only 0.052mm^2) whilst simultaneously achieving power delivery of 0.83mW, under standard operating conditions. A case study is also presented, demonstrating that CoDAPT achieves an area reduction greater than 1.7× when compared with existing works, representing an important progression towards ultra low-cost 3D-ICs through fully wireless stacking.**

I. Introduction

Three dimensional (3D) system integration is a highly promising 'more-than-Moore' technology that facilitates high density integration by extending planar ICs vertically. A range of different 3D integration methodologies exist, however one of the most prevalent is the use of through silicon vias (TSVs) to interconnect stacked dies. TSVs, however, have been reported to suffer from reliability and yield issues, and their formation requires a number of additional processing stages [1]. This results in TSV-based 3D integration incurring high design and manufacturing costs [2]. To address this, recent research has explored the use of inductive coupling links (ICLs) to transmit data between vertically stacked dies. ICLs allow *contactless* 3D integration where data is transmitted purely by electromagnetic (EM) coupling between planar inductors fabricated in the back-end-of-line (BEOL) interconnect layers of each die. When adopting ICLs (for 3D integration), existing fabrication processes can be used without alteration, making them an attractive *low-cost* alternative to TSVs.

One challenge when using ICLs, however, is delivering *power* between tiers. Whilst existing ICL designs are useful for communicating *data* between dies, each die must still have its own power supply. This is typically achieved through using wire-bonding (to bond power ground and reset signals to each stacked tier [3]). For cases where many dies are stacked this becomes complicated, and intricate stacking patterns (such as *terraced* or *spiral-stair* stacking [3]) are required. This inflates the cost and complexity of devices, and the addition of wire bonds undermines many of the benefits associated with *contactless* integration.

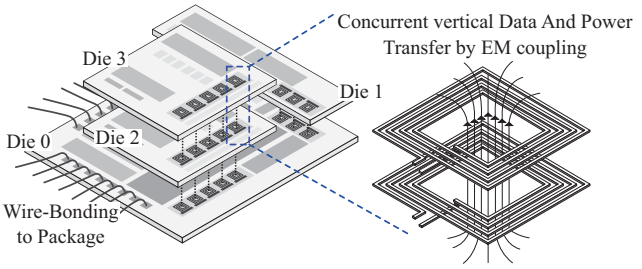

Fig. 1: Exploded illustration of fully wireless 3D-IC enabled by CoDAPT.

In this paper, we present an alternative approach, an ICL architecture that enables Concurrent Data And Power Transmission (CoDAPT) between stacked dies, using a single small-footprint inductor. The concept of CoDAPT is illustrated in Fig. 1: *fully wireless* 3D integration, whereby data and power are delivered vertically through a single inductive coupling channel. In achieving this, the novel contributions of this paper can be summarised as follows:

- A bi-phase shift-keying ICL transceiver architecture that achieves vertical *data* and *power* delivery concurrently within a 3D-IC.
- In-depth analysis of ICL inductor layouts focussing on the trade-off between power delivery efficiency and bandwidth, resulting in a high-coupling-coefficient (k = 0.36), high-bandwidth (1.3GHz) design.
- Validation of the proposed transceiver and layout demonstrating the capability to communicate data vertically at a rate of 1.3Gbps/channel whilst simultaneously achieving a power delivery density of 16.0mW/mm^2. This represents the most area efficient solution available for simultaneous *power* and *data* delivery in contactless 3D-ICs (more than 1.7× improvement on the state-of-the-art).
- Experimental evaluation of the effects of die-to-die misalignment (between stacked tiers) on the proposed approach, demonstrating that it can tolerate $\pm 28\,\mu\mathrm{m}$ of lateral displacement in x and y directions whilst maintaining power delivery performance within 10% of the optimum.

Experimental data used in this paper can be found at DOI:10.5258/SOTON/D0728 (https://doi.org/10.5258/SOTON/D0728).

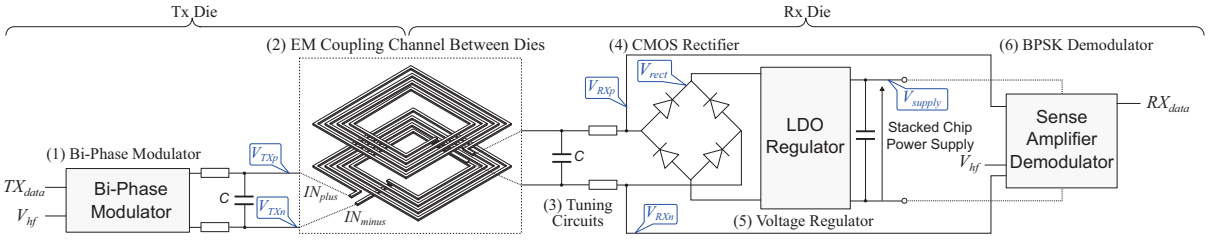

Fig. 2: Schematic diagram illustrating the proposed CoDAPT architecture.

II. Background

Contactless 3D integration, most notably using near-field inductive coupling to communicate data, has been proposed as a low-cost alternative to TSVs for designing 3D-ICs [2]. In such systems, data is encoded in a series of current pulses which are fed through a planar transmit (TX) inductor, fabricated in the upper BEOL interconnect layers of the transmitting die. These current pulses form a magnetic field, which is intersected by a second inductor fabricated in the receiving (RX) die, as illustrated in Fig. 1. According to the principle of electromagnetic induction, this causes a corresponding current (and hence voltage) to be induced in the recipient inductor which can be de-coded to recover the data.

Three dimensional integrated circuits constructed using this approach are widely reported [4]–[6], however only provide a contactless interface for *data* delivery between tiers. Because of this, 3D-ICs using ICLs often achieve power delivery through other separate means, the most common being wire-bonding. Wire-bonding is an adequate solution which achieves the goal of circumventing TSVs, however, the stacking arrangements required for such systems are intricate and complex (as outlined above), and undermine some of the benefits of *contactless* 3D integration which aims to be cheap, simple and robust.

One alternative to wire-bonding, for power delivery, is the use of Highly Doped Silicon Vias (HDSVs), proposed in [2]. HDSVs are vertical channels formed from highly doped wells to deliver power through dies after aggressive thinning. Whilst this is a promising future technology, it is yet to be practically realised and HDSVs will require a substrate thickness less than $5\,\mu\text{m}$ [2], likely introducing a number of physical challenges, in addition to significantly increasing the cost, beyond wire-bonded approaches. Another method of transferring power between vertically stacked dies is using wireless power transfer (WPT). Prior works report WPT of between 2.5mW [7] and 12.3mW [8] per channel within 3D-ICs. These works, however, use large inductors (separate to those for data transmission) that are often greater than $500\,\mu\text{m}$ in diameter [7], meaning that the entire contactless interface (for *power* and *data* delivery) can consume up to 1mm^2 of silicon area, or more, which is undesirably large.

III. Concurrent Power and Data Delivery Architecture

To address this challenge, as discussed in the introduction, the aim of the CoDAPT architecture is to facilitate *power* and *data* delivery concurrently using a single inductive channel. To achieve this, continuous bi-phase shift keying (BPSK) modulation will be used to ensure constant power delivery between tiers, irrespective of the TX data stream (unlike prior works which discretise transmission). Fig. 2 shows an overview of the proposed CoDAPT architecture, consisting of: (1) a bi-phase shift keying modulator, (2) the ICL channel, (3) tuning circuits to ensure that the system operates at resonance (to improve efficiency [9]), (4) a CMOS rectifier, (5) an LDO regulator (based upon a band-gap reference) to manage the received power supply for the recipient die, and (6) a sense-amplifier (SA) based coherent de-modulator. For the system to work correctly, each of these elements must be carefully designed to maximise *power* delivery efficiency, whilst still supporting *data* transmission. The entire system is designed for on-chip integration and will hence facilitate straightforward, low-cost 3D integration where dies can be fabricated, and then stacked, with no additional processing required. The design of each element is documented below.

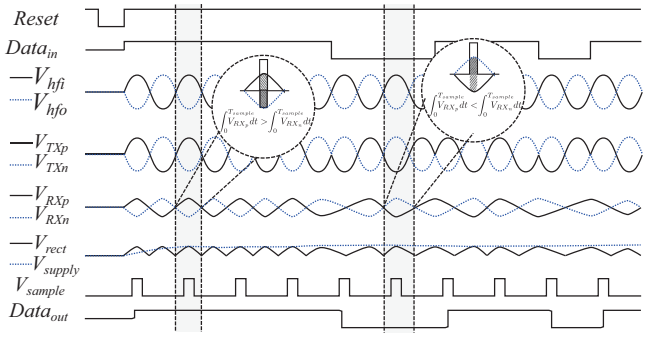

Fig. 3: Operation of CoDAPT: V_{hfi} and V_{hfo} are the *in* and *out-of* phase carriers, V_{rect} is the rectified RX signal, V_{supply} is the RX supply and V_{sample} is the SA sample window.

A. Bi-Phase Transceiver Design

Fig. 3 illustrates the BPSK modulation scheme proposed for use in this work. The CoDAPT architecture is differential and the modulator operates by selectively driving the in-phase or out-of-phase (180° shifted) carrier around the coil in accordance with the TX data stream. Fig. 4 illustrates the proposed modulation circuit required to realise this transmission. Here, V_{hf_i} is the in-phase high frequency carrier signal, V_{hf_o} is the shifted carrier signal, and IN_{plus} and IN_{minus} are the driving ports for the ICL channel. The modulation circuits operate at nominal voltage (1.2V) to minimise power dissipation,

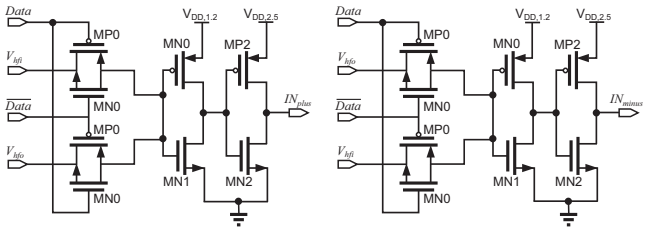

Fig. 4: Schematic diagram of proposed CoDAPT bi-phase keying modulator

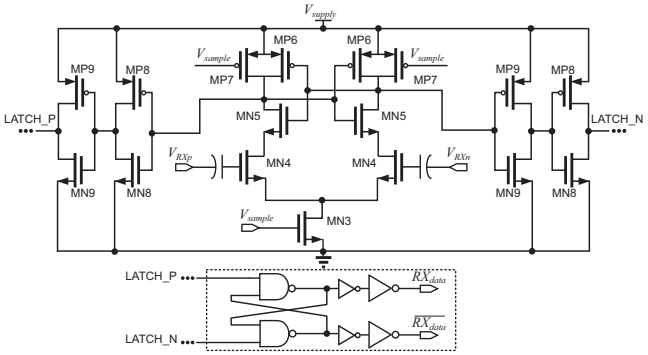

Fig. 5: Schematic diagram of proposed CoDAPT sense-amplifier based de-modulator.

however to maximise the RX pulse amplitude the coils are driven by MN2 and MP2 which connect to a 2.5V supply. Fig. 5 shows the proposed corresponding demodulator design, based on a sense amplifier (SA) [10]. The operation of this circuit is illustrated in the dashed circles in Fig. 3. The SA will sample the differential received signal, V_{RX_n},V_{RX_p} in the interval T_{sample}. In the case the at a '1' has been transmitted

$$\int_0^{T_{sample}} V_{RX_p} dt > \int_0^{T_{sample}} V_{RX_n} dt \tag{1}$$

and hence, LATCH_P will be pulled high by the differential pair (MN4) and a '1' will be latched at the output. Conversely, as shown on Fig. 3, if a '0' has been transmitted

$$\int_0^{T_{sample}} V_{RX_p} dt < \int_0^{T_{sample}} V_{RX_n} dt \tag{2}$$

as the sampling period aligns with a peak in the V_{TX_n} signal. In this case, the differential pair will pull LATCH_N high, and hence a '0' will be received. The sensitivity of this sense amplifier is determined by the width of MN4.

One of the main sources of power dissipation in CMOS circuits is dynamic power consumption. Because of this, a trade-off between power *delivery* and power *efficiency* exists within the transceiver: When operating at a higher frequency, the variation in magnetic flux will be greater, allowing more power delivery between coils. When operating at higher frequency, however, the dynamic switching power dissipation will be much greater. To strike a balance between these two factors, a carrier frequency of 2GHz was selected. This represents a sufficiently high frequency for meaningful power transfer,

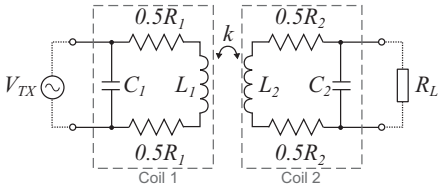

Fig. 6: Equivalent circuit model of an ICL channel [13] which assumes that each coil can be accurately modelled by its resistance (R_i), capacitance (C_i), inductance (L_i).

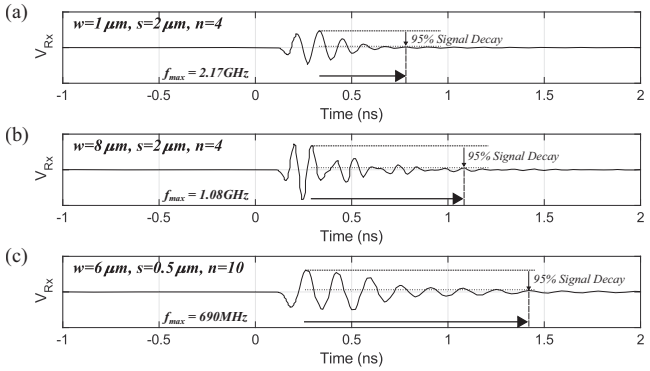

Fig. 7: Illustration of the effects of physical layout parameters (track *width*, w, track *spacing*, s, and *number of turns*, n) on the RX voltage signal for 3 example cases.

whilst remaining in the operating tolerances of the 65nm technology (used for implementation in this work), hence minimising dynamic power dissipation.

B. Inductive Channel Design

The second element in the CoDAPT architecture is the inductive coupling channel itself, consisting of two coupled planar inductors. Power transmission between two stacked inductors is optimised when their layouts are congruent [11]. Therefore, two congruent square spiral inductors are considered in this paper (as square inductors offer the highest inductance per unit area [12]). As the aim of CoDAPT is to enable concurrent wireless data and power delivery with a low area overhead, a maximum inductor area of 0.04mm^2 was selected, representing a 2.5× reduction compared to state-of-the-art works exploring WPT in 3D-ICs [8].

Fig. 6 shows an equivalent circuit model of an inductive coupling channel where each inductor, i, is modelled by its self-capacitance C_i, resistance, R_i, inductance, L_i and the EM coupling coefficient k that exists between the inductor pair. From this model, an equation for the power delivery efficiency, η_{pow}, (power-out/power-in) of a given link can be derived in terms of C_i, R_i, L_i, k and the link's excitation frequency. This is shown in Footnote 1. As the channel in this work will be used to transmit *data* (in addition to power), consideration must also be given to the coil's RC parasitics. Whilst coil layouts with high numbers of turns, and small intra-turn spacing may maximise η_{pow}, these result in high self-capacitance which can cause inter-symbol interference

[1] $\eta_{pow} = \omega^2 M^2 R_L / \Big\{ {R_L}^2 \left[\left(\omega^4 {C_2}^2 \left(R_2 M^2 + R_1 {L_2}^2 \right) \right) + \omega^2 \left(R_1 \left({C_2}^2 {R_2}^2 - 2 C_2 L_2 \right) + \left({L_2}^2 R_1 + M^2 \left(R_L + R_2 \right) \right) \right) \right] + R_1 \left(R_L + R_2 \right)^2 \Big\}$ (3)

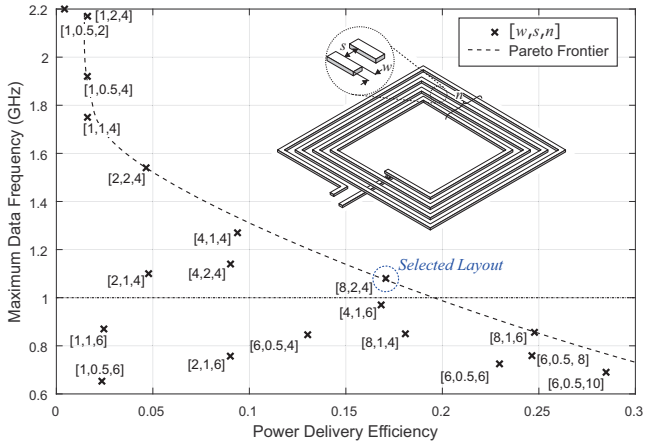

Fig. 8: Trade-off between power efficiency and maximum operating frequency, including pareto-optimal frontier (only a small sample of layouts are presented here for clarity).

(ISI) when transmitting data.

This effect is illustrated in Fig. 7. Here, three transient simulations are presented illustrating the received voltage signal (responding to a square transmit pulse at 0ns) when transmitted through an ICL channel where the inductor layout parameters: track *width* (w), track *spacing* (s), and *number of turns* (n), vary between (a) and (c). As can be observed, the layout in Fig. 7 (a) has fewer turns and a large turn spacing meaning parasitics are low, and the pulse smearing is minimal. Conversely, Fig. 7 (c) uses 10 turns with a small turn-spacing, meaning that the self-capacitance of the coil, C_i, is high. As a result the signal duration is much longer.

Fig. 8 illustrates the trade-off between power delivery efficiency, η_{pow}, and the maximum data bandwidth supported by the link for a small number of selected layouts. The maximum data bandwidth was calculated from the inverse of the 95% decay point shown in Fig. 7. To select an inductor layout for use in CoDAPT, the pareto frontier was added to Fig. 8 and an arbitrary minimum bandwidth of 1GHz was defined, to remain competitive with prior ICL data links [6]. The layout with the highest power delivery efficiency, whilst meeting this target, was then selected with w = 8 µm, s= 2 µm and n=4. This corresponds to a resistance of 5.48 Ω, k, of 0.36 and a capacitance of 36.7fF when mapped to the model in Fig. 6.

C. Tuning Circuit Design

Although the generation of this optimised layout includes consideration for the link's operating frequency, the resistance R and capacitance C of the coil may only be selected from a finite number of RC combinations that correspond to real, physical inductors. Because of this, the performance of the system can be 'fine-tuned' by adding a series-parallel tuning circuit before and after the coil, as shown in Fig. 2. In order to ensure maximal power delivery between tiers within the 3D-IC, the link should operate at resonance [9]. In this case, resonant operation also ensures that the received voltages are sufficient to allow direct LDO regulation (to the nominal 1.2V) without requiring an additional boost converter. In

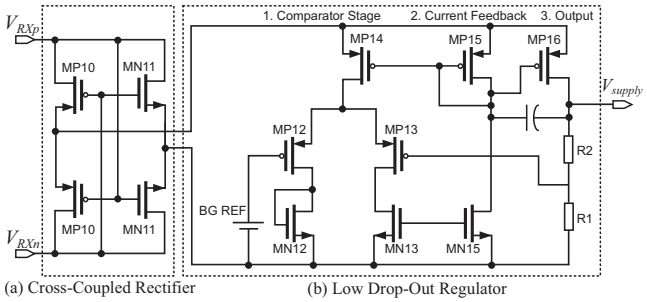

Fig. 9: Schematic diagram of (a) Cross-coupled CMOS rectifier and (b) Low drop-out voltage regulator circuit.

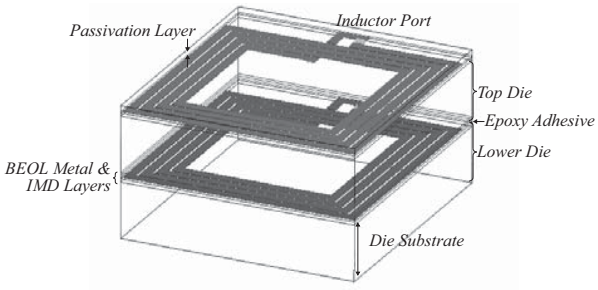

Fig. 10: 3D Illustration of stackup used for EM simulation.

this implementation, no alteration is made to the resistance, however a small tuning capacitor C is added in parallel with the coil, as shown on Fig. 2, to achieve resonance at 2GHz.

D. Rectifier and Low Drop-Out Regulator Design

To rectify the received BPSK signal (and hence recover the transmitted power), a CMOS cross-coupled rectifier is used as illustrated in Fig. 9 (a). Work by Han *et al.* [9] presents extensive comparison of available on-chip rectifier solutions for this style of application, concluding that a cross-coupled rectifier can provide the highest efficiency [9]. Following this rectification stage, a low-drop-out regulator is incorporated in order to regulate the power supply in the recipient die. This is shown in Fig. 9 (b). The regulator operates on the principal that as the voltage (V_{supply}) rises, the comparator stage (2) (that compares V_{supply} to the band-gap reference, BG REF) will cause the gate voltage of MP16 to increase, hence increasing the resistance across it. This will have the effect of limiting the supply voltage to the pre-defined value (set by R_1, R_2). The size of the storage buffer (placed at the output, V_{supply}) for experiments in this paper was selected to be 1pF.

IV. Results and Evaluation

A. Experimental Set-Up

Combining each of these components, the proposed architecture was experimentally validated using commercial simulation tools. The layout was imported to Ansys HFSS for EM simulation of the channel, using the stack-up in Fig. 10. Here, the default metal (and corresponding dielectric) layer thicknesses associated with the TSMC 65nm technology are used (passivation = 2 µm, metal = 0.9 µm) and the epoxy thickness is assumed to be 2 µm. The only additional processing assumed is wafer thinning to 50 µm, in-line with realistic

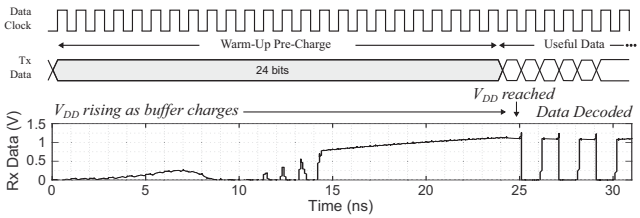

Fig. 11: Transient simulation of CoDAPT start-up sequence.

METRIC OF PERFORMANCE	VALUE
Area (Including Inductors)	0.052mm^2
Bandwidth	1.3GHz
Bit Error Rate (at 1Gbs)	$< 10^{-9}$
Latency (at 1Gbs)	1ns
Warm-Up Period (at 1Gbs)	24 bits
Peak Power Delivery (per channel)	2.1mW
Average Power Delivery (per channel)	0.83mW
Power Delivery Density	16mW/mm^2

TABLE I: Tabular summary of CoDAPT's performance.

fabrication capabilities. A fitted broadband SPICE model of the channel was exported for simulation of the link in H-SPICE (with the above outlined circuits). Results from these simulations are presented below.

B. Results

1) Start-Up: Initially, the start-up behaviour of the CoDAPT system was assessed. As the recipient die is powered directly from the communicated data signal when using CoDAPT, there is a small period of time where the energy buffer must charge. Fig. 11 shows the transient performance of the proposed system during this time. Here, a current sink of 0.5mA (representing extraneous circuits in the recipient die) is applied. The *warm-up* period required to ensure robust operation of the ICL data transceiver under these conditions was determined to be approximately 24ns (24 bits at 1Gbps).

2) Data Delivery Performance: After the warm-up period has elapsed, this transceiver was found to exhibit a maximum bandwidth of 1.3Gbps, slightly larger than the theoretical maximum suggested on Fig. 8. The bit error rate (BER) of the proposed transceiver when operating at the target frequency (1GHz) was found to be $<10^{-9}$. The latency, at the same testing frequency, was determined as 1 clock cycle.

3) Power Delivery Performance: The stability of the supply voltage when using the CoDAPT architecture was then assessed. For normal operation (assuming the transmission of an equiprobable random binary bit sequence) the maximum deviance in the recovered supply voltage (1.2V) was measured to be 7%. The instantaneously delivered power reached 2.1mW under ideal conditions, however the average power for typical operation was determined to be 0.83mW (as there is a slight dependency between the delivered power and the TX data-stream)[2]. These metrics are summarised in Table I.

The power and area overheads of the CoDAPT approach were also evaluated. To ascertain the silicon footprint of the approach, physical layout of the CoDAPT transceiver was performed using TSMC 65nm LP CMOS technology. The itemised results are shown in Table II.

[2]Quoted figures are inclusive of the CoDAPT circuitry power dissipation (including data recovery) and carrier signal generation.

COMPONENT	POWER	AREA (65nm technology)
TX/RX Inductor	N/A	0.04mm^2
Transmitter	6.59mW	840 µm^2
Receiver, Demodulator	2.47 µW	400 µm^2
Receiver, Regulation	0.661mW	11 600 µm^2
Total	7.16mW	0.052mm^2

TABLE II: Itemised summary of CoDAPT Overheads.

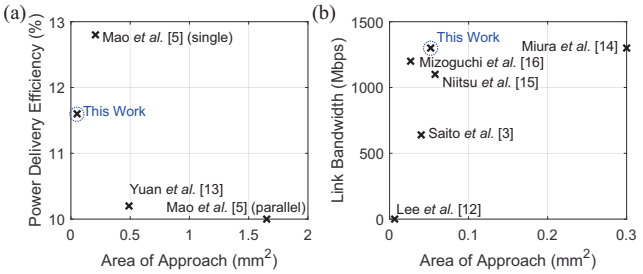

Fig. 12: Comparison of CoDAPT's performance against (a) WPT-specific prior works, and (b) data-specific ICL works.

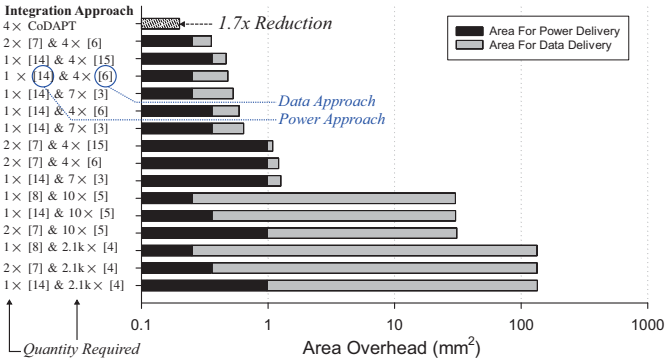

Fig. 13: Area overhead of existing *data* and *power* approaches compared with CoDAPT for the assumed integration scenario.

C. Advantages of the CoDAPT Approach

As discussed in the introduction, CoDAPT enables ultra-low cost 3D integration, where no additional processing is required due to the fact that both power and data are delivered wirelessly. Previously, fully wireless 3D integration could only be realised using combinations of WPT schemes and data ICLs, resulting in significant area overhead. CoDAPT addresses this by combining power and data delivery in the same circuits.

1) Comparison With Existing Work: Fig. 12 (a) compares the power delivery efficiency of the proposed approach against other works exploring WPT between stacked dies. Despite the fact that CoDAPT supports data transmission *in addition to WPT* (which is untrue of other approaches in the figure), CoDAPT is very competitive providing high efficiency (11.6%) with low silicon overhead. Fig. 12 (b) plots bandwidth against area to compare CoDAPT to existing data ICL implementations. Again, CoDAPT is highly competitive achieving the highest bandwidth-per-unit-area using the BPSK scheme.

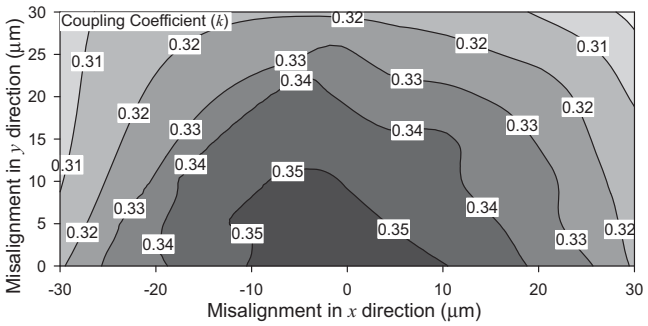

Fig. 14: Effects of lateral die-to-die misalignment on channel coupling coefficient (k).

As *concurrent* power and data delivery in 3D-ICs is a new concept, CoDAPT can only be compared fairly with *combinations* of existing data ICLs, and WPT schemes to achieve the same overall net effect. Therefore, for more in-depth comparison, Fig. 13 compares the area overhead of CoDAPT with combinations of data-ICL and WPT approaches assuming a use-case scenario of two stacked CPU systems communicating vertically through a 64-bit, 50MHz data-bus. Modelling each CPU as an Arm M0+ MCU results in a power delivery requirement of approximately 3.0mW [16] alongside the data bandwidth requirement of 3.2Gbps. To meet this specification using CoDAPT requires 4 links, resulting in an area overhead of 0.208mm^2. Fig. 13 shows the area overheads of contactless *power* and *data* delivery approaches that can be also combined together to meet this specification. From the figure, it can be observed that CoDAPT outperforms each approach in terms of area efficiency, by at least 1.7× through concurrent data and power transmission, demonstrating that CoDAPT is successful in achieving its aim.

D. Tolerance to Lateral Misalignment

Finally, this sub-section evaluates the performance CoDAPT when misalignment exists between stacked tiers. Fig. 14 illustrates the influence of lateral die-to-die misalignment on the coupling coefficient, k (*c.f.* Fig. 6). Fig. 15 translates these k values into power delivery performance values, expressed as a percentage of the average perfectly-aligned case (0.83mW). Setting a target performance tolerance of $\pm 10\%$, results show that the proposed design allows $\pm$ 28 µm of lateral misalignment in x and y directions (equating to a total offset of 39.6 µm, almost half of the coil's radius) whilst remaining within this target. Additionally, the proposed architecture can tolerate up to 37 µm of lateral misalignment in both directions, before significant degradation in data-transmission performance. When compared to the use of TSVs, this represents an order-of-magnitude improvement, as TSVs typically demand sub-micron alignment accuracy [17].

V. Conclusions

This paper presents a novel fully wireless ICL transceiver (CoDAPT), for 3D integration, where *data* and *power* can be concurrently delivered through a single channel. Thorough evaluation demonstrated that CoDAPT achieves a data-rate

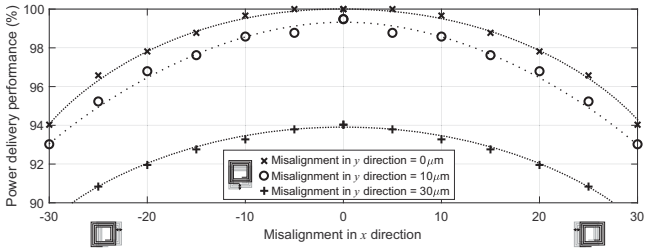

Fig. 15: Effects of lateral die-to-die misalignment on power delivery (normalised to 0.83mW).

of 1.3Gbps (BER$< 10^{-9}$) whilst simultaneously transferring 0.83mW of power per channel under typical operating conditions. For the integration scenario discussed in this paper, the area savings when using CoDAPT were in excess of 1.7× compared to the state-of-the-art. Results also demonstrate tolerance of $\pm$28 µm lateral die-to-die stacking misalignment, representing an important progression towards low-cost fully wireless 3D integration.

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