Adiabatic Implementation of Manchester Encoding for Passive NFC System

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***Abstract*—Energy plays an important role in NFC passive tags as they are powered by radio waves from the reader. Hence reducing the energy consumption of the tag can bring large interrogation range, increase security and maximizes the reader's battery life. The ISO 14443 standard utilizes Manchester coding for the data transmission from passive tag to the reader in the majority of the cases for NFC passive communications. This paper proposes a novel method of Manchester encoding using the adiabatic logic technique for energy minimization. The design is implemented by generating replica bits of the actual transmitted bits and then flipping the replica bits, for generating the Manchester coded bits. The proposed design was implemented using two adiabatic logic families namely; Positive Feedback Adiabatic Logic (PFAL) and Improved Efficient Charge Recovery Logic (IECRL) which are compared in terms of energy for the range of frequency variations. The energy comparison was also made including the power-clock generator designed using 2-stepwise charging circuit (SWC) with FSM controller. The simulation results presented for 180nm CMOS technology at 1.8V power supply shows that IECRL shows approximately 40% less system energy compared to PFAL family.**

Keywords— adiabatic logic technique, manchester encoding power-clock, passive NFC system , radio waves

I. INTRODUCTION

The use of adiabatic logic technique instead of the non-adiabatic logic design can considerably decrease the energy consumption in a large system [1]-[2]. Though it is in existence for more than two decades, still, its full potential has not been explored. One of the significant works was done by Teichmann [3], where the author designed various arithmetic circuits and implemented an adiabatic CORDIC-based DCT as a test vehicle to demonstrate the system level applicability of adiabatic logic for ultra-low-power digital signal processing [4]. In [5] the behavior of adiabatic logic circuits in weak inversion or subthreshold regime is analyzed. Through extensive post-layout simulation, it demonstrated that subthreshold adiabatic circuits can save significant energy compared with an equivalent non-adiabatic implementation. Over the years, adiabatic logic technique has also found its application in power-analysis attack resilient secure logic [6]-[8]. Recently, a VHDL based modelling approach for precise timing analysis for 4-phase adiabatic logic families have also been proposed [9]. All the above cited work vouches the applicability of adiabatic logic technique in reducing the energy dissipation. However, according the authors best knowledge, none has described the adiabatic logic technique for data transfer application for wireless communication technology.

The power resource plays an essential role in the tag properties since the energy source of the reader specifies the life time, cost and mainly the tag's potential read range; also, this factor determines the functionality that a tag can provide. Moreover, the increased hardware complexity due to add-on functionalities, such as security and data-storage [10] has the associated cost in terms of high energy dissipation in passive NFC tags. When the tag comes near the reader, it initiates the communication by modulating its field. This enables the signals to be transmitted from the reader to the tag and vice-versa by means of different coding techniques. Miller coding is used to transmit signal from the reader to the tag, whereas, Manchester coding is used for data transfer from tag to the reader. Thus, in case of increased number of retransmissions when a reader detects an error in tag-to-reader data transfer [11] it causes the energy dissipation in a passive NFC system to increase. Therefore, we propose a method for Manchester encoding technique using 4-phase adiabatic logic for energy minimization.

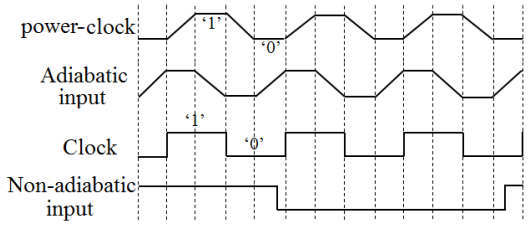

Fig. 1. Adiabatic and non-adibatic signals representations.

In adiabatic logic, waveforms are more complex because of the multi-phase clocking and the dual-rail encoding of inputs and outputs. Thus, in addition to logic '1' and logic '0', the adiabatic power-clock supply uses two more logic levels where the power-clock transition is a ramp such that all the four levels share the same period. Whereas, in the sequential non-adiabatic logic circuits a constant (DC) power-supply (logic '1') is used. The sequential logic is one which has clock as one of the inputs and works either at the rising or falling edge of the clock input. However, the major difference between the two lies in the fact that in adiabatic logic technique, data (input) and the power-clock have the same frequency of operation with same ramping time. However, in sequential non-adiabatic logic the data and the clock have different time interval. In non-adiabatic logic, the clock is a

freely running pulse train with fixed time period whereas, input do not have a fixed time period. Fig. 1 shows the representation of the signals using adiabatic and non-adiabatic logic.

The paper is structured as follows; Section II describes the adiabatic logic technique and its associated challenges. Manchester encoding using adiabatic logic technique is presented in section III. Section IV presents the implementation and simulation results. The paper is concluded in section V.

II. ADIABATIC LOGIC TECHNIQUE

The term '*adiabatic'*, is of Greek origin and refers to a system in which a transition occurs without energy/heat being either lost to or gained from the system. To have less dissipation, the adiabatic logic circuit uses a slowly changing power-supply/clock -the so-called "power-clock" to evaluate the function, allowing approximately constant current charging/discharging and avoiding current surges [12]. Decreased energy dissipation with increased switching time is, therefore, the defining property of an adiabatic switching. In addition, this slowly charging process gives an additional advantage of pumping the stored energy back to the power supply during the discharging process which can be recovered using a power-clock generator [13], [14].

$$E_D = (RC_L/T_r)\, C_L V_{DD}^2 \qquad (1)$$

Where E_D is the energy dissipation, T_r is the ramping time, C_L is the effective output load capacitance, R is the charging path resistance and V_{DD} is the supply voltage. It should be noted that the above equation doesn't take into account the energy loss due to leakage and threshold voltage degradation known as non-adiabatic loss (NAL). The detailed derivation of (1) is given in [12]. Fig. 2 shows the 4-phase power-clock broken down into four equal time periods with each having 90° phase difference.

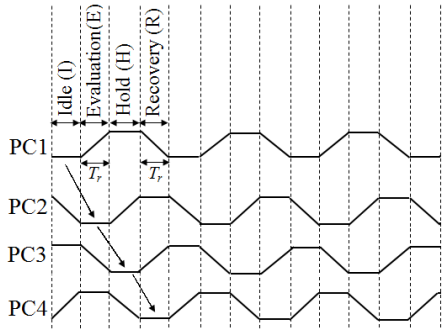

Fig. 2. 4-phase power-clocking scheme.

Based on the comparison results [15], the 4-phase adiabatic system is the most promising in terms of performance and energy requirement compared to single and 2-phase power-clocking adiabatic logic scheme. The 4-phase adiabatic logic is implicitly pipelined and glitch-free. This suggests that there is no concern about the critical paths.

III. NOVEL MANCHESTER ENCODING METHOD

The idea behind the passive NFC system is the use of radio frequency (RF) for contactless power transfer and communication when contacting a reader wirelessly with the integrated circuit embedded in a tag. In these systems, the data through modulation is transmitted between the tag and reader. The data is encoded in order to reduce error rate and improve efficiency before being modulated. In general, the Manchester codes are used as described in part 3 of ISO/IEC 14443A whenever the data from the tag to the reader is transmitted [16]. At the receiver side (reader), the Manchester decoding is done to recover the data and the clock.

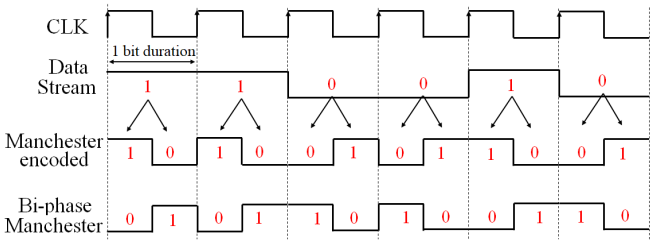

Fig. 3. Manchester encoding waveform

Manchester encoding is a synchronous clock encoding technique to encode the clock and data of a synchronous bit stream [17]. In the Manchester encoding, the logic '1' is indicated by a '1' to '0' transition and logic '0' is indicated by a '0' to '1' transition. Manchester code is also called as bi-phase code, where the logic '1' is encoded as transition from '0' to '1', and vice versa. Here, for both the above cases, the signal transitions always occurs at the center of each bit duration. The absence of expected signal transition at the center can be used for error detection. The waveform for a Manchester encoded bit stream '110010' is shown in Fig 3. The typical implementation of Manchester encoding requires an exclusive OR (XOR) function between the clock (CLK) and the data bit stream. To use the same method using adiabatic logic is challenging because;

1) The input and the power-clock both have the same time-period (frequency), only having 90° phase difference.

2) Secondly, if the two different power-clock frequencies are used in the same circuit then we may require to generate them separately which will add on to the energy consumption.

3) Finally, the use of two different frequencies will voilate the adiabatic principle and will also cause the energy to increase.

Therefore, a different method and hardware is proposed for encoding the data such that the long string's of 1's and 0's are avoided. One advantage of the adiabatic implementation is that since the input bit stream has the same frequency as that of the power-clock, the clock and the data can easily be extracted at the receiver side. Fig. 4 shows the manchester encoding using the proposed method. The method is described as follows;

Step 1: Data bit stream is stored into the adiabatic register unit.

Step 2: Using a 2-state counter, each bit from the register is read twice in consecutive cycles, such that each bit from the actual data stream is replicated and forms a bit pair.

Step 3: The complement of the replicated bit stream is generated The replicated bit stream and its complement are multiplexed to form Manchester coded data bit stream.

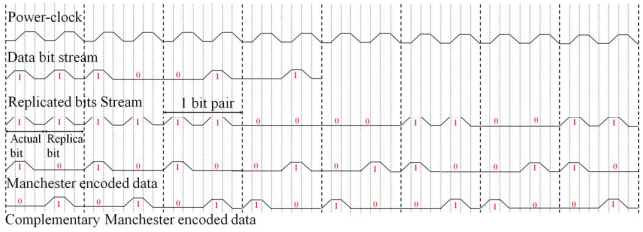

Fig. 4. Proposed Manchester encoding for adiabatic logic.

The hardware requirement for the proposed manchester encoding is as simple as the basic method. However, the proposed method requires few more logic gates for replicating the bit stream and then multiplexing it for generating the manchester encoded data. Nonetheless, adiabatic logic has an advantage over conventional CMOS due to its dual-rail output, generating both manchester and bi-phase encoded data.

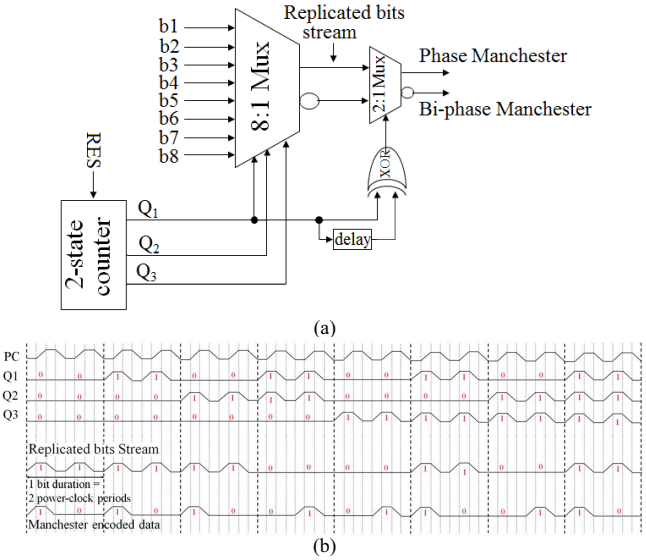

Fig. 5. Proposed Manchester encoding design output waveform.

For generating the replica bits, the proposed method uses a two state counter which remains in the same state for two power-clock cycles. Then the extended data bit stream and its complementary data stream are multiplexed. The manchester encoded signal is generated by sequentially turning the switch on and off between the data bits stream and complementary data bits stream. The select signal to the 2:1 multiplexer is generated by the XOR operation between the LSB bit of the counter and its delayed bit to maintain synchronization between the bit stream and the counter. The adiabatic design of the manchester coding for 8 bit data stream is shown in Fig. 5 (a), whereas, Fig. 5 (b) shows the corresponding outputs of 2-state counter, double bits stream and manchester coded signal. The input bits stream b1-b8 is taken as '11100101' as an example. To the authors best knowledge, this is the first time Manchester encoding using adiabatic logic technique is proposed and implemented.

IV. Simulation Results

The 4-phase PFAL and IECRL are chosen for the SPICE simulation based on the author's previous work [15]. The SPICE simulations were performed with Spectre simulator using Cadence EDA tool in a 'typical-typical', TT process corner using TSMC 180nm CMOS process at 1.8V power supply. The transistor sizes for both are set to the technology minimum ($W_{min}=W_n=W_p=220nm$, $L_{min}=L_n=L_p=180nm$).

The implementation of Manchester encoding is a part of initialization and anti-collision specified in ISO standard 14443-3, thus the energy dissipation was measured as the energy per cycle for 40 data bits [16]. The energy measurement is taken at 1MHz, 10MHz and 100MHz frequencies for a load capacitance of 10ffF. Table I shows that IECRL implementation has the lowest energy compared to PFAL. The increment in PFAL energy is not significant from 1 MHz to100MHz in comparison to IECRL. Though table I shows IECRL consumes minimum energy but as the load capacitance is increased, its energy consumption will increase due to the non-adiabatic losses occurring during both the evaluation period and the recovery period [1], [15]. Nevertheless, this comparison is incomplete without taking consideration of the power clock generator.

TABLE I. Energy comparison of PFAL and IERCL Family

	Energy Consumption per power-clock cycle (fJ)		
Frequency (MHz)	1	10	100
PFAL	253.30	253.78	310.38
IERCL	119.98	119.46	304.77

Unlike conventional CMOS, adiabatic circuits are powered from the clock, requiring a separate "power-clock" supply. A power-clock will consume a significant amount of the energy (analogous to the clock generation in conventional CMOS). It is important to bear in mind that power-clock circuitry will be able to supply power to considerably more circuitry than the Manchester encoded design presented here. Nevertheless, it is appropriate to consider its energy too, which is often neglected in the papers on adiabatic logic technique presented in literature. Power-clocks can be generated either using a capacitor-based Stepwise-Charging (SWC) circuit [14] or inductor-based resonant circuit [13]. Since the inductor-based circuit occupies a large area it is not suitable for NFC application. Thus, an SWC based power-clock generator is used, as found in [14].

The simulation was performed for the 2-step power-clock frequency of 10MHz (ramping time of 25ns) supply-voltage 1.8V and 10fF capacitive load attached to the output of an adiabatic core [14]. The reference clock is taken to be 40 MHz for generating the power-clock frequency of 10MHz. The tank capacitance chosen for all the logic families is 5pF. The aspect ratio of the 2-step-charging circuit for both the logic families are taken same in order to differentiate between the energy efficient logic designs.

TABLE II. ENERGY COMPARISON OF THE COMPLETE ADIABATIC SYSTEM @ 40MHZ CLK FREQUENCYAND 10 MHZ POWER-CLOCK

	Energy Consumption per power-clock cycle (pJ)		
Frequency (MHz)	Controller	SWC+Core	Total
PFAL	1.040	1.524	2.565
IERCL	1.002	1.098	2.10

Table II reports the energy consumed by the adiabatic system including the power-clock generator for encoding data bits stream into Manchester code. As the adiabatic core represents the load to the SWC, the energy is measured for the controller and the SWC by measuring the current at the supply voltage (V_{DD}). It is also worth to be noted from Table II, that the energy consumption of the controller for SWC is almost constant for all system size [3]. More importantly, the energy consumption of the SWC for PFAL family is approximately 40% more in comparison to IECRL. This is due to the evaluation network of PFAL family connected between the power-clock and output [1] which adds on the extra load capacitance of minimum two nMOS transistors (drain terminal) connected to the power-clock. As a result, PFAL presents a large load to SWC, although showing a decrease in output impedance.

V. CONCLUSION

The paper presents a novel method of encoding data bits into Manchester coding using adiabatic logic technique. The proposed implementation generates Manchester as well as bi-phase Manchester encoded data simultaneously as it is implicitly dual-rail logic. Moreover, adiabatic logic does not require clock signal to be exclusive XOR with the data bits since the power-clock and the input have the same frequency. At the receiver side, the decoding of the received Manchester coded data take place, where the real data and the clock is decoded and will be checked for collision. The only disadvantage the proposed method has is that it doubles the bit duration which makes the proposed method applicable for NFC application working at few MHz frequency ranges. It is concluded that IECRL consumes less energy compared to PFAL at 10fF load capacitance. If the load capacitance increases the IECRL adiabatic core energy will increase [15] but it is anticipated that the overall system energy will not be more compared to the PFAL family.

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