Single-Event Double-Upset Self-Recoverable and Single-Event Transient Pulse Filterable Latch Design for Low Power Applications

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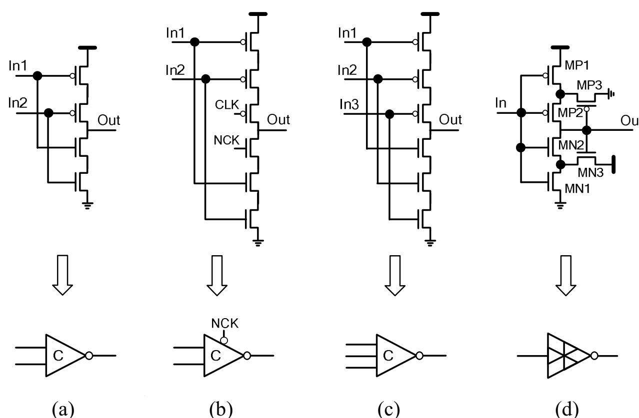
***Abstract*—This paper presents a single-event double-upset (SEDU) self-recoverable and single-event transient (SET) pulse filterable latch design for low power applications in 22nm CMOS technology. The latch mainly consists of eight mutually feeding back C-elements and a Schmitt trigger. Simulation results have demonstrated both the SEDU self-recoverability and SET pulse filterability for the latch using redundant silicon area. Using clock gating technology, the latch saves about 54.85% power dissipation on average compared with the up-to-date SEDU self-recoverable latch designs which are not SET pulse filterable at all.**

I. Introduction

In advanced nanoscale CMOS technology, radiation effect can easily result in soft errors due to the striking of high energy particles like neutrons, protons and alpha particles [1]. Recently, researchers have pointed out that high energy electron can also result in a soft error [2]. The soft error is of transient error resulted from particle-striking induced transient fault, and as the scaling of technology, soft error issue is becoming more serious for circuit reliability design [1, 3]. This implies that the logic state of a circuit node becomes more easily disturbed by particle-striking in silicon [1, 4].

Researchers indicated that single-event upset (SEU), single-event double-upset (SEDU) and single-event transient (SET) are the main types of soft errors, and as technology scaling, these effects dominate the radiation response of circuits [4]. As regards a storage cell, in deep-submicron technology, particle-striking may result in state change of only one node inside the cell, which is referred to as an SEU. However, in advanced nanoscale CMOS technology, particle-striking may result in state changes of double nodes inside the cell, which is referred to as an SEDU. On the other hand, particle-striking may result in a transient pulse at the output of a logic gate in a combinational block, which is referred to as an SET. If an SET propagates through logic gate cells arriving at a storage cell, it may be captured by the storage cell.



(a) (b) (c) (d)

Fig. 1. Widely used components for radiation hardened latch designs. (a) 2-input C-element. (b) Clock gating based 2-input C-element. (c) 3-input C-element. (d) Schmitt trigger.

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As regards SEU hardening, in recent years, researchers have proposed a series of hardened schemes to effectively tolerate an SEU [3, 5-18]. Using redundant hold nodes or techniques like transistor resizing and dual-modular redundancy, most of the above hardened schemes can robustly retain data against SEUs. Note that, among these hardened schemes, using temporal redundancy, some are also SET pulse filterable especially for latch designs in [14-16, 18]. However, only SEU and/or SET hardening are not sufficient for nanoscale CMOS technology. The very large scale integration and aggressively scaled transistor sizes and supply voltages can allow particle-striking induced single-event charge collection to affect double nodes and cause an SEDU [19]. Researchers indicated that SEDUs are becoming more prominent especially in harsh radioactive environments and soft error rate resulting from SEDU is rising [20-21]. Hence, existing SEU and/or SET hardened schemes are not robust facing to SEDU, and cannot be applied to circuits and systems requiring higher reliability.

As regards SEDU hardening, researchers have recently proposed a series of hardened schemes to effectively tolerate an SEDU [5, 19, 21-28]. To tolerate an SEDU, enlarging transistor sizes seems a feasible method, but weak node pairs can also be flipped when the energy of the radiation particle is large enough. Meanwhile, the layout solutions like well isolation and node spacing increase can also make a circuit SEDU tolerant, but these techniques can increase the complexity of integrated circuit designs [25]. Hence, an efficient way to tolerate SEDUs relies on radiation hardening by design (RHBD) technique using multiple-modular redundancy or redundant hold nodes and accordingly, integrated circuit designers have recently proposed many more reliable latch designs to fully tolerate SEDUs. However, the recently proposed SEDU hardened latch designs also suffer from some problems like whether they are SEDU self-recoverable, whether they are also SET pulse

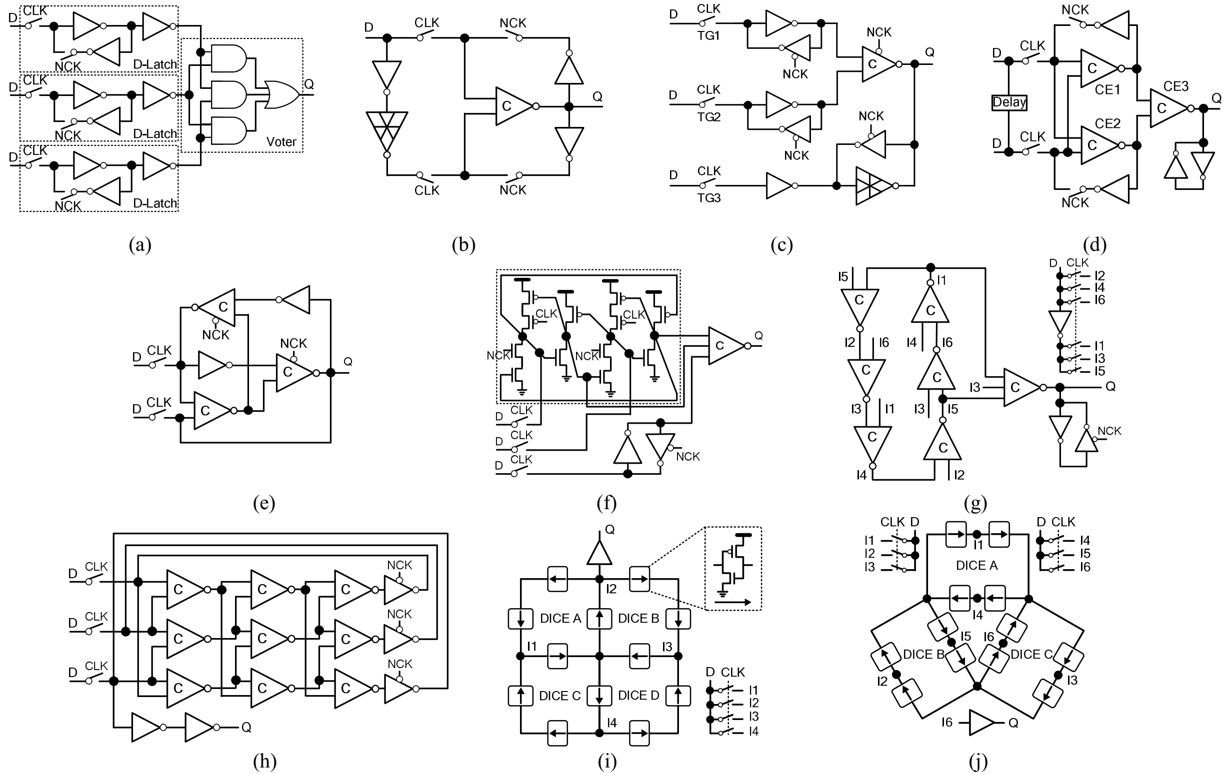

Fig. 2. Schematics of the reviewed previous hardened latch designs. (a) TMR [13]. (b) DET-SEHP [14]. (c) LCHR [15]. (d) FERST-EV [16]. (e) RFC [17]. (f) CLCT [24]. (g) DNCS [25]. (h) NTHLTCH [26]. (i) DONUT [27]. (j) DeltaDICE [28].

filterable or whether they are cost effective.

In this paper, an SEDU self-recoverable and SET pulse filterable latch design is proposed. Using eight mutually feeding back C-elements and a Schmitt trigger, the latch is not only SEDU self-recoverable but also SET pulse filterable with low power. Simulation results have demonstrated the SEDU self-recoverability and SET pulse filterability for the latch.

The remainder of the paper is organized as below. In Section II, we review examples of previous hardened latch designs. In Section III, the latch circuit and simulations will be presented. In Section IV, we quantitatively show the comparison results for overheads, followed by conclusions in Section V.

II. Previous Hardened Latch Designs

Fig. 1 presents the widely used components of hardened latch designs. As regards a 2-input C element (CE), it behaves as an inverter if all inputs are identical and it retains its previous value if all inputs become different. As regards the clock gating (CG) based, its behavior can also be controlled by clock signals and we would discuss Schmitt trigger in Sec. III. Fig. 2 shows the schematics of the reviewed SEU, SEDU and/or SET hardened latch designs.

The TMR latch [13] uses three D-latches and a voter to tolerate any SEU; however, an SEU may be kept in any D-latch. Besides, the latch cannot tolerate an SEDU and SET pulse.

The DET-SEHP latch [14] mainly uses a Schmitt trigger for SET pulse filtering and a CE feeding back to its inputs for SEU tolerance. However, if there is an SEU at Q or an SEDU at two inputs of the CE, the latch would retain invalid value.

The LCHR latch [15] employs a Schmitt trigger to filter an SET pulse and uses keepers to tolerate an SEU/SEDU. However, if there is an SEDU at the inputs of the CE, the latch cannot tolerate.

The FERST-EV [16] latch uses temporal redundancy to filter an SET pulse and uses two interlocked feedback loops connecting to CE3 as presented in Fig. 2-(d) to tolerate an SEU. However, if there is an SEDU at the inputs of CE3, the latch cannot tolerate as well.

The RFC latch [17] mainly employs three interlocked and mutually feeding back CEs to achieve SEU self-recoverability. However, if the outputs of two CEs are flipped due to an SEDU, the latch would retain invalid data. Besides, the latch cannot filter an SET pulse.

The CLCT latch [24] uses a CG based DICE cell and a D-latch connecting to a 3-input CE to tolerate an SEDU. However, there is at least one node pair which is not SEDU self-recoverable and the latch cannot filter an SET pulse.

Using a large feedback loop connecting to a 3-input CE, the DNCS latch tolerates any SEDU [25]. However, similarly to the CLCT latch, the latch cannot provide good tolerance for SEDU and SET pulse.

The NTHLTCH latch [26] mainly employs nine 2-input CEs and three CG based inverters to achieve SEDU self-recoverability. However, the latch cannot filter an SET pulse as well.

The DONUT latch [27] comprises four interconnected DICE cells for providing enough redundant nodes to ensure SEDU

self-recoverability. However, the latch is not cost effective due to much current competition and cannot filter an SET pulse.

The DeltaDICE latch [28] uses three interlocked DICE cells to achieve SEDU self-recoverability; however, the latch has the same drawbacks compared with the DONUT latch. We would further quantitatively discuss the overheads in Section IV.

III. Proposed Hardened Latch Design

A. *Circuit Structure and Behavior*

The circuit structure of our proposed SEDU self-recoverable and SET pulse filterable (referred to as DURTPF) latch design has been presented in Fig. 3. Layout of the proposed DURTPF latch design has been presented in Fig. 4. As we can see, the latch design constructs from eight 2-input CEs CE1 to CE8, four transmission gates TG1 to TG4 and a Schmitt trigger at output stage. Note that among the CEs, CE2, CE4, CE6 and CE8 are CG based ones. In the latch, D is the input, I1 to I8 are the internal nodes, Q is the output and CLK and NCK are the system clock and negative system clock, respectively.

When CLK is high and NCK is low, the transmission gates are ON and the latch works in transparent mode of operation. In this mode, all the system clock and negative system clock related transistors in the CG based CEs are OFF. As we can see in Fig. 3, the inputs of both CE1 and CE5 are driven by D through TG2 and TG4, respectively, thus the output of CE1 and the output of CE5 can be known. Similarly, the inputs of both CE3 and CE7 are driven by D through TG1 and TG3, respectively, thus the output of CE3 and the output of CE7 can be known as well. In summary, we can firstly get the output of any CE among CE1, CE3, CE5 and CE7, respectively, since the inputs of these CEs are known.

As we can see in Fig. 3, the inputs of CE2 are driven by both the output of CE1 and the output of CE5, respectively, but the output of CE2 is blocked using CG technology. In this way, we can avoid current competition at the output of CE2 to save power dissipation. Similarly, the output of CE4, CE6 and CE8 is respectively blocked to save power dissipation as well. In summary, we can get all the inputs and output of any CE. On the other hand, since the output of CE7 is feeding back to the Schmitt trigger at output stage, we can get output of the latch and hence all the transistors in the latch are biased properly.

The reason for why the latch is SET pulse filterable when working in transparent mode of operation can be briefed as below. If an SET pulse arrives at D, obviously, the pulse would be firstly reversed by CE7 and then can be filtered by the Schmitt trigger. Here we only take a positive SET pulse (low-high-low) for example, the transistors MP1, MP2, MN3 in Fig. 1-(d) are pre-charged and biased properly, thus when D changes from low to high (rise stage), the output of the Schmitt trigger will not change until the drain of MN1 is discharged to low from high, which needs a period of time especially when the aspect ratios of MN1 and MN3 are larger. Within that period of time, D may change from high to low (fall stage), and obviously the output of the Schmitt trigger will not be changed. In summary, the SET pulse can be masked.

When CLK is low and NCK is high, the transmission gates are OFF and the latch switches to hold mode of operation. In this mode, all the system clock and negative system clock related transistors in the CG based CEs are ON, hence the outputs of the CG based CEs are prevented from being driven by D through the transmission gates and instead they are driven by the CG based CEs themselves, respectively. In this way, all the interlocked feedback loops in the latch are constructed to effectively keep values and the feedback rule for the CEs can be briefed as below, i.e., the output of any CE in the ordered and circulated CE list <CE1, CE2, CE3, CE4, CE5, CE6, CE7, CE8> is fed back to both one input of the next CE and one input of the triply prior CE. Finally, Q is robustly driven by the output of CE7 through the Schmitt trigger to keep values.

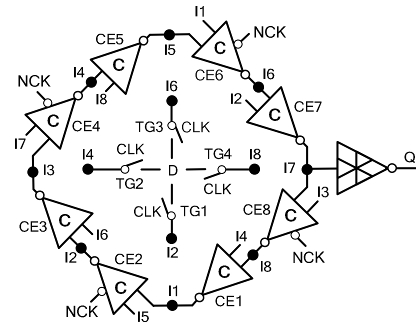

Fig. 3. Circuit structure of the proposed DURTPF latch design.

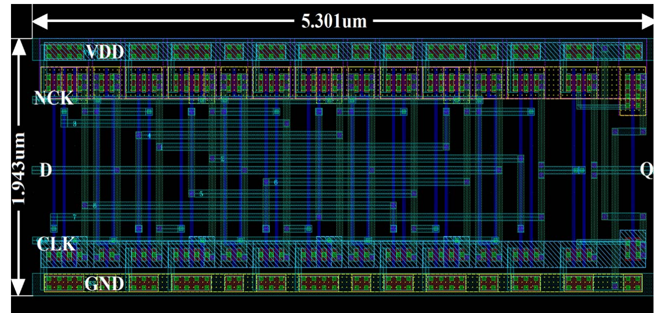

Fig. 4. Layout of the proposed DURTPF latch design.

In the presence of an SEU for the latch when it works in hold mode of operation, there are totally 9 cases because an SEU may affect any of the internal nodes I1 to I8 as well as the output of the latch. Here we take the case that an SEU affects I1 resulting in a glitch for example. According to the CEs' feedback rule, the glitch can propagate to one of the inputs of CE2 as well as one of the inputs of CE6, but CE2 and CE6 can intercept the glitch. On the other hand, because the SEU cannot affect the inputs of CE1, I1 can restore back the correct value through the correct inputs of CE1. This way, a conclusion can be drawn that the internal nodes of the latch can restore back the correct values from any SEU, and finally the output of the latch can restore back the correct value through the Schmitt trigger. In summary, all nodes in the latch eventually keep correct values, i.e., the latch is SEU self-recoverable.

In the presence of an SEDU for the latch when it works in hold mode of operation, any node pair should be considered. In the left circular structure, since any two of the internal nodes I1 to I8 can be affected by an SEDU no matter whether we

consider layout information or not, there are obviously totally $C_8^2=28$ cases in the presence of an SEDU. On the other hand, since the output of the latch and one of the 8 internal nodes I1 to I8 can also be affected by an SEDU, there are obviously other 8 cases in the presence of an SEDU. However, since the latch is SEU self-recoverable, as regards the just mentioned 8 cases in the presence of an SEDU, the internal node can firstly self-recover and the output node can secondly self-recover from the SEDU. Hence, the latch is SEDU self-recoverable for the 8 cases and we only have to prove that the left circular structure of the latch is SEDU self-recoverable (totally 28 cases) to ensure the SEDU self-recoverability for the latch.

As regards two adjacent CEs in the left circular structure of the latch, if we denote the node distance between their outputs as 'λ', we can get all output-node distances between CEs as and only as 'λ', '2λ', '3λ' and '4λ', respectively, since the CEs are ordered, circulated and symmetrical as presented in Fig. 3. Hence, we only need four indicative node pairs such as <I1, I2>, <I1, I3>, <I1, I4> and <I1, I5> for the 28 cases in the presence of an SEDU to prove the self-recoverability for the latch.

In the presence of an SEDU for <I1, I2> resulting in glitches, according to the above-mentioned CEs' feedback rule, the glitch at I1 can propagate to one input of CE2 and one input of CE6, the glitch at I2 can propagate to one input of CE3 and one input of CE7; however, all the other one or two inputs of all the other CEs are not affected by the SEDU. Since a CE can intercept a glitch though its one-input is affected, CE6 and CE7 intercept the glitches and the outputs of them, i.e. I6 and I7 are correct. Meanwhile, since I6 is fed back to one input of CE3, the output (I3) of CE3 is correct as well. On the other hand, since the output of CE8 and the output of CE4 are correct, I1 can restore back to the correct value through CE1, and finally I2 can restore back to the correct value through CE2. In summary, the latch can self-recover from the SEDU at <I1, I2>.

In the presence of an SEDU for <I1, I3> resulting in glitches, according to the above-mentioned CEs' feedback rule, the glitch at I1 can propagate to one input of CE2 and one input of CE6, the glitch at I3 can propagate to one input of CE4 and one input of CE8; however, all the other one or two inputs of all the other CEs are not affected by the SEDU. Since a CE can intercept a glitch though its one-input is affected, CE2 and CE4 intercept the glitches and the output of them, i.e. I6 and I8 are correct. Meanwhile, since the inputs of CE1 and CE3 are correct, I1 and I3 can self-recover from the glitches through CE1 and CE3, respectively. In summary, the latch can self-recover from the SEDU at <I1, I3>. Similarly, we can get the scenario in the presence of an SEDU for <I1, I4> or <I1, I5> resulting in glitches but the analysis flow is omitted.

As discussed above, the latch can be properly operated in transparent mode and can retain data in hold mode of operation. Besides, the latch can filter an SET pulse in transparent mode and can self-recover from any SEDU in hold mode, i.e., the latch is SEDU self-recoverable and SET pulse filterable.

B. Simulation Results

The DURTPF latch has been designed by means of 22nm CMOS technology library. The layout has been drawn by means of the Cadence platform (Virtuoso) and pertinent simulations for verification of SET pulse filterability and

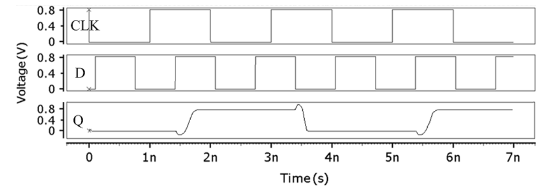

Fig. 5. Simulation results for DURTPF considering error free case.

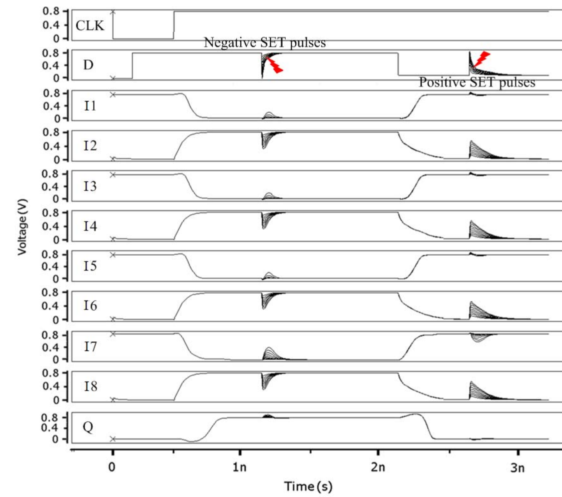

Fig. 6. Simulation results for DURTPF considering negative and positive SET pulses in transparent mode of operation.

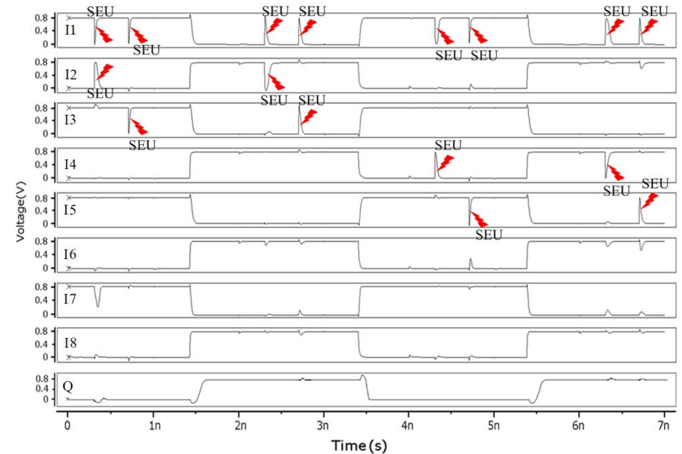

Fig. 7. Simulation results for DURTPF considering SEDUs at key node pairs <I1, I2>, <I1, I3>, <I1, I4> and <I1, I5>.

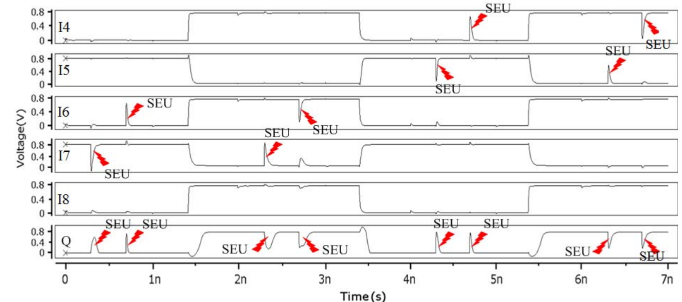

Fig. 8. Simulation results for DURTPF considering SEDUs at key node pairs <I7, Q>, <I6, Q>, <I5, Q> and <I4, Q>.

SEDU self-recoverability using HSPICE tool were performed. The supply voltage Vdd was set to 0.8V.

The transistor sizes for the latch design are listed in the following. (a) As regards the normal CEs, the PMOS transistor had W/L = 130/22 nm, the NMOS transistor had W/L = 40/22 nm; (b) as regards the CG based CEs, the PMOS transistor had W/L = 130/22 nm, the NMOS transistor had W/L = 80/22 nm; c) as regards the Schmitt trigger, the PMOS transistor had W/L = 120/44 nm, the NMOS transistor had W/L = 120/44 nm.

To verify the normal operation for our proposed DURTPF latch design, the simulation for DURTPF considering error free case has been firstly performed as presented in Fig. 5. According to the simulation results, the operation of the latch in transparent and hold mode of operation is the same as that of a traditional D-latch.

To verify the SET pulse filterability for our proposed DURTPF latch design, Fig. 6 shows the simulation results for DURTPF considering a series of negative and positive SET pulses in transparent mode of operation. Note that, the pulses are simulated by SWEEP statement using HSPICE. As we can see in Fig. 6, some pulses can propagate to the inputs and/or output of some CEs; however, no matter for which injection on correct value low or high of D, all of the injected pulses result in nearly no any effect on Q, i.e. these pulses are masked by the latch. In summary, the latch is SET pulse filterable.

To verify SEDU self-recoverability for our proposed DURTPF latch design, Fig. 7 shows the simulation results for DURTPF considering SEDUs at key node pairs <I1, I2>, <I1, I3>, <I1, I4> and <I1, I5>. Note that, since the CLK and D signals are the same as those in Fig. 5, they are omitted in Fig.7. As presented in Fig. 7, at 0.3, 0.7, 2.3, 2.7, 4.3, 4.7, 6.3 and 6.7 ns, an SEDU is respectively injected at node pairs <I1, I2>, <I1, I3>, <I1, I2>, <I1, I3>, <I1, I4>, <I1, I5>, <I1, I4> and <I1, I5>, but the node pairs can restore back to the correct data. In summary, all key node pairs can self-recover from an SEDU no matter the correct value is high or low, i.e. the latch is SEDU self-recoverable for all key node pairs.

On the other hand, as regards a node pair including the output of the latch and one of the 8 internal nodes I1 to I8, Fig. 8 has presented the simulation results for DURTPF considering key node pairs <I7, Q>, <I6, Q>, <I5, Q> and <I4, Q>. Similarly, the CLK and D signals are omitted and at 0.3, 0.7, 2.3, 2.7, 4.3, 4.7, 6.3 and 6.7 ns, an SEDU is respectively injected at node pairs <I7, Q>, <I6, Q>, <I7, Q>, <I6, Q>, <I5, Q>, <I4, Q>, <I5, Q> and <I4, Q>, but the node pairs can also restore back to the correct data. In summary, all key node pairs can self-recover from an SEDU no matter the correct value is high or low, i.e. the latch is SEDU self-recoverable for all node pairs.

As has been discussed above, the simulation results have demonstrated the SET pulse filterability as well as SEDU self-recoverability for the DURTPF latch. In the simulations, we have used a controllable double-exponential current source model to perform the SET and SEDU injections as well [25] to simulate alpha particle-striking. The worst case injected charge has been chosen to be up to 75fC, which is large enough to validate circuit operations. The time constant of the rise and fall of the current pulse was set to 0.1 and 3 ps, respectively.

IV. Latch Comparison and Evaluation

To quantitatively make a fair comparison, the reviewed latch designs in Section II have been designed in the same technology as well. Detailed comparison results among the latch designs including ours have been presented in Table I, with respect to the average of dynamic plus static power dissipation, D to Q transmission delay i.e. the average of rise and fall delays of D to Q, silicon area, power-delay-width product (PDWP), filterable SET pulse width and SET pulse filtering ability (SPFA), respectively. The PDWP and SPFA calculation formulas are given as below.

$$\text{PDWP} = \text{Power} \times (\text{Delay} - \text{Width}) \quad (1)$$

$$\text{SPFA} = \text{Width} / \text{Delay} \times 100\% \quad (2)$$

In the formulas, Power is the average of dynamic plus static power dissipation, Delay is D to Q transmission delay and Width is filterable SET pulse width whose value is not available for SET-not-filterable latch designs. As we can see, among the same type latch designs (e.g. SET pulse filterable ones), a smaller PDWP or a larger SPFA is better.

From Table I we can see that, in order to ensure SEDU self-recoverability and SET pulse filterability, we have used larger silicon area. Nevertheless, compared with the either SEDU self-recoverable (5th to 7th) or SET pulse filterable (8th to 10th) latch designs, ours has the smallest power dissipation due to low power design using CG technology. On the other hand, compared with the SET pulse filterable latch designs, delay of ours is not very smaller, but the comprehensive PDWP of ours is the smallest. Besides, SPFA of the DET-SEHP latch is larger due to the usage of two-stage SET pulse filtering operation, but SPFA of ours is comparable to the latch.

To make a further detailed quantitative comparison, the relative overheads in terms of power (ΔPower), delay (ΔDelay), area (ΔArea) and PDWP (ΔPDWP) among the reviewed latch designs compared with ours have been listed in Table II/III, and the calculation formula is given as below.

$$\Delta = (\text{Compared} - \text{Proposed}) / \text{Compared} \times 100\% \quad (3)$$

From Table II we can see that, compared with the SEDU

TABLE I
Comparison Results For Alternative SEU/SEDU/SET Hardened Latch Designs

Latch Name	Overheads			SET (ps)	PDWP	SPFA (%)
	Power (μW)	Delay (ps)	Area (μm^2)			
TMR [13]	1.43	40.92	7.02	-	58.52	-
RFC [17]	0.44	3.09	4.95	-	1.36	-
CLCT [24]	0.98	29.2	5.13	-	28.62	-
DNCS [25]	2.38	65.53	8.83	-	155.96	-
NTHLTCH [26]	2.27	13.19	10.07	-	29.94	-
DONUT [27]	2.30	19.34	7.98	-	44.48	-
DeltaDICE [28]	2.21	16.35	8.05	-	36.13	-
DET-SEHP [14]	1.78	156.5	6.89	110.9	55.89	70.9
LCHR [15]	1.12	127.0	8.97	89.2	42.34	70.2
FERST-EV [16]	2.60	128.1	6.23	91.4	95.42	71.4
DURTPF (Proposed)	1.02	131.4	10.30	95.2	36.92	72.5

TABLE II
RELATIVE OVERHEADS OF SEDU SELF-RECOVERABLE LATCH DESIGNS COMPARED WITH OURS

Latch Name	ΔPower (%)	ΔDelay (%)	ΔArea (%)	ΔPDWP (%)
NTHLTCH [26]	55.07	-	-2.28	-23.32
DONUT [27]	55.65	-	-29.07	16.99
DeltaDICE [28]	53.85	-	-27.95	-2.19
Average (Savings of ours)	54.85	-	-19.77	-2.84

TABLE III
RELATIVE OVERHEADS OF SET PULSE FILTERABLE LATCH DESIGNS COMPARED WITH OURS

Latch Name	ΔPower (%)	ΔDelay (%)	ΔArea (%)	ΔPDWP (%)
DET-SEHP [14]	42.70	16.04	-49.49	33.94
LCHR [15]	8.93	-3.46	-14.83	12.79
FERST-EV [16]	60.77	-2.58	-65.33	61.31
Average (Savings of ours)	37.46	3.33	-43.22	36.01

self-recoverable latch designs, to perform both SEDU and SET hardening, our latch design saves about 54.85% power dissipation due to the usage of clock gating transistors at the cost of 19.77% silicon area plus 2.84% PDWP on average. However, these compared latches are not SET filterable at all. Note that the ΔDelay is not suitable for comparison since the latch designs and ours are not the same type (SET pulse filterable ones, but Table III presents this type). From Table III we can see that, compared with the SET pulse filterable latch designs, all the average data of ours are better except for ΔArea since we have achieved both SEDU self-recoverability and SET filterability at the cost of silicon area for the latch. The increase in silicon area may make the latch vulnerable to soft errors; however, the latch can self-recover from the SEU/SEDUs and can also filter the SET pulse. In summary, we have used redundant area to achieve higher reliability.

V. CONCLUSIONS

Technology scaling results in that soft errors like SEDU and SET pulse are becoming serious. Most of existing latch designs are not SEDU and SET simultaneously hardened or perform with larger overheads like power dissipation. Facing this, we present an SEDU self-recoverable and SET pulse filterable latch design with reasonable overheads. Simulations have demonstrated the SEDU self-recoverability and SET pulse filterability at the cost of silicon area.

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