Package and Chip Accelerated Aging Methods for Power MOSFET Reliability Evaluation

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***Abstract*—This paper investigates power MOSFET stress strategies for both package and chip aging evaluation. Two stress test methods are developed to speed up packaging and chip aging process respectively. As a result, the characteristics shifts of package and chip aging can be plotted independently. Thus, the measurement accuracy and measurement time can be improved. A test chip is designed and fabricated in a 0.15μm BCD process. The measured results demonstrate a 10kμm power MOSFET has R_{on} increased by 72% after 6.3hr stress for the package aging. For the chip aging, the MOSFET has R_{on} increased by 12% after 600 times stress pulses. The measurement verifies that the accelerated aging in the package and the chip can be controlled separately.**

Keywords—accelerated aging, accelerated testing, power MOSFET

I. INTRODUCTION

Monolithic power ICs are popular in small and medium power applications such as power modules for LED lighting and portable devices [1]–[3]. They integrate both HV (High Voltage) switching MOSFETs and LV (Low Voltage) control circuits in one chip not only for reducing the circuit footprint but also for decreasing the IC package cost. Both the static power dissipation and the power efficiency can be improved by the integration. However, the integrated power MOSFET design has many reliability risk in the power uniformity and the temperature distribution [4]. They may drive the early failure and accelerated aging. The prediction of intrinsic oxide lifetime as a function of the electric field can be calculated from a unified model [5]. It can be uniquely decided at any given temperature and the oxide field as shown in Fig. 1. In particular, the temperature acceleration is widely used for the product reliability analysis such as *High Temperature Operating Life* (HTOL) test.

Fig.2 shows the bathtub curve that depicts the lifelong reliability for semiconductor devices. It can be roughly divided into three periods, infancy, operational, and wear-out periods. It is important to learn the length of each period such that the devices can serve their best purposes. There are acceleration tools to speed up the characteristic processes, such as burn-in test [6]. However, it remains time consuming and costly. Furthermore, it usually gives lumped results which are difficult to find the cause-effect relationship.

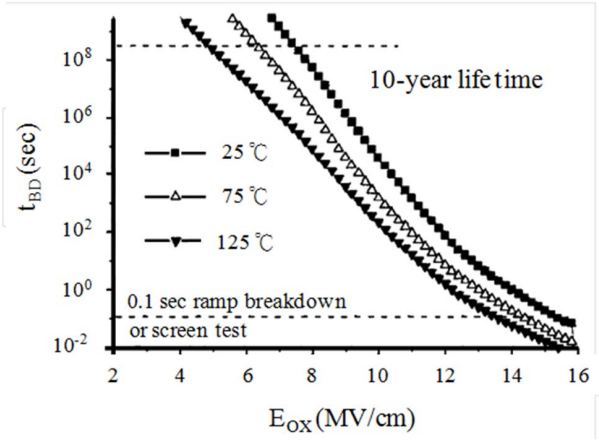


Figure 1. Lifetime is decided at any given temperature and oxide field. (Source: [5])

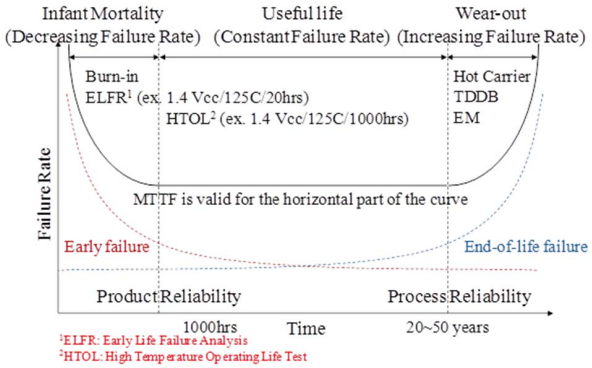


Figure 2. The bathtub curve in semiconductor reliability. (Source: [6])

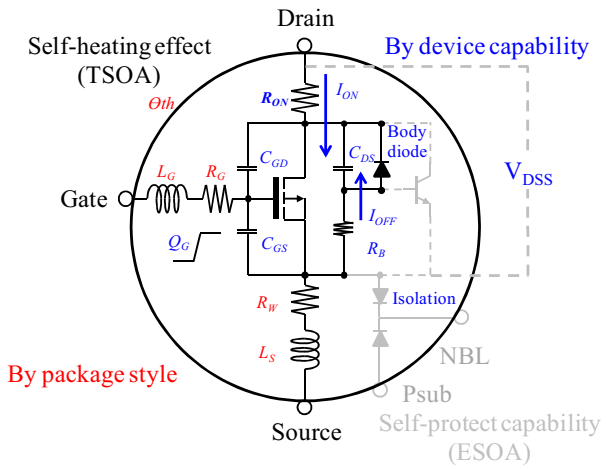


Figure 3. Equivalent circuit and key parameters of a power MOSFET.

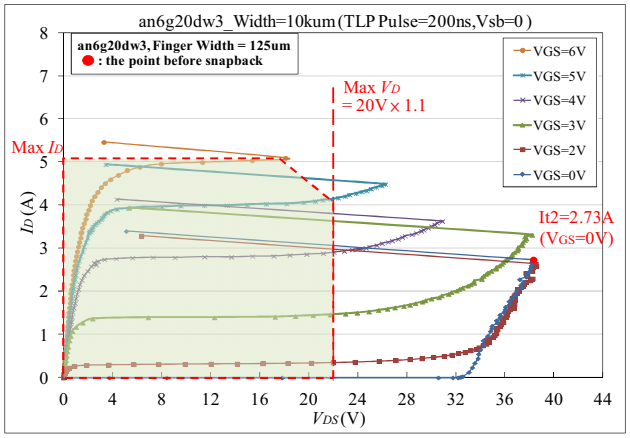


Figure 4. E-SOA definition.

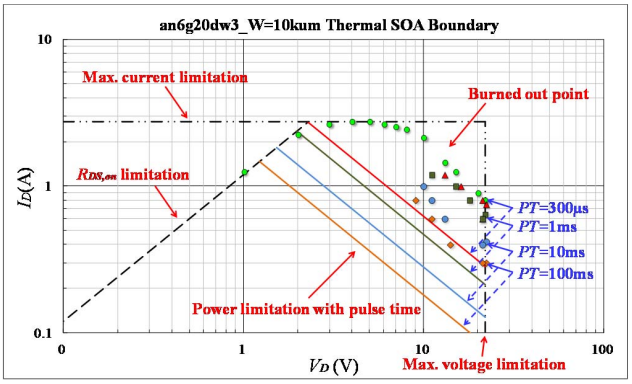


Figure 5. Thermal SOA definition.

According to the Military Handbook (MIL-HDBK-217F) and the reliability standard (MIL-STD), the lifetime is reduced to half for every increase of 10°C in the junction temperature. Therefore, many test tools increase environment temperature to shorter test time. The acceleration process is called burn-in test. In semiconductor, lifetime prediction method is to accelerate aging in small size or single finger device by high electric field and high temperature [5]. In addition, some measurement items are widely used to find the limiting boundary in a switch operation. It includes *Thermal Safe Operating Area* (T-SOA), *Unclamped Inductive Switching* (UIS), reverse recovery time, switch time, and gate charge tests. However, they cannot summaries any prediction for the life time in power MOSFET. Two stress test methods are developed to speed up packaging and chip aging process respectively. As a result, the characteristics shifts of package and chip aging can be plotted independently. Thus, the measurement accuracy and measurement time can be improved.

The rest of this paper is organized as follows. Section II describes the T-SOA and proposes a measurement methodology. Section III presents and analyzes the measured data on a 0.15µm 1P3M test chip to verify the proposed methodology. Finally, conclusions are drawn in section IV.

II. T-SOA TESTING FOR POWER MOSFET

A. Power MOSFET

The equivalent circuit model of a power MOSFET is described in Fig. 3. There has showed the turn-on resistance R_{ON} and the bond wire resistance R_W. In a *Laterally Diffused MOSFET* (LDMOS), the turn-on resistance R_{ON} is made by

$$R_{ON} = R_{ch} + R_{drift} + R_{metal} \quad (1)$$

Here, R_{ch} is the channel resistance in linear mode operation, R_{drift} is the drift region resistance, R_{metal} is the internal metal routing resistance. In this paper, a 20V N-type power MOSFET is designed with the total width of 10kµm and the package by SOP-8 (Small Outline Package- 8 pins).

The term of *Safe Operating Area* (SOA) is used to describe the region in the I_D-V_{DS} plane without suffering damage in the switching device. The boundary of the SOA is under the control of the device designer. At the snapback point, the trigger current I_{t2} is the current that destructs the parasitic n-p-n transistor in nanoseconds. This SOA is also called *electrical-SOA* (E-SOA) which only focuses on the electrical characterization of the MOSFET and the electrical effect of the parasitical bipolar transistor. There is no self-heating effect under consideration. Therefore, an ultra short pulse is often used for the E-SOA testing. The E-SOA region is defined by the I-V curve in Fig. 4. They are usually measured by 100ns to 200ns pulses in the *Transmission Line Pulse* (TLP) measurement [7]–[8]. However, the SOA determinations for the actual applications are not a simple matter. This is because both the thermal and the electrical effects enter into the boundary. The T-SOA plays an important role to the actual applications.

B. T-SOA in power MOSFET

These thermal related measurements are frequently destructive with complicated comparison between theory and experiment. Thermal characterization is focused on the power system design. The high temperature will shorten the device's lifetime or even destroy the device. The suggested highest operating temperature is around 150°C. As depicted in Fig. 5, T-SOA boundaries are used to limit for the operating conditions in the maximal operating drain voltage, the maximal drain current, and the maximum power. They have different

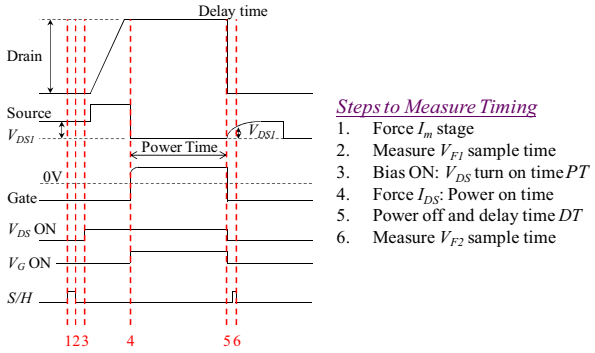


Figure 6. Measurement timing diagram.

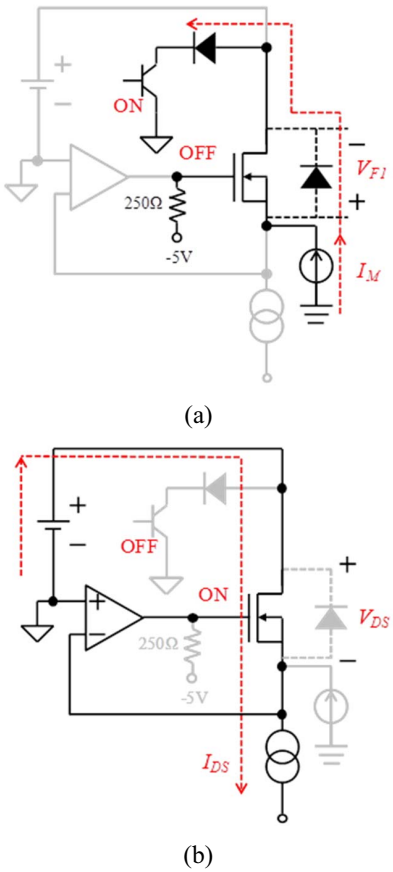


Figure 7. T-SOA measurement schemes of (a) sense step and (b) stress step.

limitations under the operation frequency. The limitation of the turn-on resistance is defined by the total R_{ON}. It determines how much current the device can carry in the on-state situation. The maximum allowable current can be considered as the current limit. The bond wire fusing is also one of the limiting factors. The device like a bond wire or contact region can be locally heated to be destructed. The voltage is limited by the breakdown voltage of the diffusion layer. The avalanche breakdown can lead to the loss of electrical control or the direct physical alteration of the device's structure. Maximum allowable power is caused by normal switching mode operation and the heat dissipation. The active part of the device becomes very hot that it is said to be physically or chemically altered. They make the T-SOA being defined for the long term operation considerations. The part of the solid line is the actual usable range under lifetime consideration.

C. T-SOA measurement

T-SOA is defined as the limiting condition for the operating voltage and current of the device. It is expected to operate the device without self-damage. To find the maximum allowable current for a device at a given voltage across the terminals of the MOSFET is shown in Fig. 5. It may trigger the parasitic n-p-n transistor to destruct the device due to thermal runaway event with a medium time pulses (time scale order in µs-ms). Other event drives damage with the high temperature such as the short circuit condition. For power MOSFET, the T-SOA test procedure is suitable to evaluate the power MOSFETs as shown in Fig. 6. In Fig. 7(a), the measurement of sense step is forcing the measured current I_M to obtain the forward voltage V_{F1} in the body diode. In the stress step, it is to force a power with fixed V_{DS} and I_{DS} during a power pulse time PT *as* shown in Fig. 7(b). After the power pulse with delay time DT, the sensing step is measured again to obtain the changed value of the forward voltage V_{F2}. They are used to calculate the raised temperature ΔT.

$$\Delta V_F = V_{F1} - V_{F2} \tag{2}$$

$$\Delta T = \Delta V_F / K \tag{3}$$

Where K is a coefficient of the forward diode voltage changed with the temperature. It is helpful to characterize the design reference or evaluates the thermal runaway performance in the layout, the package, and the backend assembly structures.

The body diode of the power MOSFET has been used to detect the channel temperature. The yielded voltage has a negative temperature coefficient due to I_M in the forward bias condition. At the lower I_M, K-factor will be large due to the temperature leakage issue. For measurement accuracy, it suggests to choose the small K-factor (large body current) to calibrate the junction temperature (Tj).

Accordingly, we fix all related parameters like pulse time, delay time, K-factor, and V_G of DUT and then, calculate the maximum current (I_{DS}) for different voltage (V_{DS}). DT is needed due to the oscillation resulting from the capacitance in the circuit and the device. To find out ΔT without any thermal sink effect, we vary the DT as 50µs, 100µs, and 300µs for different the rising temperature at 1µs.

$$\Delta T_{DT=t} = a \times \ln(DT) + \Delta T_{DT=1\mu s} \tag{4}$$

Hence, the thermal resistance θ_{th} (°C/W) is driven by

$$\theta_{th} = \Delta T_{DT=1\mu s} / (V_{DS} \times I_{DS}) \tag{5}$$

Within the safe operating range, the life time of the semiconductor device is strongly affected by the temperature fluctuations due to the loading. Every change in temperature causes mechanical stress in the device, which affects the solder and the bond connections. As per the observation, the effective

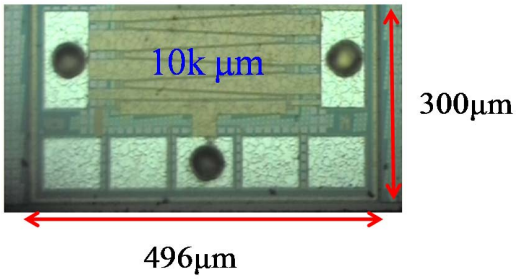


Figure 8. Die photo.

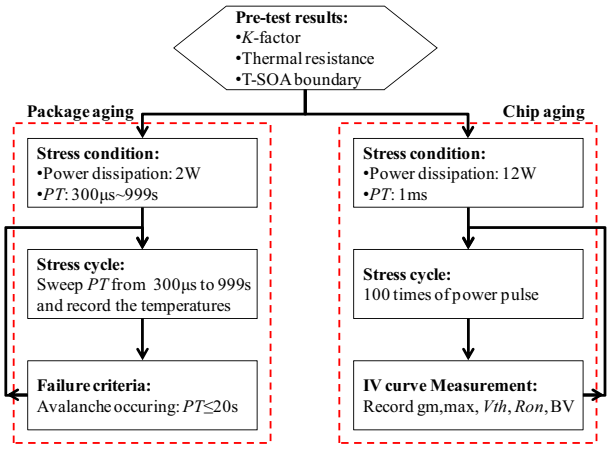


Figure 9. Flow chart for package aging and chip aging methods.

thermal resistance is influenced by many factors not just the die size and the power dissipation. It is also influenced by the layout, the metal area, and the heating or cooling from adjacent devices.

III. Implementation and Measurements for Power MOSFET Aging Test

A test chip has been designed and fabricated in 0.15µm 1P3M BCD process. The 20V LDMOS is used to build the large array power MOSFET devices. Fig. 8 shows the photograph of the test chip. The power MOSFET layout area size including the bond pads is 496µm×300µm. For measuring the T-SOA characterization, it is packaged by SOP-8. As shown in Fig. 7, the DUT (Device Under Test) of MOSFET is controlled to force a power stress pulse. After some delay time in micro-second level, we inject a biasing current to measure the forward voltage in the body diode to obtain the operating channel temperature. Fig.9 shows the proposed aging test flow. It is included the accelerating methods for the package aging and the chip aging. Before the test, the T-SOA and thermal model have to be obtained for defining the test criteria.

Fig. 10 shows the measured data of the forward diode voltage versus temperature under I_M = 10mA. To measure the temperature coefficient of the body diode, wafer chamber is used to control the temperatures. In this measurement, the *K*-factor is 1.53mV/°C for 10kµm MOSFET. The channel temperature of the power MOSFET can be estimated with obtained *K*-factors.

Fig. 11 shows the avalanched lines and final burned out

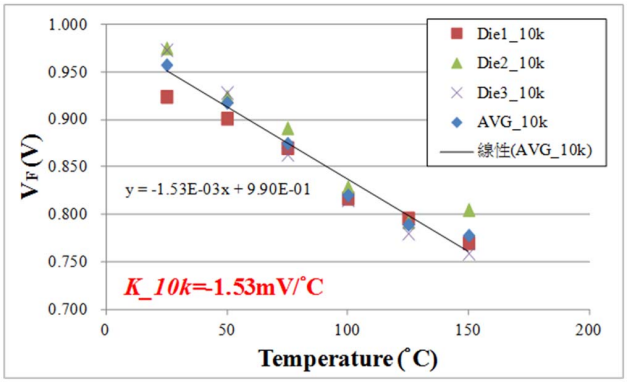


Figure 10. Forward IV curve of 20V power MOSFETs with the total width equal to 10kµm.

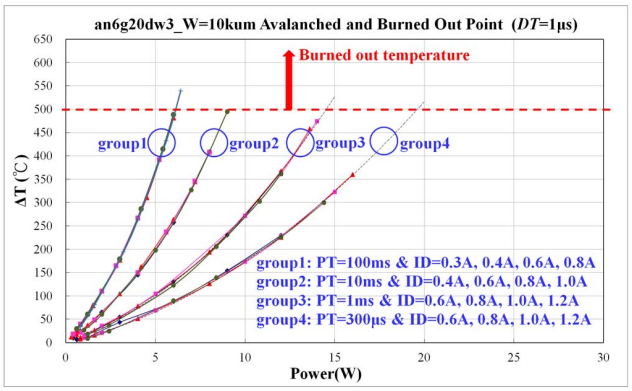


Figure 11. Temperature increasing at these avalanched and burned out points versus power dissipation in pulse time of 300µs, 1ms, 10ms and 100ms.

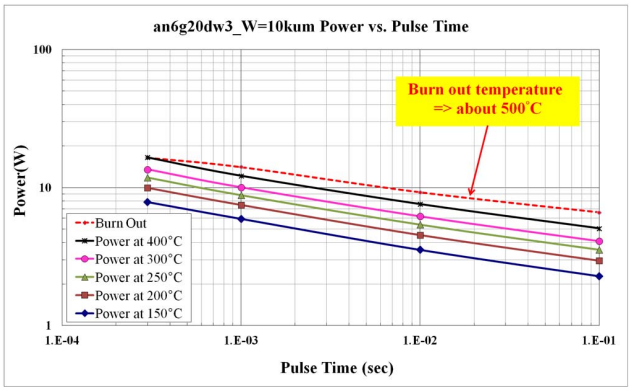


Figure 12. Power dissipation boundary versus pulse time under limited channel temperature.

area at different power dissipation and the pulse time. It shows the temperature rising at each point. All of burned out temperatures are above 500°C. These temperatures are estimated after 1us delay time to the power pulse. Therefore, it can be used to limit the stress temperature for our aging test experiment.

Fig. 12 shows the power needed for a single power pulse time *PT* to rise the channel temperature to the limit target. For 150°C operation limited in the circuit design, the channel of

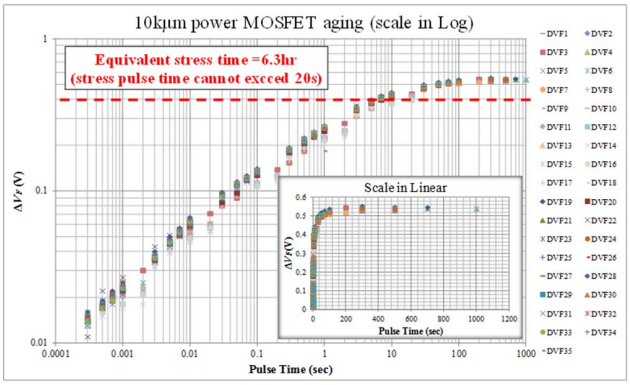


Figure 13. Forward voltage versus pulse time stress for 10kμm power MOSFET.

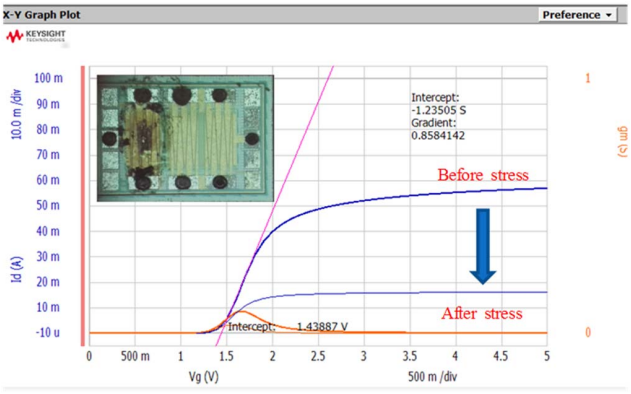
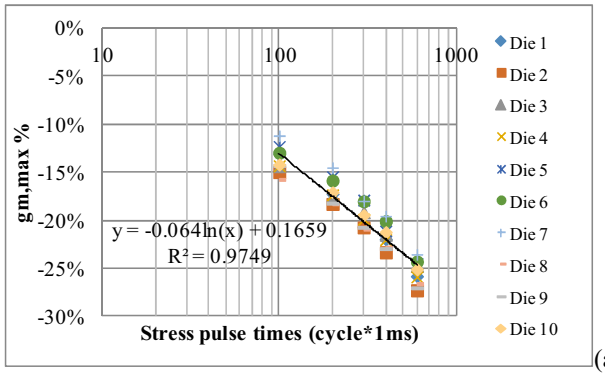


Figure 14. I_D-V_G curve for 10kμm MOSFET before and after stress.

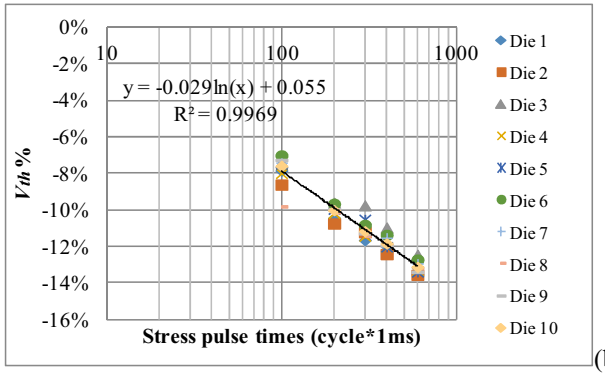
10kμm power MOSFET can rise the power dissipation by 6W under 1ms pulse. For those larger designs with lower turn-on resistance, the power dissipation is reduced. The lifetime getting extended when the rise of junction temperature is small. Finally, the T-SOA boundary can be drawn as those in Fig. 5.

According to the previous result, we select 2W power dissipation as the stress condition. In this case, the results of V_{F1} and V_{F2} are measured in 50μs power pulse. Then, it waits until the channel temperature back to the room temperature. When ΔV_F is less than 5mV, the pulse time is sequentially changed from 300μs to 999s step by step. That is repeated until the stress pulse time cannot exceed 20 seconds. Here, the components have the voltage avalanche phenomenon, but no damaged.

Fig. 13 shows the stress results. It shows the correlation between the pulse time and the forward voltage. When the stress pulse time over 20 seconds, the values of ΔV_F are almost unchanged. It means the whole chip's body temperature achieved heat saturation. This saturation temperature is related to the heat sink performance such as the materials of metal, package, PCB…etc. Based on Eq. (3), the saturation temperature can be derived approximately 350°C for 10kμm power MOSFET. Fig. 14 shows the measurement I-V curve for 10kμm MOSFET before and after IC stresses. After the avalanche condition happened, the $I_{D,sat}$ has degraded approximately 67% and 72% R_{ON} increasing after the 6.3hr stress time. From the failure analyses, the die photo shows the



(a)



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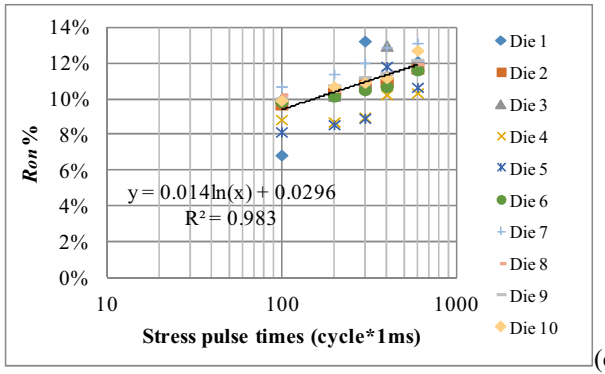

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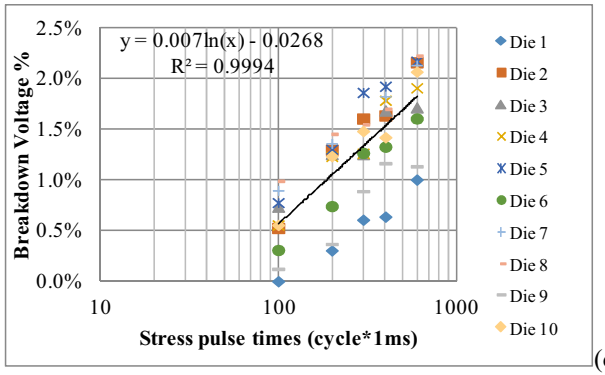

(d)

Figure 15. Degradation results of (a)gm,max, (b) Vth, (c) Ron, and (d) breakdown voltage versus stress pulse times for 10kμm MOSFET. (1 cycle stress condition: PT=1ms, V_{DS}=24V, I_D=0.5A).

colloidal melting that affects the bounding PADs and drives a high resistance. But it has a similar I-V curve as that before

stresses after we removed the IC package and then, probed the chip. It is verified that the aging in the package and bonding wire interface is more obvious than that in the chip.

In the chip aging measurements, we select 1ms pulse time with 12W power dissipation as one kind of stress cycle which causes the junction temperature rise to over 300°C. That will not increase the case and the substrate temperature because of the thermal conduction effect. It is needed to have enough time to transfer heat to the substrate and the package case. After the stress pulse, it is used for a period to sink the junction temperature to the room temperature. In this case, the measured time is approximately one second in one stress cycle. Hence, we measure the I-V curve after each 100-stress cycle to obtain the characteristics of the 10kμm power MOSFET for tracing the chip degradation. The degradation results are shown in Fig. 15.

Accordingly, the total stress time only at 600ms (600 cycles of power stress) can drive the degradation of the gm,max to change at -25% as shown in Fig. 15(a). In Fig. 15(b), the V_{th} has changed about -13% after the stress. Fig. 15(c) and (d) show the R_{on} with 12% degradation and the breakdown voltage with 1.8% shift. They are stressed by the pulse time of 1ms, drain voltage of 24 volt, and drain current of 0.5A in a cycle pulse. Based on the above experiments, we can trace the lifetime behavior by changing different power dissipation of the stress pulse as soon as possible.

IV. Conclusions

This paper has successfully explored the accelerated aging methods for the power chip. The proposed stress conditions for both the package aging and the chip aging can reduce the measurement time of obtaining the power MOSFET aging characterizations. According to the results, it is clearly to understand the junction temperature related to the power pulse time, the chip size and the heat sink of the devices. The proposed methods use different pulse time and power dissipation to control the channel temperature operating under adding the device temperature or not. A test chip is designed and fabricated in 0.15μm 1P3M BCD process. The measured results demonstrate the 10kμm power MOSFET degradation with 72% R_{ON} increasing after the 6.3hr stress time under the package aging test. In the chip aging, the measured results showed the MOSFET by increasing 12% R_{ON} after 600 times stress. The measurement verified that the accelerated aging in package or chip can be controlled separately.

We suggest that you use a text box to insert a graphic (which is ideally a 300 dpi TIFF or EPS file, with all fonts embedded) because, in an MSW document, this method is somewhat more stable than directly inserting a picture.

To have non-visible rules on your frame, use the MSWord "Format" pull-down menu, select Text Box > Colors and Lines to choose No Fill and No Line.

Acknowledgment

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