University Booth at DATE 2019

The University Booth is organised during DATE and will be located in the exhibition area. All demonstrations will take place from Tuesday, March 26 to Thursday, March 28, 2019 during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.
The University Booth programme is composed of 32 demonstrations from 10 different countries, presenting software and hardware solutions. The programme is organised in 9 sessions of 2 or 2.5 h duration and will cover the topics:

- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Heterogeneous Computing: Embedded meets Hyperscale and HPC
- Model-Based Design of Intelligent Systems

The University Booth at DATE 2019 invites you to find out more about the latest trends in software and hardware from the international research community.
Most demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.
We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.
More information is available online at https://www.date-conference.com/exhibition/u-booth. The University Booth programme is included in the conference booklet and available online at https://www.date-conference.com/exhibition/ub-programme. The following demonstrators will be presented at the University Booth.

A FAST PROTOTYPING FRAMEWORK FOR SERVICE-ORIENTED AUTOMOTIVE APPLICATIONS

Authors:
Matthias Becker, Zhonghai Lu and De-Jiu Chen, KTH Royal Institute of Technology, SE

Timeslots:
- UB02.3 (Tuesday, March 26, 2019 12:30 - 15:00)
- UB03.3 (Tuesday, March 26, 2019 15:00 - 17:30)
- UB07.3 (Wednesday, March 27, 2019 14:00 - 16:00)

***Abstract**: Service-Oriented Architectures (SOA) provide a flexible platform for advanced automotive software applications. We present a research platform for fast prototyping of platform software and applications. The hardware is built around a RC car. Several sensors and actuators are connected over microcontrollers that can be accessed from higher-level ECUs over bus connections. User applications are executed on 4 Linux-based ECUs which communicate over a multi-hop Ethernet network. All communication of applications is realized over SOME-IP, an automotive middleware layer that is based on the SOA principle. The development framework generates code skeletons for user tasks, and all required management and configuration code of the underlying SOA framework, based on a user specified application model. It is then automatically transferred and compiled on the respective ECUs. We show the usability of the platform by a remote-operation scenario.*

A MODULAR RECONFIGURABLE DIGITAL MICROFLUIDICS PLATFORM

Authors:
Georgi Tanev[1], Winnie Svendsen[2] and Jan Madsen[3]
[1]Technical University of Denmark, DK; [2]DTU Bioengineering, DK; [3]DTU Compute, DK

Timeslots:
- UB02.10 (Tuesday, March 26, 2019 12:30 - 15:00)
- UB08.8 (Wednesday, March 27, 2019 16:00 - 18:00)
- UB10.4 (Thursday, March 28, 2019 12:00 - 14:30)

***Abstract**: Digital microfluidics is a lab-on-a-chip (LOC) technology that allows for manipulation of a small amount of liquids on a chip-scaled device patterned with individually addressable electrodes. Microliter sized droplets can be programmatically dispensed, moved, mixed, react, split and stored thus implementing sample preparation protocols. Combining digital microfluidics with miniaturized analytical methods allows biomedical lab assays to be implemented on a LOC device that provides full sample-to-answer functionality. The growing complexity and integration of the LOC devices impose the need of software tools and hardware instruments to design, simulate, program and operate the broad range of LOC instrumentation needs. To address this matter, we present a modular reconfigurable microfluidics instrumentation platform (shown in Figure 1) capable of evolving to match the instrumentation needs of a specific LOC. The prototype shown in Figure 2 serves the purpose to demonstrate the platform.*

A RISC-V BASED VIRTUAL PROTOTYPE WITH AN INTEGRATED HARDWARE-IN-THE-LOOP RADAR

Authors:
Peer Adelt, Denis Zeinel, Bastian Koppelmann, Wolfgang Mueller and Christoph Scheytt, University of Paderborn, DE

Timeslots:
- UB06.6 (Wednesday, March 27, 2019 12:00 - 14:00)

***Abstract**: Our demonstration shows a small radar sensor in interactive communication with a RISC-V processor board and a RISC-V Virtual Prototype (VP) where the VP and the processor concurrently execute exactly the same target compiled software without a visible difference in reaction time. This demonstrates that widely available open source based virtual prototyping environments provide an adequate, stable, and efficient framework for the analysis of such embedded applications. The demonstration integrates our in-house developed 120GHz radar sensor via CAN bus with the SiFive RISC-V HiFive1 development board and our QEMU based VP. For the HiFive1 integration, we developed an Ardunio compliant board with an SPI-CAN adapter and a display. For the VP integration, we implemented the same components as QEMU QOM hardware models. Though the VP is executed in a linux based VirtualBox virtual machine on top of an additional host operating system, the impact of both is not visible in this setup.*

ACSIM: A NOVEL, SIMULATOR FOR HETEROGENEOUS PARALLEL AND DISTRIBUTED SYSTEMS THAT INCORPORATE CUSTOM HARDWARE ACCELERATORS

Authors:
Nikolaos Tampouratzis[1] and Ioannis Papaefstathiou[2]
[1]Technical University of Crete, GR; [2]Synelixis Solutions LTD, GR

Timeslots:
- UB01.5 (Tuesday, March 26, 2019 10:30 - 12:30)
- UB02.5 (Tuesday, March 26, 2019 12:30 - 15:00)

***Abstract**: The growing use of hardware accelerators in both embedded (e.g. automotive) and high-end systems (e.g. Clouds) triggers an urgent demand for simulation frameworks that can simulate in an integrated manner all the components (i.e. CPUs, Memories, Networks, Hardware Accelerators) of a system-under-design (SuD). By utilizing such a simulator, software design can proceed in parallel with hardware development which results in the reduction of the so important time-to-market. The main problem, however, is that currently there is a shortage of such simulation frameworks; most simulators used for modelling the user applications (i.e. full-system CPU/Mem/Peripherals) lack any type of support for tailor-made hardware accelerators. ACSIM framework is the first known open-source, high-performance simulator that can handle holistically system-of-systems including processors, peripherals, accelerators and networks. The complete ACSIM framework together with its sophisticated GUI will be presented.*

ADDRESSING MEAN-IN-THE-MIDDLE THREAT IN EXTENSIVELY CONNECTED CARS AND NEXT-GENERATION AUTOMOTIVE NETWORKS

Authors:
Luca Crocetti and Luca Baldanzi, University of Pisa, IT

Timeslots:
- UB07.5 (Wednesday, March 27, 2019 14:00 - 16:00)

***Abstract**: Today's trend in the automotive industry is to integrate more and more interconnected electronics systems in order to offer functionalities and services orientated to the autonomous driving, also by adoption of wireless communication links such as Wi-Fi 802.11p. Thus a connected car results to act as a node of many and heterogeneous networks and thus being exposed to the typical threats of the IT field. The proposed demo aims to investigate the security vulnerabilities of a hypothetical real application scenario exploiting the wireless links and to target the related cybersecurity mechanisms required to counteract possible attacks. The demo consists of two FPGA boards that act as nodes of a 802.11p based network, one as the car and one as an infrastructure unit, and a laptop that acts as malicious entity and performs a Man-In-The-Middle attack. The emulated malicious node alters the communication between the two FPGA nodes and expose the car-like FPGA node to threats as car stealing.*

APODOSIS: ADVANCED ORCHESTRATOR FOR SMART-BUILDINGS

Authors:
Kostas Siozios[1] and Stylianos Siskos[2]
[1]Aristotle University of Thessaloniki, GR; [2]Department of Physics, Aristotle University of Thessaloniki, GR

Timeslots:
- UB02.9 (Tuesday, March 26, 2019 12:30 - 15:00)
- UB10.5 (Thursday, March 28, 2019 12:00 - 14:30)

***Abstract**: This work presents a distributed system for supporting advanced orchestrator of a smart grid environment. By efficiently control energy production from renewable sources and the energy loads, it is feasible to minimize the energy cost. In contrast to similar approaches, the proposed decision-making is performed in a distributed manner, while it also exhibits limited computational complexity.*

ASAM: AUTOMATIC SYNTHESIS OF ALGORITHMS ON MULTI CHIP/FPGA WITH COMMUNICATION CONSTRAINTS

Authors:
Amir Masoud Gharehbaghi, Tomohiro Maruoka, Yukio Miyasaka, Akihiro Goda, Amir Masoud Gharehbaghi and Masahiro Fujita, The University of Tokyo, JP

Timeslots:
- UB03.4 (Tuesday, March 26, 2019 15:00 - 17:30)
- UB07.7 (Wednesday, March 27, 2019 14:00 - 16:00)
- UB09.3 (Thursday, March 28, 2019 10:00 - 12:00)

***Abstract**: Mapping of large systems/computations on multiple chips/multiple cores needs sophisticated compilation methods. In this demonstration, we present our compiler tools for multi-chip and multi-core systems that considers communication architecture and the related constraints for optimal mapping. Specifically, we demonstrate compilation methods for multi-chip connected with ring topology, and multi-core connected with mesh topology, assuming fine-grained reconfigurable cores, as well as generalization techniques for large problems size as convolutional neural networks. We will demonstrate our mappings methods starting from data-flow graphs (DFGs) and equations, specifically with applications to convolutional neural networks (CNNs) for convolution layers as well as fully connected layers.*

CS: CRAZYSQUARE

Authors:
Federica Caruso[1], Federica Caruso[1], Tania Di Mascio[1], Alessandro D'Errico[1], Marco Pennese[2], Luigi Pomante[1], Claudia Rinaldi[1] and Marco Santic[1]
[1]University of L'Aquila, IT; [2]Ministry of Education, IT

Timeslots:
- UB05.5 (Wednesday, March 27, 2019 10:00 - 12:00)
- UB09.5 (Thursday, March 28, 2019 10:00 - 12:00)

***Abstract**: CrazySquare (CS) is an adaptive learning system, developed as a serious game for music education, specifically indicated for young teenager approaching music for the first time. CS is based on recent educative directions which consist of using a more direct approach to sound instead of the musical notation alone. It has been inspired by a paper-based procedure that is currently used in an Italian middle school. CS represents a support for such teachers who prefer involving their students in a playful dimension of learning rhythmic notation and pitch, and, at the same time, teaching playing a musical instrument. To reach such goals in a cost-effective way, CS fully exploits all the recent advances in the EDA domain. In fact, it is based on a framework composed of mobile applications that will be integrated with augmented reality HW/SW tools to provide virtual/augmented musical instruments. The proposed demo will show the main features of the current CS framework implementation.*

DESIGN SPACE EXPLORATION FRAMEWORKS FOR APPROXIMATE COMPUTING

Authors:
Alberto Bosio[1], Olivier Sentieys[2] and Daniel Ménard[3]
[1]University of Lyon, FR; [2]University of Rennes, INRIA/IRISA, FR; [3]INSA Rennes - IETR, FR

Timeslots:
- UB01.7 (Tuesday, March 26, 2019 10:30 - 12:30)
- UB06.9 (Wednesday, March 27, 2019 12:00 - 14:00)
- UB09.10 (Thursday, March 28, 2019 10:00 - 12:00)

***Abstract**: Approximate Computing (AxC) investigates how to design energy efficient, faster, and less complex computing systems. Instead of performing exact computation and, consequently, requiring a high amount of resources, AxC aims to selectively relax the specifications, trading accuracy off for efficiency. The goal of this demonstrator, is to present a Design Space Exploration framework able to automatically explore the impact of different approximate operators on a given application accordingly to the required level of accuracy and the available HW architecture. The first demonstration relates to the word-length optimization of variables in a software or hardware system to explore cost (e.g., energy) and quality trade-off solution. The tool is scalable and targets both customized fixed-point and floating-point arithmetic. The second demonstration is about the use of other approximate techniques. The proposed demonstrator is linked with the DATE19 Monday tutorial M03.*

EDP PLAYER: A DESIGN ASSISTANT FOR PROCEDURAL DESIGN AUTOMATION OF ANALOG INTEGRATED CIRCUITS

Authors:
Matthias Schweikardt[1], Husni Habal[2] and Jürgen Scheible[1]
[1]Hochschule Reutlingen, DE; [2]Infineon Technologies, DE

Timeslots:
- UB06.2 (Wednesday, March 27, 2019 12:00 - 14:00)
- UB07.2 (Wednesday, March 27, 2019 14:00 - 16:00)

***Abstract**: In this demonstration, we address procedural circuit design automation of analog integrated circuits. Procedural automation means, that the knowledge-based strategy of human experts is captured in an executable script, which makes it reusable. We call this principle EDP (Expert Design Plan). An EDP can cover different performance parameters, technologies and topologies. We present the EDP Player, which enables the creation and execution of plain EDPs. The tool provides a preliminary version of an instruction set tailored to the typical manual analog circuit design flow, called EDPL (EDP-Language). The tool is fully integrated within Cadence Virtuoso based on Cadence SKILL. The tool has been utilized for three different examples: the automated design of a miller operational amplifier, a bandgap, and the automated creation of variants of a smart power IC. The usage of EDPs leads to a strong reduction of design time without loss of both design quality and reliability.*

EQ-PYD-NET: ENERGY-EFFICIENT MONOCULAR DEPTH ESTIMATION ON ARM-BASED EMBEDDED PLATFORMS

Authors:
Andrea Calimera[1], Valentino Peluso[1], Antonio Cipolletta[1], Matteo Poggi[2], Fabio Tosi[2] and Stefano Mattoccia[2]
[1]Politecnico di Torino, IT; [2]Università di Bologna, IT

Timeslots:
- UB02.4 (Tuesday, March 26, 2019 12:30 - 15:00)
- UB07.4 (Wednesday, March 27, 2019 14:00 - 16:00)
- UB08.4 (Wednesday, March 27, 2019 16:00 - 18:00)

***Abstract**: The demonstration intends to show the implementation of energy-efficient monocular depth estimation using a low-cost CPU for low-power embedded systems. Through the demo we're going to present the PyD-Net depth estimation network, which consists of a lightweight CNN designed for CPUs and able to approach state-of-the-art accuracy. Then we introduce an accuracy-driven complexity reduction strategy based on a hardware-friendly fixed-point quantization. The objective is (i) to demonstrate the portability of the Quantized PyD-Net model into a general-purpose RISC architecture of the ARM Cortex family, (ii) quantify the accuracy-energy tradeoff of unsupervised monocular estimation to establish its use in the embedded domain. During the live demonstration the QPyD-Net will be made running on a Raspberry PI board powered by a Broadcom BCM2837 chip-set.*

HEPSYCODE-MC: ELECTRONIC SYSTEM-LEVEL METHODOLOGY FOR HW/SW CO-DESIGN OF MIXED-CRITICALITY EMBEDDED SYSTEMS

Authors:
Luigi Pomante[1], Vittoriano Muttillo[1], Marco Santic[1] and Emilio Incerto[2]
[1]Università degli Studi dell'Aquila - DEWS, IT; [2]IMT Lucca, IT

Timeslots:
- UB05.4 (Wednesday, March 27, 2019 10:00 - 12:00)
- UB09.4 (Thursday, March 28, 2019 10:00 - 12:00)

***Abstract**: Heterogeneous parallel architectures have been recently exploited for a wide range of embedded application domains. Embedded systems based on such kind of architectures can include different processor cores, memories, dedicated ICs and a set of connections among them. Moreover, especially in automotive and aerospace application domains, they are even more subjected to mixed-criticality constraints. So, this demo addresses the problem of the ESL HW/SW co-design of mixed-criticality embedded systems that exploit hypervisor (HPV) technologies. In particular, it shows an enhanced CSP/SystemC-based design space exploration step, in the context of an existing HW/SW co-design flow that, given the system specification is able to (semi)automatically propose to the designer: - a custom heterogeneous parallel HPV-based architecture; - an HW/SW partitioning of the application; - a mapping of the partitioned entities onto the proposed architecture.*

HIPACC: SYNTHESIZING HIGH-PERFORMANCE IMAGE PROCESSING APPLICATIONS WITH HIPACC

Authors:
M. Akif Özkan[1], Oliver Reiche[1], Bo Qiao[1], Richard Membarth[2], Jürgen Teich[1] and Frank Hannig[1]
[1]Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE; [2]German Research Center for Artificial Intelligence (DFKI), DE

Timeslots:
- UB01.4 (Tuesday, March 26, 2019 10:30 - 12:30)

***Abstract**: Programming heterogeneous platforms to achieve high performance is laborious since writing efficient code requires tuning at a low level with architecture-specific optimizations and is based on drastically differing programming models. Performance portability across different platforms can be achieved by decoupling the algorithm description from the target implementation. We present Hipacc (http://hipacc-lang.org), a framework consisting of an open-source image processing DSL and a compiler to target CPUs, GPUs, and FPGAs from the same program. We demonstrate Hipacc's productivity by considering real-world computer vision applications, e.g. optical flow, and generating target code (C++, OpenCL, C-based HLS) for three platforms (CPU and GPU in a laptop and an FPGA board). Finally, we showcase real-time processing of images acquired by a USB camera on these platforms.*

LABSMILING: A SAAS FRAMEWORK, COMPOSED OF A NUMBER OF REMOTELY ACCESSIBLE TESTBEDS AND RELATED SW TOOLS, FOR ANALYSIS, DESIGN AND MANAGEMENT OF LOW DATA-RATE WIRELESS PERSONAL AREA NETWORKS BASED ON IEEE 802.15.4

Authors:
Carlo Centofanti, Luigi Pomante, Marco Santic and Walter Tiberti, University of L'Aquila, IT

Timeslots:
- UB05.8 (Wednesday, March 27, 2019 10:00 - 12:00)
- UB07.9 (Wednesday, March 27, 2019 14:00 - 16:00)
- UB09.6 (Thursday, March 28, 2019 10:00 - 12:00)

***Abstract**: Low data-rate wireless personal area networks (LR-WPANs) are constantly increasing their presence in the fields of IoT, wearable, home automation, health monitoring. The development, deployment and testing of SW based on IEEE 802.15.4 standard (and derivations, e.g. 15.4e), require the exploitation of a testbed as the network grows in complexity and heterogeneity. This demo shows LabSmiling: a SaaS framework which connects testbeds deployed in a real-world-environment and the related SW tools that make available a meaningful (but still scalable) number of physical devices (sensor nodes) to developers. It provides a comfortable out-of-the-box service designed to fulfill developer needs giving them full control on single motes (program, reset, physical power on/off, up/down links, commands/messages/packets in/from the network). Advanced services are: full-customizable testing scenario, validation/testing protocol compliances/extensions, run low level packet sniffers with QoS metrics.*

LOGIC MINIMIZER: LOGIC MINIMIZERS FOR PARTIALLY DEFINED FUNCTIONS

Authors:
Tsutomu Sasao, Kyu Matsuura, Kazuyuki Kai and Yukihiro Iguchi, Meiji University, JP

Timeslots:
- UB05.2 (Wednesday, March 27, 2019 10:00 - 12:00)
- UB08.2 (Wednesday, March 27, 2019 16:00 - 18:00)

***Abstract**: Logic Minimizers for Partially Defined Functions Tsutomu Sasao, Meiji University, Kanagawa 214-0034, Japan. abstract: This demonstration shows a minimization system for partially defined functions. The minimizer reduces the number of the input variables to represent the function using linear transformations. Applications include implementations of random functions; code converter; IP address table; English word list; and URL list. Outline of Demonstration In the demonstration, a PC and a poster are used to show: * Introduction of partially defined functions. * A method to reduce variables by linear decompositions. * Implementation of code converters. * Implementation of IP address tables. * Implementation of English dictionaries. * Implementation of random functions. * Implementation of URL lists.*

MASCARA: A MACHINE LEARNING AUTOMATIC SPEECH RECOGNITION PLATFORM FOR USERS WITH DYSARTHRIA

Authors:
Davide Mulfari, Gabriele Meoni and Luca Fanucci, University of Pisa, IT

Timeslots:
- UB02.6 (Tuesday, March 26, 2019 12:30 - 15:00)
- UB03.6 (Tuesday, March 26, 2019 15:00 - 17:30)
- UB06.8 (Wednesday, March 27, 2019 12:00 - 14:00)

***Abstract**: We exploit machine learning technology to build Automatic Speech Recognition (ASR) solutions for people with dysarthria, a speech disorder characterized by low intelligibility of users' speaking and related to many motor disabilities. Within the field of ASR, nowadays popular voice assistant solutions (e.g.,Apple Siri) perform poorly on dysarthric speech processing, so users with disabilities cannot benefit from such technologies in many scenarios, like smart home. To address these issues, a custom ASR has been prototyped using a speaker dependent approach: it recognizes predefined keywords from disabled Italian persons who have already shared their voices. The demo shows our edge computing platform for speech recognition and its usage within the field of human computer interaction. We also present a mobile app allowing users to record and to share voice while they say selected keywords. With these data, we enrich our speech model in order to serve many application scenarios.*

MDC: MULTI-DATAFLOW COMPOSER TOOL: DATAFLOW TO HARDWARE COMPOSITION AND OPTIMIZATION OF RECONFIGURABLE ACCELERATORS

Authors:
Francesca Palumbo[1], Carlo Sau[2], Tiziana Fanni[2], Claudio Rubattu[1] and Luigi Raffo[2]
[1]University of Sassari, IT; [2]University of Cagliari, IT

Timeslots:
- UB01.6 (Tuesday, March 26, 2019 10:30 - 12:30)
- UB05.6 (Wednesday, March 27, 2019 10:00 - 12:00)

***Abstract**: UNICA-Eolab and UNISS-IDEA booth is demonstrating the capabilities of the Multi-Dataflow Component (MDC) tool: a model-based toolset for design and development of virtual coarse-grain reconfigurable (CGR) circuits. MDC provides multi-function substrate composition, optimization and integration in real environments. 1 Baseline Core: automatic composition of CGR substrates. Inputs kernels are provided as dataflow networks, and target agnostic RTL description is derived. [FPGA(1)/ASIC(2)] 2 Profiler: automated design space exploration to determine the optimal multi-functional CGR substrate given a set of constraints. [2] 3 Power Manager: power consumption minimization. Model level identification of the logic regions to determine optimal power/clock domains and apply saving strategies. [1/2] 4 Prototyper: automatic generation of Xilinx-compliant IPs and APIs. [1] MDC is part of the H2020 CERBERO toolchain. Material: http://sites.unica.it/rpct/ and IDEA Lab Channel www.goo.gl/7fXme3.*

MECO: AN AUTONOMIC MANAGER FOR EDGE-COMPUTING PLATFORMS

Authors:
Gabriella D'Andrea, Tania Di Mascio, Luigi Pomante and Giacomo Valente, University of L'Aquila, IT

Timeslots:
- UB05.9 (Wednesday, March 27, 2019 10:00 - 12:00)
- UB07.8 (Wednesday, March 27, 2019 14:00 - 16:00)
- UB09.9 (Thursday, March 28, 2019 10:00 - 12:00)

***Abstract**: In the Cyber-Physical-Systems word, the need for hardware platforms able to satisfy increasing requirements in computing performance, while keeping the adaptability imposed by the interactions with the physical world is leading on the use FPGAs, due to their inherent run-time reconfigurability. So, this demo presents an implementation of a self-adaptive loop for edge- computing devices targeting FPGAs. An adaptive run-time manager, together with a smart monitoring system, evaluates the quality of service and determines whether is convenient to perform a dynamic partial reconfiguration. The whole development flow, that exploits a library of elements to compose the monitoring system and then selects the appropriate manager, will be shown by means of a reference use case implemented on a Zynq Ultrascale+ SoC. Finally, a comparison among different functionalities will be illustrated as well.*

MICROPLAN: MICRO-SYSTEM DESIGN AND PRODUCTION PLANNING TOOL

Authors:
Horst Tilman, Robert Fischbach and Jens Lienig, Technische Universität Dresden, DE

Timeslots:
- UB01.3 (Tuesday, March 26, 2019 10:30 - 12:30)
- UB03.1 (Tuesday, March 26, 2019 15:00 - 17:30)
- UB06.3 (Wednesday, March 27, 2019 12:00 - 14:00)
- UB10.3 (Thursday, March 28, 2019 12:00 - 14:30)

***Abstract**: We present a tool that enables to layout and plan the production of heterogeneous micro-systems. The tool consists of a simple layout editor, a visualization of the wafer utilization and eventually a calculation of the production cost for a given order quantity. Being superior with regard to performance, heterogeneous systems are often rendered unviable due to high production costs. However, using our tool allows users to design heterogeneous systems with an emphasis on low production costs. The tool is developed within the MICROPRINCE project and in close cooperation with X-Fab. The tool doesn't require installation and can be used by any visitor on their smartphone or computer.*

MROS AND ZYTLEBOT: DESIGN PLATFORMS FOR EMBEDDED ROBOT SYSTEMS

Authors:
Hideki Takase[1], Yasuhiro Nitta[1] and So Tamura[2]
[1]Kyoto University, JP; [2]Kyoto Universiy, JP

Timeslots:
- UB06.4 (Wednesday, March 27, 2019 12:00 - 14:00)
- UB08.9 (Wednesday, March 27, 2019 16:00 - 18:00)

***Abstract**: We are researching design platforms for robot systems based on ROS (Robot Operating System). In the booth, we will present the current status of two research activities. The first project is mROS, a lightweight runtime environment of ROS nodes. mROS offers a ROS-compatible communication library to be operated on the embedded mid-range processor which cannot be operated with Linux. mROS contributes to utilizing low power embedded devices into the ROS system. We will show the case study of mROS on the distributed camera system. The second is ZytleBot, an autonomous driving robot as an FPGA integrated platform utilizing the Xilinx programmable SoC. In ZytleBot, the FPGA performs preprocessing of the road surface image acquired from the camera and calculation of HOG feature calculation for signal detection. We achieved about 5 times faster performance by utilizing the FPGA. We will demonstrate the real-time signal detection task on the ZytleBot that won FPT'18 FPGA design competition.*

POETS: PARTIALLY ORDERED EVENT DRIVEN SYSTEMS

Authors:
Jonathan Beaumont[1], Ghaith Tarawneh[2], Shane Fleming[1], Matthew Naylor[3], Andrew Brown[4], Andrey Mokhov[2], Simon Moore[3] and David Thomas[1]
[1]Imperial College London, GB; [2]Newcastle University, GB; [3]University of Cambridge, GB; [4]University of Southampton, GB

Timeslots:
- UB08.6 (Wednesday, March 27, 2019 16:00 - 18:00)

***Abstract**: POETS technology is based on the idea of an extremely large number of small cores embedded in a fast, hardware, parallel communications infrastructure. The application network communication is effected by small, fixed size hardware data packets (a few bytes). This project is a collaborative effort between 4 UK universities, researching and developing a software methodology and the hardware to realise the potential of this architecture. A POETS booth will consist of live demonstrations of applications benefiting from this architecture, such as Graph Traversal algorithms, Heat Dissipation Equations and Dissipative Particle Dynamics. Applications run on hardware based in Cambridge, and laptops display visualisations of these applications, produced from data output received via wi-fi, allowing visitors to view these applications in real-time. Some of the demonstrations are interactive; a visitor can affect the application and see how this changes the outcome in real-time.*

PREESM: GENERATING ENERGY-OPTIMIZED ADAPTIVE SOFTWARE ON A HETEROGENEOUS PLATFORM WITH PREESM

Authors:
Maxime Pelcat[1], Karol Desnos[1], Daniel Menard[1], Florian Arrestier[1], Alexandre Honorat[1], Claudio Rubattu[2], Antoine Morvan[1], Julien Heulot[1] and Jean-François Nezan[1]
[1]INSA Rennes/IETR, FR; [2]UNISS, INSA Rennes/IETR, FR

Timeslots:
- UB03.5 (Tuesday, March 26, 2019 15:00 - 17:30)
- UB06.5 (Wednesday, March 27, 2019 12:00 - 14:00)
- UB08.5 (Wednesday, March 27, 2019 16:00 - 18:00)

***Abstract**: This Booth demonstrates how PREESM and SPIDER tools generate energy-optimized sensor-based adaptive software on a heterogeneous platform. PREESM is a rapid system prototyping tool provided with a runtime manager named SPIDER. PREESM simulates stream processing applications and generates code for multi/many-cores. Processing can either be statically mapped or adaptively managed by SPIDER. Steps when using PREESM are: 1- Model your Application: PREESM provides you with a dataflow language, designed to express parallelism. 2- Model your Architecture: PREESM simulates and generates code for a wide range of systems (e.g., ARM, DSP, FPGA). 3- Prototype and Run your Design: PREESM takes mapping decisions and provides early design space information such as scheduling, memory use, and core loads. PREESM and SPIDER are available on GitHub, and supported by tutorials and a reactive community. PREESM and SPIDER are part of the H2020 CERBERO toolchain. http://preesm.org*

REQV: A TOOL FOR REQUIREMENTS FORMAL CONSISTENCY CHECKING

Authors:
Luca Pulina[1], Massimo Narizzano[2], Armando Tacchella[2] and Simone Vuotto[1]
[1]University of Sassari, IT; [2]University of Genoa, IT

Timeslots:
- UB03.8 (Tuesday, March 26, 2019 15:00 - 17:30)
- UB07.10 (Wednesday, March 27, 2019 14:00 - 16:00)
- UB09.8 (Thursday, March 28, 2019 10:00 - 12:00)
- UB10.8 (Thursday, March 28, 2019 12:00 - 14:30)

***Abstract**: In the demo we will present ReqV, a tool for requirements formal consistency checking developed in the context of the H2020 EU project CERBERO (http://www.cerbero-h2020.eu/tools-and-tutorials/). ReqV takes as input a set of requirements expressed in natural language, so it does not require any background knowledge of formal methods and logical languages. A video tutorial is currently available at http://www.cluster-prossimo.it/docs/ReqV_video.mp4. The basic technologies used in ReqV are an extension of Property Specification Patterns to constrained numerical signals -- which enables to write useful requirements specifications in the context of Cyber-Physical Systems -- and Linear Temporal Logic satisfiability solvers for the formal consistency checking part. In the case of inconsistency of the set of input requirements, ReqV can also extract the minimal set of conflicting requirements, in order to help the designer to correct a wrong specification.*

RESCUE: EDA TOOLSET FOR INTERDEPENDENT ASPECTS OF RELIABILITY, SECURITY AND QUALITY IN NANOELECTRONIC SYSTEMS DESIGN

Authors:
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Timeslots:
- UB01.8 (Tuesday, March 26, 2019 10:30 - 12:30)
- UB02.8 (Tuesday, March 26, 2019 12:30 - 15:00)
- UB07.1 (Wednesday, March 27, 2019 14:00 - 16:00)
- UB08.1 (Wednesday, March 27, 2019 16:00 - 18:00)
- UB09.2 (Thursday, March 28, 2019 10:00 - 12:00)
- UB10.2 (Thursday, March 28, 2019 12:00 - 14:30)

***Abstract**: The demonstrator will introduce an EDA toolset developed by a team of PhD students in the H2020-MSCA-ITN RESCUE project. The recent trends for the computing systems include machine intelligence in the era of IoT, complex safety-critical applications, extreme miniaturization of technologies and intensive interaction with the physical world. These trends set tough requirements on mutually dependent extra-functional design aspects. RESCUE is focused on the key challenges for reliability (functional safety, ageing, soft errors), security (tamper-resistance, PUF technology, intelligent security) and quality (novel fault models, functional test, FMEA/FMECA, verification/debug) and related EDA methodologies. The objective of the interdisciplinary cross-sectoral team from Tallinn UT, TU Delft, BTU Cottbus, POLITO, IHP, IROC, Intrinsic-ID, Cadence and Bosch is to develop in collaboration a holistic EDA toolset for modelling, assessment and enhancement of these extra-functional design aspects.*

RISC-V VP: RISC-V BASED VIRTUAL PROTOTYPE: AN OPEN SOURCE PLATFORM FOR MODELING AND VERIFICATION

Authors:
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Timeslots:
- UB01.9 (Tuesday, March 26, 2019 10:30 - 12:30)
- UB05.10 (Wednesday, March 27, 2019 10:00 - 12:00)

***Abstract**: RISC-V, being an open and free Instruction Set Architecture (ISA), is gaining huge popularity as processor ISA in Internet-of-Things (IoT) devices. We propose an open source RISC-V based Virtual Prototype (VP) demonstrator (available at http://www.systemc-verification.org/riscv-vp). Our VP is implemented in standard compliant SystemC using a generic bus system with TLM 2.0 communication. At the heart of our VP is a 32 bit RISC-V (RV32IMAC) Instruction Set Simulator (ISS) with support for compressed instructions. This enables our VP to emulate IoT devices that work with a small amount of memory and limited resources. Our VP can be used as platform for early SW development and verification, as well as other system-level use cases. We support the GCC toolchain, provide SW debug, coverage measurement capabilities and support FreeRTOS. Our VP is designed as configurable and extensible platform. For example we provide the configuration for the RISC-V HiFive1 board from SiFive.*

SCCHARTS: THE KIELER SCCHARTS EDITOR - A MODULAR OPEN-SOURCE MODELING SUITE WITH AUTOMATIC DIAGRAM SYNTHESIS

Authors:
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Timeslots:
- UB02.7 (Tuesday, March 26, 2019 12:30 - 15:00)
- UB03.7 (Tuesday, March 26, 2019 15:00 - 17:30)
- UB05.7 (Wednesday, March 27, 2019 10:00 - 12:00)
- UB06.7 (Wednesday, March 27, 2019 12:00 - 14:00)

***Abstract**: When using high-level DSLs, the model-based approach promises a more transparent and efficient development process, for example in the hardware domain. By leveraging the compilation workflow to a meta level, the tool developer and the modeler can benefit from an interactive development process. Combined with modern transient view technologies, working with model transformation systems becomes transparent and less time consuming. Modeling tools should guide the modeler to potential issues and provide means to understand details about the transformations. The KIELER SCCharts Editor is a modular, open-source modeling suite, using the synchronous language SCCharts as main demonstrator. The editor supports compilation, automatic syntheses of intermediate results, and deployment to different platforms, both software and hardware. The modular concept of the compiler framework allows for rapid application and prototype development. The concepts can be applied to other languages or domains.*

SETA-RAY: A NEW IDE TOOL FOR PREDICTING, ANALYZING AND MITIGATING RADIATION-INDUCED SOFT ERRORS ON FPGAS

Authors:
Luca Sterpone, Boyang Du and Sarah Azimi, Politecnico di Torino, IT

Timeslots:
- UB01.10 (Tuesday, March 26, 2019 10:30 - 12:30)
- UB03.9 (Tuesday, March 26, 2019 15:00 - 17:30)
- UB08.7 (Wednesday, March 27, 2019 16:00 - 18:00)
- UB09.7 (Thursday, March 28, 2019 10:00 - 12:00)

***Abstract**: One of the main concern for FPGA adopted in mission critical application such as space and avionic fields is radiation-induced soft errors. Therefore, we propose an IDE including two software tools compatible with commercial EDA tools. RAD-RAY as the first and only developed tool capable to predict the source of the SET phenomena by taking in to account the features of the radiation environment such as the type, LET and interaction angle of the particles, the material and physical layout of the device exposed to the radiation. The predicted source SET pulse in provided to the SETA tool as the second developed tool integrated with the commercial FPGA design tool for evaluating the sensitivity of the industrial circuit implemented on Flash-based FPGA and mitigate the original netlist based on the performed analysis. This IDE is supported by ESA and Thales Alenia Space. It has been applied to the EUCLID space mission project that will be launched in 2021.*

SWARM: SELF-ORGANIZED WIRING AND ARRANGEMENT OF RESPONSIVE MODULES

Authors:
Daniel Marolt and Jürgen Scheible, Hochschule Reutlingen, DE

Timeslots:
- UB05.3 (Wednesday, March 27, 2019 10:00 - 12:00)
- UB08.3 (Wednesday, March 27, 2019 16:00 - 18:00)

***Abstract**: This demonstration exemplifies a new automation methodology for layout design of analog integrated circuits: Self-organized Wiring and Arrangement of Responsive Modules (SWARM). Based on the idea of decentralization, it addresses the task with an innovative multi-agent system. Its basic principle, similar to the roundup of a sheep herd, is to let responsive layout modules (implemented as procedural generators) interact with each other in a user-defined layout zone. Each module is allowed to autonomously move, rotate and deform itself, while a supervising control organ successively tightens the layout zone to steer the interaction towards increasingly compact layout arrangements. Considering various principles of self-organization, SWARM is able to evoke the phenomenon of emergence: although each module only has a limited viewpoint and selfishly pursues its personal objectives, remarkable overall solutions can emerge on the global scale.*

T-CREST: THE TIME-PREDICTABLE MULTICORE PROCESSOR T-CREST

Authors:
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Timeslots:
- UB03.2 (Tuesday, March 26, 2019 15:00 - 17:30)
- UB07.6 (Wednesday, March 27, 2019 14:00 - 16:00)

***Abstract**: Future real-time systems, such as advanced control systems or real-time image recognition, need more powerful processors, but still a system where the worst-case execution time (WCET) can be statically predicted. Multicore processors are one answer to the need for more processing power. However, it is still an open research question how to best organize and implement time-predictable communication between processing cores. T-CREST is an open-source multicore processor for research on time-predictable computer architecture. In consists of several Patmos processors connected by various time-predictable communication structures: access to shared off-chip, access to shared on-chip memory, and the Argo network-on-chip for fast inter-processor communication. T-CREST is supported by open-source development tools, such as compilation and WCET analysis. To best of our knowledge, T-CREST is the only fully open-source architecture for research on future real-time multicore architectures.*

TIMING & POWER CHARACTERIZATION FRAMEWORK FOR EMBEDDED PROCESSORS

Authors:
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Timeslots:
- UB01.1 (Tuesday, March 26, 2019 10:30 - 12:30)
- UB02.1 (Tuesday, March 26, 2019 12:30 - 15:00)
- UB05.1 (Wednesday, March 27, 2019 10:00 - 12:00)
- UB06.1 (Wednesday, March 27, 2019 12:00 - 14:00)

***Abstract**: We present a framework that significantly reduces the effort for creating accurate energy/timing models for embedded processors covering different conditions (e.g. varying temperature and clock frequency). It supports the systematic collection of large amount of timing and power data needed to cover the complete microprocessors' ISA in different working conditions. Since manual measurements are tedious and error-prone we present an automated approach. The physical setup consists of a processor board, a power measurement device, a heating element and a logic analyser observing the processor's GPIOs. The software consists of a code-generator for characterization binaries, a control program which orchestrates the physical setup and the evaluation software which generates the desired timing and power data. We will demonstrate this framework for an ARM Cortex-M microcontroller and present interesting and even undocumented behaviour while using certain CPU and FPU features.*

TINYWIDS: A INTRUSION DETECTION SYSTEM FOR WIRELESS SENSOR NETWORKS

Authors:
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Timeslots:
- UB09.1 (Thursday, March 28, 2019 10:00 - 12:00)
- UB10.1 (Thursday, March 28, 2019 12:00 - 14:30)

***Abstract**: In the domain of Wireless Sensor Networks (WSN), providing an effective security solution to protect the motes and their communications is challenging. Due to the hard constraints on performance, storage and energy consumption, normal network-security related techniques cannot be applied. Focusing on the "Intrusion Detection" problem, we propose a real-world application of our WSN Intrusion Detection System (WIDS). WIDS exploits the Weak Process Models to classify potential security issues in the WSN and to notify the operators when an attack tentative is detected. In this demonstration, we show how our IDS works, how it detects some basic attacks and how the IDS can evolve to fullfil the needs of secure WSN deployments.*

WTG: WAVEFORM TRANSITION GRAPHS: A DESIGNER-FRIENDLY FORMALISM FOR ASYNCHRONOUS CIRCUITS

Authors:
Danil Sokolov, Newcastle University, GB

Timeslots:
- UB01.2 (Tuesday, March 26, 2019 10:30 - 12:30)
- UB02.2 (Tuesday, March 26, 2019 12:30 - 15:00)

***Abstract**: Asynchronous circuits are a promising class of digital circuits that has numerous advantages over their synchronous counterparts, especially in the domain of "little digital" speed-independent (SI) controllers. Nonetheless, their adoption has not been widespread, which in part is attributed to the difficulty of entry into complex models employed for specification of SI circuits, like Signal Transition Graphs (STGs), by electronic designers. We propose a new model called Waveform Transition Graphs (WTGs) which resembles the timing diagrams, that are very familiar to circuit designers, and defines its formal behaviour semantics. This formalization enables translation of the WTGs into equivalent STGs in order to reuse the existing body of research and tools for verification and logic synthesis of speed-independent circuits. The development of WTGs has been automated in the Workcraft toolkit (https://workcraft.org), allowing their conversion into STGs, verification and synthesis.*

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