DATE PhD Forum 2019

The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

The DATE PhD Forum is associated with the DATE 2019 Welcome Reception and will take place on Monday, March 25, 2019, from 1800 - 2100 at the DATE venue in the Lunch Area. All registered conference delegates and exhibition visitors are kindly invited.

Robert Wille, Johannes Kepler University Linz (Chair, DATE PhD Forum 2019)

PhD Forum Committee
Juergen Alt, Intel Germany
Davide Bertozzzi, University of Ferrara
Armin Biere, Johannes Kepler University Linz
Alberto Bosio, Lyon Institute of Nanotechnology
Luigi Carro, UFRGS
Krishnendu Chakrabarty, Duke University
Anupam Chattopadhyay, Nanyang Technological University
Deming Chen, UIUC
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Rolf Drechsler, University of Bremen/DFKI
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Tim Güneysu, Ruhr-Universität Bochum
Ian Harris, University of California Irvine
Tsung-Yi Ho, National Tsing Hua University
Oliver Keszocze, Friedrich-Alexander University Erlangen
Gi-Joon Nam, IBM Research
Yehuda Naveh, IBM Research - Haifa
Martin Omana, DEI - University of Bologna
Felipe Rocha da Rosa, UFRGS
Daniele Rossi, University of Hertfordshire
Andreas Steininger, Vienna University of Technology
Daniel Tille, Infineon Technologies
Shigeru Yamashita, Ritsumeikan University

Admitted Presentations

1. Adaptive Runtime Resource Management for Mobile CMPs through Self-awareness
   Bryan Donyanavard, University of California, Irvine, US

2. Optimization of Trustworthy Biomolecular Quantitative Analysis Using Cyber-Physical Microfluidic Platforms
   Mohamed Ibrahim, Duke University, US

3. Analysis and Optimization of Reliability Issues of VLSI Power Grid Networks
   Sukanta Dey, Indian Institute of Technology Guwahati, IN

   Alwin Zulehner, Johannes Kepler University Linz, AT

5. New Views for Stochastic Computing: From Time-Encoding to Deterministic Processing
   M. Hassan Najafi, University of Louisiana at Lafayette, US

6. System-level Mapping and Synthesis of Data Flow-Oriented Applications on MPSoCs
   Tobias Schwarzer and Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

7. ReDFD: Reusing Design-for-Debug Structures of On-Chip Architectures to Enhance Performance
   Neetu Jindal, Indian Institute of Technology Delhi, IN

8. Compositional Circuit Design with Asynchronous Concepts
   Andreas Grimmer, Johannes Kepler University Linz, AT

10. Worst-Case Execution Time Guarantees for Runtime-Reconfigurable Architectures  
    Marvin Damschen, Lars Bauer and Joerg Henkel, Karlsruhe Institute of Technology, DE

11. Architecture and Programming Model Support For Reconfigurable Accelerators in Multi-Core Embedded Systems  
    Satyajit Das, Université de Bretagne-Sud, FR

12. Supervised Testing of Embedded Concurrent Software  
    Jasmin Jahic, Fraunhofer IESE, DE

    Deepak Mathew, University of Kaiserslautern, DE

    Sukarn Agarwal, Indian Institute of Technology Guwahati, IN

15. Design Techniques for Energy-Quality Scalable Digital Systems  
    Daniele Jahier Pagliari, Politecnico di Torino, IT

16. Protecting application admission, execution and peripheral access in many-core systems  
    Luciano Lores Caimi and Fernando Moraes  
    Universidade Federal da Fronteira Sul, BR; PUCRS University, BR

17. MuTARe: A Multi-Target Adaptive Reconfigurable Architecture  
    Marcelo Brandalero, Universidade Federal do Rio Grande do Sul, BR

18. Bitstream-level Proof-Carrying Hardware  
    Tobias Wiersema, Paderborn University, DE

    Vladimir Herdt, University of Bremen, DE

20. Hybrid-DBT: Hardware-Accelerated Dynamic Binary Translation targeting VLIW processors  
    Simon Rokicki, Irisa, FR

21. Low-power Architectures for Automatic Speech Recognition  
    Hamid Tabani, Barcelona Supercomputing Center, ES

22. Low Overhead & Energy Efficient Storage Path for Next Generation Computer Systems  
    Athanasios Stratakopoulos, The University of Manchester, GB

23. A Model driven Framework with Assertion Based Verification Support for Embedded Systems Design Automation  
    Muhammad Waseem Anwar, National University of Sciences & Technology (NUST), PK

25. Multiple NoC based Custom Implementation and Traffic Distribution to attain Energy Efficient CMPs  
    Sonal Yadav, Vijay Laxmi and Manoj Singh Gaur, MNIT Jaipur, IN

26. True Random Number Generators for FPGAs  
    Bohan Yang, ESAT/COSIC and iMinds, KU Leuven, BE

27. HW/SW Co-Design Methodology for Mixed-Criticality and Real-Time Embedded Systems  
    Vittoriano Muttillo, University of L’Aquila, IT

28. Improving Bundled-Data Handshake Circuits  
    Norman Kluge, Hasso-Plattner-Institut, University of Potsdam, DE
29. **IC Design of an Inductorless DC/DC Converter with Wide Input Voltage Range in Low-Cost CMOS**  
   Gabriele Ciarpi, University of Pisa, IT

30. **Monolithic-3D Integration based Memory Design techniques towards Robust and in-memory computing**  
    Srivatsa Rangachar Srinivasa, John (Jack) Sampson, Meng-Fan (Marvin) Chang and Vijaykrishnan Narayanan  
    Penn State University, US; Penn State University, US; National Tsing Hua University, TW; Penn State University, US

    Mahdi Tala, University of Ferrara, IT

32. **Adaptive Knobs for Resource Efficient Computing**  
    Anil Kanduri, University of Turku, FI

33. **Device-Circuit Co-design Employing Phase Transitioning Materials for Low Power Digital Applications**  
    Ahmedullah Aziz, Purdue University, US

35. **Emerging Computing: Acceleration of Big Data Applications**  
    Mohsen Imani, University of California San Diego, US