Novel Application of Spintronics in Computing, Sensing, Storage and Cybersecurity

(Invited)

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***Abstract*— With conventional Von Neumann computing struggling to match the energy-efficiency of biological systems, there is pressing need to explore alternative computing models. CMOS switches, although universal, fails to offer additional features to meet this end goal. Recent experimental studies have revealed that spintronics possess many promising features that can not only enable non Von Neumann compute models but also high-density storage, sensing of environmental parameters and protection from cybersecurity threats. This paper provides an in-depth study of spintronics and its relation to these novel aspects from device, circuit and system standpoint.**

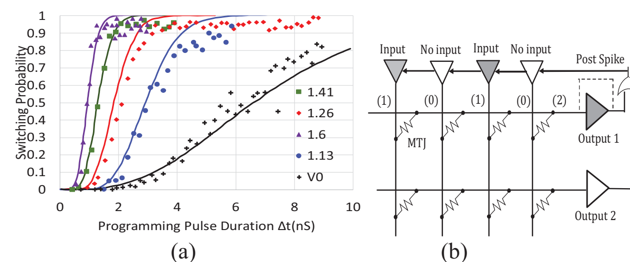
I. Introduction

Spintronic technology operates on the principle of manipulation of electron spins to perform computation and storage. Contrary to charge-based computing spintronics requires less energy to switch the output making them energy-efficient. The non-volatility is also desirable for many applications especially energy-constrained Internet-of-Things (IoT) [1] that mostly stay OFF and occasionally perform computing. Persistence of information during inactive cycles save re-initialization energy. Among spintronic devices, Magnetic RAM (MRAM), Spin-Transfer Torque RAM (STTRAM), Domain Wall Memory (DWM) and spin memristors are some of the most investigated structures [2-3]. Spintronic devices can be exploited for ultra-low power computing based on artificial neural network. Interestingly, variety of new structures have been proposed to suit particular application e.g., full adders [4], neurons [5-6] and synapses [7-10]. Challenges e.g., poor sense margin and high write current are resolved by using techniques such as, [22-23].

The most promising effect of spintronic memories is current induced modulation of magnetization dynamics (discovered in MTJ and DWM) as it opens door to energy-efficient logic and memory design. Interaction between injected current and local magnetization creates several Spin-Transfer-Torque (STT) mechanisms that are excellent sources of entropy. The thermally activated electrons in the material add to the entropy. Besides, magnetization dynamics is typically nonlinear in nature and the magnet is also sensitive to physical randomness. For example, DW motion in rough Nanowire (NW) makes it resistant to modeling-based attacks [56] that are prevalent in CMOS-based security primitives. These features coupled with shift-based access and energy-efficient computation lead to easy adoption of spintronic devices for security applications such as, encryption engines [13], TRNG [12], Physically Unclonable Function (PUF) [11], tamper sensors and so on. In the following sections, we review the application of spintronics in computing, sensing, storage and cybersecurity.

II. Application of Spintronics in Computing

Conventional computational architectures are based on Von Neumann architecture that utilize physically separated memory and processing element. This separation causes performance and energy bottlenecks for the architecture due to frequent data transfer between the memory and processor. Artificial neural network has been proposed as a promising computing alternative for certain class of problems. In recent years, the exploitation of nano devices as synapses and neuron is gaining interest in the design of neuromorphic engines. Resistive RAM (RRAM) and Phase Change Memory (PCM) as plastic synaptic device [15-19] has been proposed that can be programmed in an analog fashion. In this section, we focus on the neuron and synapse design using spintronic memories and their novel application in signal processing and computing.



(a) (b)

Fig. 1 Experimental measurement of stochastic switching probability in MTJ as a function of programming time and voltage [8]; and, (b) schematic of the crossbar architecture for STDP learning system.

A. Spintronic Synapse

- **Stochastic MTJ synapse:** STT memory has been explored in [8] as a stochastic memristive device. The time required for switching STTRAM state is a random quantity [14]. The write latency distribution shows a long tail and the worst case write bits could eventually limit the system performance [22]. Although the resistance difference between two states of MTJ is not large, using MTJ as a synapse this behavior can be considered as a useful feature to implement stochastic learning circuits. Fig. 1(a) shows experimental measurement of stochastic switching. Note that the switching probability changes with respect to programming pulse duration and amplitude. Fig. 1(b) shows a spiking neural network architecture which implements a Spike Timing Dependent Plasticity (STDP) rule which is a model for synaptic learning in the brain. Many works have exploited memory devices to implement STDP [20-21]. The key idea of STDP is that if neuron A repeatedly contribute to firing of neuron B the synaptic weight between neuron A and B will increase and vice versa. In other words, if the presynaptic spike arrives before the postsynaptic spike, the synaptic weight increases; otherwise, it decreases. The circuit consist of CMOS input neuron (Fig. 1(b)), MTJ synapse and CMOS output neuron. The MTJs are organized in a crossbar fashion connecting inputs to output neurons. Input neurons provide the inputs as asynchronous spikes to the network which is transmitted to the output depending on MTJ state which act as a synaptic weight (shown by (1)). Output neurons is a Leaky Integrate and Fire (LIF) circuit. The input spikes inject current into crossbar which is integrated by output neurons. The neuron will spike (post spike) if the current received (by output neuron) is greater than

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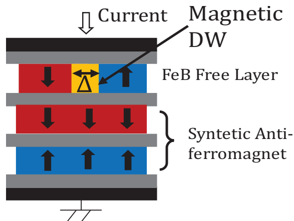


Fig. 2 MgO based magnetic tunnel junction with the domain wall in the FeB FL. Δ is the width of the domain wall.

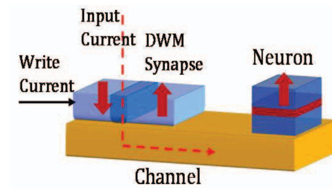


Fig. 3 DW synapse with channel interface [10].

a certain threshold that inhibits other output neurons from spiking. The MTJs connected to the spiking neuron receive post synaptic spikes (shown by (2)). If the input of corresponding MTJ is active (inactive) in a recent time window, it has a probability of switching to low (high) resistance state.

- **Spin Torque Memristor Synapse [9]:** The spin memristor is similar to MTJ with a single magnetic domain wall in its free layer (FL) as shown in Fig. 2. The DW can move forward (backward) by applying positive (negative) voltage due to spin torque effect. The DW stabilizes in different position along the NW when applied voltage is removed. Two extreme value of resistance are P and AP magnetization of FL with respect to top layer of synthetic anti-ferromagnet. This device is prone to cycle to cycle variability due to random nature of DW pinning and process variation (PV). However, it has been shown that this variability effect is negligible on learning accuracy. Moreover, the impact of variability can be minimized by applying short voltage pulses instead of DC current.
- **DWM Synapse [10]:** In DWM synapse, the programmable spin injection strength emulates the weighting operation in a synapse (Fig. 3). The current is applied along the NW to write the weight into DWM. During programing, input current is injected into channel through the DW in vertical direction. Note that displacement of DW from the center is proportional to the spin polarization of charge current flowing through channel. If DW is situated in left end of NW the charge current flowing through the channel is maximally up-spin and vice versa. Using longer NW improves the quantization of DW location providing larger number of weight levels. Moreover, employing physical notches in NW can improve stability at the notch locations which provides higher writing accuracy. A 350nm length NW with 22nm interval for each notch is used to attain 16 levels of weigh. This synapse can be incorporated in a latch (Fig. 5(b)) to weight the magnitude of current flowing from transmitting to receiving neuron.

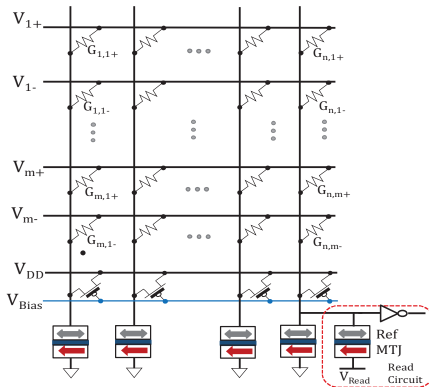


Fig. 4 Neuromorphic system implementation using STT-Neuron [5].

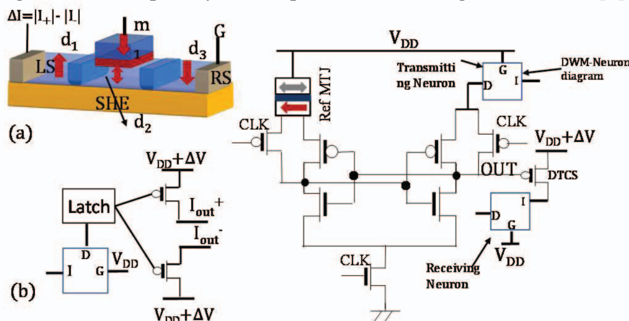


Fig. 5 (a) Unipolar DWM-neuron; and, (b) circuit integration for unipolar neuron. CMOS latch detects the neuron state and transmit current to receiving neurons through DTCS transistor.

B. *Spintronic Neuron*

- **STT-Neuron [5]:** Two basic operations in artificial neural network are weighted summation of inputs and thresholding operation. In [5] MTJ has been exploited to implement thresholding operation of a neuron in a memristive crossbar array. The weighted synaptic summation of current is performed by a resistive crossbar array where the conductance of memristive element act as a synaptic weight converting input voltage into current. Fig. 4 shows the resistive crossbar where each horizontal line provides an input voltage across each resistive synapse while each vertical line provides an input current to the STT-Neuron where is placed at the end of the vertical column. Memristor is employed to implement the resistive synapse. The weights are implemented in a bipolar fashion where two rows of input (V_{i+} and V_{i-}) are used for each input. $V_{i+}= V_{i-}=0$ represent logic '0' whereas $V_{i+}=V_{DD}$ and $V_{i-}=-V_{DD}$ represents logic '1'. If the weight $G_{i,j}$ for the j-th neuron connected to input V_i is positive then the memristor connected to V_{i+} is programmed to the corresponding low resistance state while the memristor connected to V_{i-} is programmed to high resistance state and vice versa. The current I_j is proportional to the weighted summation of the inputs V_i and the synaptic weights $G_{i,j}$. The sign of the charge current defines the excitatory/inhibitory state of the input current, thereby, determines the final state of STT-Neuron. In order to implement STT-Neuron as a thresholding device, the excitatory synaptic current must be greater than $I_{critical\ (AP\text{->}P)}$ and inhibitory current is less than $I_{Critical(P\text{->}AP)}$. In order to meet this requirement an additional PMOS transistor is connected to row in crossbar array is exploited to provide a bias current. The advantage of this technique is that by setting $I_{bias,j} = I_{critical(AP\text{->}P)}$ the current requirement for switching is provided by source biasing of PMOS transistor and small inhibitory or excitatory synaptic current makes the MTJ to switch state. Note that the neuron is reset to AP state. For the inhibitory negative current the MTJ will not switch to P state as the current is lower than the critical current whereas the MTJ will switch to P state for an excitatory current greater than critical current.
- **DW Neuron [6-7]:** In the previous crossbar array, the STT-Neuron can be replaced by DW-Neuron. A shift based programming is proposed in [7]. It is shown that domain wall motion based write is faster and consume less energy compared to MTJ based write. Thus, ultra-low voltage current mode operation of DWM can be exploited to realize summation and thresholding operation in neural networks. Fig. 5(a) shows a 3-

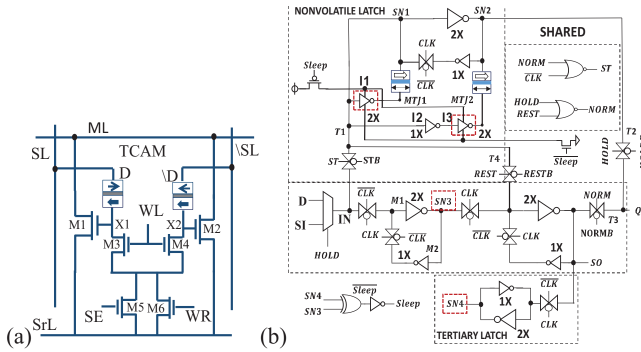
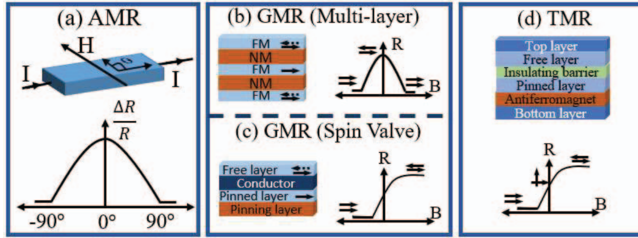


Fig. 6 (a) 6T-2MTJ CAM [26]; and, (b) state retention flip-flop [27].



FM= Ferromagnetic layer, NM= Non-magnetic layer

Fig. 7 Structures of (a) AMR; (b) GMR (multi-layer); (c) GMR (spin valve); and, (d) TMR sensors (reproduced from [28]).

terminal DWM- based spin neuron composed of a free magnetic domain d_2, which forms a Magnetic Tunnel Junction (MTJ) with a fixed magnet m_1 situated on top of it. The DWs can be shifted forward and backward by injecting charge current from left-shift (LS) and right-shift (RS) contacts. Therefore, the d_2 can be written to P/AP state. This device can detect the direction of current that flows through it. Thus, it can be exploited for current thresholding in neural network array. The minimum current required for writing to the free domain depends upon the critical current density for domain wall motion. Spin- orbital coupling in form of Spin Hall Effect (SHE) is proposed for low power high speed DW motion [7]. A dynamic latch (Fig. 5(b)) is used to sense the state of MTJ thereby obtaining the sign function of a neuron [6]. The latch drives a triode region current source transistor (DTCS) which transmit the synaptic current to the receiving neurons. For unipolar DWM neuron the current received from positive and negative synapses is subtracted in the charge mode in the crossbar array (Fig. 4) This requires 3 voltage levels V, V-ΔV and V+ΔV. The DTCS transistor connected to positive weights drives the current for receiving neurons (I_{out}^{+}), while transistor connected to negative weights drains the current from receiving neurons (I_{out}^{-}). The source terminal of the output transistors is biased at V+ΔV/V-ΔV while the ground terminal of receiving neuron is biased at V where V=1V and ΔV~30mV. As a result, the synaptic current flows across a small terminal voltage ΔV reducing the static power consumption. The magnitude of current flowing from transmitting neuron to receiving neuron can be weighted in two ways: using am memristive device in crossbar architecture (Section II.A) or weighted DTCS transistor. The spin based DWM-neuron in neuromorphic computing achieves 15X-100X lower computation energy.

C. *DWM in Signal Processing and CNN [24][25]*

In the hardware implementation of deep learning algorithms such as Convolutional Neural Networks (CNNs), vector-vector multiplications and memories for storing parameters take a significant portion of area and power consumption. In [24], a DWM based design of CNN convolutional layer is proposed where the resistive cell sensing mechanism is exploited to design a low-cost DWM-based cell arrays for storing parameters. The unique serial access mechanism and small footprint of DWM are also used to reduce the area and power cost of the input registers for aligning inputs. Contrary to the conventional implementation using Memristor-Based Crossbar (MBC), the bit-width of the proposed CNN convolutional layer is extendable for high resolution classifications and training.

Since SRAM based embedded memory and flip-flop based shift registers consume a significant portion of area and power in digital signal processing applications, a DWM based embedded memories is proposed in [25] for survivor-path memories and Last-In First-Out (LIFO) in Viterbi decoder, First-In-First-Out (FIFO) register files in FFT processor and bitonic sorter, and input register of distributed arithmetic based FIR filter. The design exploits the unique serial access mechanism, non-volatility and small footprint of DWM for area/power saving.

D. *STTRAM in Search Engine [26] and State Retention Elements [27]*

Content Addressable Memory (CAM) is widely used in the applications where searching a specific pattern of data is a major operation. Conventional CAMs suffer from area, power, and speed limitations. In [26], a STTRAM based Ternary CAM (TCAM) cells are proposed (Fig. 6(a)). The NOR type TCAM cell exhibits 62.5% (33%) reduction in number of transistor compared to conventional CMOS TCAM (spintronic TCAMs). Both NOR and NAND type CAMs support up to 256-bit word under process and temperature variation by exploiting adaptive wordline voltage control. The application of STTRAM in designing non-volatile flip-flop is explored in [27]. The design (Fig. 6(b)) can work even under sudden power outage and support enhanced scan capability for testability.

III. Application of Spintronics in Sensing

The equivalent resistance of spintronic devices is a function of external magnetic field and temperature which makes them suitable to detect and measure magnetic field and temperature.

A. *Magnetic Sensors*

The sensors are divided into 3 categories based on their physics:

- **Anisotropic Magnetoresistance (AMR):** The resistance of ferromagnetic material increases when the current through the material is in the same direction as the magnetic force (angle, θ=0°) and decreases as θ increases from 0° to |90°| (Fig. 7 (a)). *Application:* To measure external magnetic field (direction/amplitude) [29-30] and as contactless rotational sensors due to its ability to detect/measure rotational information of a magnetic object [28].

- **Giant Magnetoresistance (GMR):** GMR sensors can be realized with magnetic multilayers (Fig. 7(b)) or spin valves (Fig. 7(c)). Multilayer GMR are designed with repetitions of Ferromagnetic (FM) and Nonmagnetic (NM) layers (Fig. 7 (b)). Multilayer GRM stack has high resistance when the FM layers are antiparallel to each other and the resistance decreases as they gradually align to parallel configuration (min. when they are parallel). Multilayer GMR shows long linear detectable field range but provide relatively low sensitivity. However, spin

valve GMR provides better sensitivity due to addition of a free FM layer (see Fig. 7(c)). The fixed FM layer is pinned by an antiferromagnetic layer to keep its magnetic orientation fixed, irrespective of external magnetic field. *Application:* To measure and detect external field [28] and to read information from hard disc drive where data are stored as magnetic information [31].

- **Tunneling Magnetoresistance (TMR):** TMR sensor (also called MTJ (Fig. 7(d))) has a thin (0.5 ~ 2 nm) insulating barrier between free and pinned FM layer. The equivalent resistance of MTJ is high (low) if FL magnetic orientation is AP (P) compared to the pinned layer. *Application:* To measure and detect magnetic field with high sensitivity [32] and to image microwave reflection [33-34].

Power and performance analysis: AMR sensors consume ~10mW under continuous operation whereas GRM/TMR sensors achieve sub mW and µW power consumption respectively [28]. GMR sensor has a much lower noise than TMR sensor [35]. However, MR_{TMR} is 1 ~ 2 orders of magnitude higher than MR_{GMR} sensors [36]).

B. Temperature Sensors

TMR and GMR sensors are also proposed as thermal sensors [37-38] as their equivalent resistances are also a function of external temperature. Domain wall motion based spintronic memristors are also proposed as temperature sensors [39-40].

C. Miscellaneous Sensors

TMR sensors are also proposed as biosensors for gene or micro-organism detection [41]. MTJ-based spintronic strain-gauge sensor is proposed with a gauge factor of 5000 [42]. Spintronic memristors are proposed for magnetic bio-sensing [43] and interfacing with DNA and solid-state devices [44]. Spin-Torque Nano-Oscillators are proposed for magnetic pattern recognition [45]. Vehicle detection based on the local disturbance in the earth's magnetic field by the vehicle (ferrous material) is also proposed in [28].

IV. Application of Spintronics in Storage

In this section, we present the application of spintronics in high-density storage applications.

A. Crosspoint Storage [46]

Access device has been predominantly a three terminal transistor for STTRAM limiting the memory footprint. Selection device is critical to enable memory scaling and large scale integration. Selector diodes (SD) such as Mixed Ionic Electronic Conduction (MIEC), Metal-Insulator-Metal (MIM) tunneling, oxide heterojunction p-n, and Schottky diodes for ReRAM have been extensively studied. Integration of SD and ReRAM have been attempted due to material compatibility and simplistic structure. Unlike ReRAM, MTJ do not need electroforming which simplifies the integration however, new challenges are imposed such as low TMR, and, read/write and retention sensitivity to the noise and variations. Also, SD can increase the switching voltage which is undesirable for cache. However, SD will allow high-density and scalability by enabling 3D stacking to enable new applications e.g., Internet-of-Things (IoTs) which warrants study of SD-MTJ integration. In [46], a simulation based study is conducted to understand the integration potential of MIIM SD with MTJ. It has been shown that the intended asymmetry in diode I-V behavior provides better sense margin for larger arrays. Design challenges and device-circuit co-optimization and novel techniques e.g., write voltage biasing and series/parallel connected SD for robustness and retention is proposed for on-chip cache and external storage applications. The proposed structure can also enable 3D stacking of MTJ for density beyond $4F^2$.

B. STTRAM for embedded Flash (eFlash) Replacement [47]

In embedded application such as microcontroller SoC of IoTs, eFlash is widely employed. However, eFlash is also associated with cost, poor reliability and high write energy consumption. Therefore, replacing eFlash with emerging NVMs is desirable in IoTs. However, STTRAM brings several new security and privacy challenges such as magnetic attacks that pose a significant threat to sensitive programs stored in memory. These challenges are investigated in [47] and a novel memory architecture is proposed for attack resilient IoT network. The information redundancy present in a homogeneous peer-to-peer connected IoT network is exploited to restore the corrupted memory of any IoT node after magnetic attack. The number of corrupted bits are reduced by using high retention STTRAM at the cost of one-time write energy overhead since restoring program memory from other IoT incurs high energy overhead.

V. Application of Spintronics in Cybersecurity

In this section, we summarize spintronic PUFs and TRNGs.

A. PUF

PUF is a security primitive to prevent cloning of chips. It replaces the hard-coded key in the IC with specifically designed circuits that work on the principle of challenge-response. The response to a particular challenge is based on the process condition of the chip which makes the response hard to clone. We review various spintronic (STTRAM/MRAM/DWM) PUFs below that exploit spintronic properties.

- *PUF-1 [48]:* This work proposes a STTRAM PUF that exploits the randomly initialized magnetic orientation of MTJ FL to generate a PUF response. During registration phase, it compares two STTRAM bits that are in two complementary rows for generating the response. The technique relies on the noise and the sense amplifier offset to decide the response if the bits are initialized to the same value. Repeatability is ensured by writing back the corresponding complementary values to the STTRAM bits. Furthermore, a fuzzy extractor is used to enhance PUF response quality.
- *PUF-2 [49]:* This MRAM PUF employs the random initialization of MTJ due to its physical variations which create random tilt of energy barrier. The distribution of tilt angle is Gaussian. Therefore, the magnetic orientation of the MTJ FL is prone to prefer certain initial position much similar to SRAM PUF. The proposed technique first destabilizes the magnetic orientation of the MTJ FL hard axis and releases it to settle to its preferred state.
- *PUF-3 [50]:* An err-PUF is proposed in [56] based on the cell error rate distribution of STTRAM. A generated stable fingerprint based on a novel concept called Error-rate Differential Pair (EDP) is used rather than using the error rate distribution directly. The technique does not need modification of the read/write circuits. It has been shown that, if two cells that are an EDP, they have considerably different error rates

even with the environmental variation. The BER of the same STTRAM array under Error-Least-State (the best case with lowest error rate) and Error-Most-State (the worst case with highest error rate) needs to be considered. To be an EDP pair, the difference of the total number of errors in N round of test for the corresponding two cells should be >= N, in all cases.

- *PUF-4 [51]:* In [51], a PUF is proposed exploiting the high variability and uncontrollability of MTJ resistance in AP state and the transistor threshold voltage. First, all cells including reference cells are written to AP state. The reference cells are read, and the current through the cells are averaged to get a reference current, I_{ref}. Now, each active cell is read, and if the read current, $I>I_{ref}$, the sense amplifier interprets the stored data as '0'. However, if the read current, $I<I_{ref}$, the sense amplifier interpret the stored data as '1'. The output of the sense amplifier is stored as the PUF value.
- *PUF-5 [52]:* A MTJ-PUF is proposed based on intrinsic properties of spin transfer switching (STS) [52]. Due to PV and extrinsic properties, each measured MTJ shows different switching voltage for both switching cases; P→AP and AP→P. For PUF extraction, at first, all cells are reset to P. Next, a specific voltage, V_{PUF} is applied to the MTJs to induce switching with a 50% probability. A random distribution of P/AP state is achieved due to stochastic switching nature. Now, every MTJ is read by the PUF extraction circuit, and they are categorized into three groups: i) much less than 50%(white); ii) around 50% (gray); and iii) much more than 50% (black). The result is stored, and the array is reset. For a better reliability, the extraction operation is repeated multiple times to extract white and black bits and discard gray bits. Finally, the black bits are chosen for the PUF signature. It is technically impossible to make a clone as this PUF exploits stochastic STS.
- *PUF-6:* In [53], a buffer free memory based PUF (BF-MPUF) is proposed. This PUF can be realized using any emerging NVM technologies like STTRAM, PCM, RRAM, etc. and it can produce random keys without disturbing the data stored in the memory. This technique does not require buffer storage and additional write back operation circuit like conventional SRAM-based PUF as it utilizes the non-volatility of NVMs resulting lower power and area overhead. For memory mode, first a voltage is applied to the memory cell, and the current I_{dat} is measured. Then, the measured current is compared with a reference current, $I_{ref} = (I_H + I_L)/2$, where I_H and I_L are the reference current of AP and P state respectively. The polarity of this comparison is output as a digital bit. However, for PUF mode, at first the cells are checked to determine the current state, and I_{ref} is set to I_H if cell stores '1', otherwise I_{ref} is set to I_L. Therefore, both P and AP states are exploited to generate responses according to the current state of the NVM without disturbing its state. SRAM PUF with embedded MTJ for added stability is also proposed in [54].
- *PUF-7:* In [55-56], the physical randomness in the DWM is employed to generate response for a challenge. A relay-PUF is designed with multiple stages of parallel NWs [55]. Conventional muxing circuit between each consecutive stage is introduced to toggle the paths and create new challenges. Furthermore, a higher number of stages also provides a higher degree of randomness in the signature. An arbiter block is placed at the end to compare the arrival times of the respective DWs. In contrast to conventional delay-PUF, the relay-PUF also provides extra degrees of freedom to choose challenges namely shift pulse voltage, pulse width and pulse frequency. These new challenges can be employed to increase the number of challenges with low area overhead. The response of the relay-PUF (0 or 1) is determined by an arbiter that decides the early arrival of DWs in parallel NWs. The switching of paths in association with shift pulse width, duration and frequency provides several layers of randomness in the race condition. As the physical roughness varies NW-to-NW, the DWs will race with different speeds and the response will vary between chips.

B. True Random Number Generator (TRNG)

TRNG harnesses the natural entropy present in the system such as thermal noise. The chaotic phenomena of MTJ has been exploited to generate true random numbers.

- *TRNG-1 [12]:* In [12], a spintronic dice is proposed where the key idea is to first reset the MTJ to AP state and next excite the FL of the MTJ to the bifurcation point by applying a current pulse and let the magnetization settle in the random state due to thermal noise. To improve the randomness of the response and kill the correlation among bits they are XOR'ed with each other. Although promising, the reset pulse is detrimental to MTJ reliability. Furthermore, the sharing of reset and sense circuit makes sense MTJ susceptible to read disturb.
- *TRNG*-2 [57]: A conditional perturb technique is proposed in [57] which avoids the usage of reset pulse by applying an optimal pulse and brings the MTJ to 50% switching probability contour. Therefore a high-quality key generation is realized at lower energy with faster rate. Elimination of reset pulse also prolongs the MTJ lifetime.
- *TRNG*-3 [58]: In [58], the MTJ is disturbed using DC current and the random value is sensed and processed using an entropy extractor. A tamper detection unit is also designed by monitoring a run of 0s or 1s in the random number generated from the MTJ array.

A complementary polarized MTJ structure is proposed to enhance the randomness of bits generated [59]. The precession of MTJ FL is also employed to generate random number [60]. Current pulse width is applied and adjusted to cause the FL precession that settles to a random state. A similar technique applies a current in between read and write current to the MTJ to change its switching probability between 0 and 1. The random bit is extracted and processed further for key generation [61]. Other MTJ-based TRNG is also proposed by exploiting pulse width/amplitude [62] and voltage [63] with Error Correcting Code (ECC) as post processing circuit.

Design challenges: The stability of spintronic PUFs and TRNGs can be affected by factors such as, thermal noise, read disturb, write failure, reliability/ endurance failure, tampering and side channel attacks. These require further study.

VI. CONCLUSIONS

We reviewed the application of spintronics in computing, sensing, storage and cybersecurity. Innovations at device-level and circuits can open new avenues and application domains for this promising technology.

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