Low-Power 3D Integration using Inductive Coupling Links for Neurotechnology Applications

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Abstract—**Three dimensional system integration offers the ability to stack multiple dies, fabricated in disparate technologies, within a single IC. For this reason, it is gaining popularity for use in sensor devices which perform concurrent analogue and digital processing, as both analogue and digital dies can be coupled together. One such class of devices are *closed-loop neuromodulators*; neurostimulators which perform real-time digital signal processing (DSP) to deliver bespoke treatment. Due to their implantable nature, these devices are inherently governed by very strict volume constraints, power budgets, and must operate with high reliability. To address these challenges, this paper presents a low-power inductive coupling link (ICL) transceiver for 3D integration of digital CMOS and analogue BiCMOS dies for use in closed-loop neuromodulators. The use of an ICL, as opposed to through silicon vias (TSVs), ensures high reliability and fabrication yield in addition to circumventing the use of voltage level conversion between disparate dies, improving power efficiency. The proposed transceiver is experimentally evaluated using SPICE as well as nine traditional TSV baseline solutions. Results demonstrate that, whilst the achievable bandwidth of the TSV-based approaches is much higher, for the typical data rates demanded by neuromodulator applications (0.5 - 1 Gbps) the ICL design consumes on average 36.7% less power through avoiding the use of voltage level shifters.**

I. INTRODUCTION

Three dimensional (3D) system integration promises the ability to stack multiple disparate dies (e.g. analogue, digital, MEMS), fabricated in different process technologies within a single, small form-factor, low-power IC. For this reason, an increasing number of devices which perform concurrent analogue and digital processing are being fabricated 'in 3D' to enhance their performance, whilst simultaneously reducing power consumption and size. One such class of devices are closed-loop neuromodulators. Open-loop neurostimulators (which deliver therapy according to a predefined program regardless of the patient's clinical symptoms) are an established treatment for patients suffering from movement disorders, chronic pain, or epilepsy [1]. However presently, researchers look towards *closed-loop* chronically implantable devices which are able to analyse neural signals in real-time and respond with customised neural stimulation [2], resulting in more efficient therapy. This, however, necessitates the introduction of powerful digital signal processing [3] (DSP) to detect bio-markers pre-emptively (e.g. for sensing oncoming seizures) [3]. These digital processing elements must co-exist

with the analogue amplifiers and filters found in existing open-loop solutions, and as such the use of 3D integration has been proposed, where analogue sensing dies and digital processing dies are stacked and interconnected vertically [4].

Typically for 3D system integration, the research community look to through silicon vias (TSVs) [5] which can provide electrical pathways passing entirely through each die, facilitating face-to-back stacking. However, their formation introduces many additional processing stages and mechanical stresses within the IC which can pose reliability and yield concerns [6]. Contactless inductive coupling links (ICL) have been proposed as an alternative to TSVs for 3D integration. ICLs rely on electromagnetic (EM) coupling between coils to transmit data between dies and hence hold potential to greatly enhance the reliability of 3D-ICs [7].

Aside from reliability, when considering 3D-ICs for neuro-implantable devices (which typically operate on a stringent energy budget), the most important consideration is their power consumption. This paper, therefore, investigates the feasibility of using ICLs for 3D integration in implantable neurotechnology applications, focussing on their power-consumption. We propose an ICL for contactless integration of low-power digital CMOS and analogue BiCMOS (SiGe) dies, with intrinsic voltage level conversion. The proposed design is experimentally validated using SPICE and compared with nine equivalent TSV-based benchmark implementations. The novel contributions of this paper are, therefore, summarised as follows:

- Design of a low-power ICL, with intrinsic voltage level conversion, for 3D integration of digital (CMOS) and analogue (BiCMOS) dies to meet the fabrication requirements of typical closed-loop neuromodulators.
- Experimental validation of the proposed ICL between TSMC 65nm LP CMOS and IBM 180nm BiCMOS tiers using SPICE, demonstrating that the proposed design operates with high reliability (bit-error-rate (BER) $< 10^{-15}$) and low latency (0.72ns) at a data-rate of 0.64Gbps (a typical data-rate for neuromodulator applications).
- Detailed power analysis of the proposed design compared with nine TSV-based benchmark designs (on an iso-area basis) when used in conjunction with voltage level shifting circuitry. Our results demonstrate that, the proposed ICL reduces power consumption by 36.7% on average, when compared to the benchmark TSV-based designs operating at 0.64Gbps.
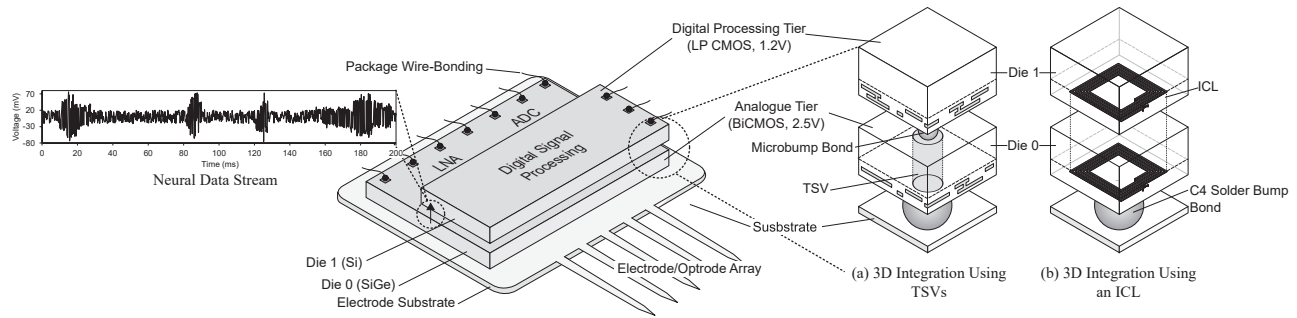
Fig. 1: Illustratory diagram of an implantable closed-loop neuromodulation device with stacked analogue and digital tiers using (a) through silicon vias or (b) an inductive coupling link (ICL).

II. INDUCTIVE COUPLING LINK DESIGN

A. Background

Fig. 1 illustrates the stacked 3D implantable neuromodulator considered in this paper. The system consists of a base substrate containing an electrode (or optrode) array for neural sensing and stimulation, an analogue Bi-CMOS tier providing low-noise amplification and filtering of the sensed neural signal (in addition to analogue-to-digital conversion) and a digital CMOS tier for performing real-time data analysis. Due to the requirement that the analogue die must be flip-chip bonded to the substrate, the digital and analogue dies must be stacked in a face-to-back fashion. For this style of 3D system integration, the research community typically looks to through silicon vias (as shown in Fig. 1(a)) which provide high-density low latency connectivity [8]. Despite this, TSV-based 3D integration still faces many challenges such as high manufacturing and testing complexity [7] in addition to poor yields, making 3D systems incorporating TSVs prone to low-reliability [6].

More recently, research has looked to the use of ICLs for 3D integration. As shown in Fig. 1(b) ICLs can make use of conventional IC fabrication processes without modification, resulting in a low-complexity, robust alternative to TSVs [9]. To encode data, inductive coupling transceiver implementations typically use inductive nonreturn-to-zero (NRZ) signalling [10], where current pulses are transmitted at every data transition with positive and negative polarities indicating *rising* and *falling* edges. They are therefore, current driven, meaning that when communicating data between two tiers with disparate supply voltages, additional voltage level conversion circuitry can be avoided (as demonstrated in [11], where an inductive coupling transceiver for integration of 65nm and $0.35\,\mu m$ CMOS processes is presented). This makes their power efficiency more favourable for heterogeneous 3D integration where each tier has a different supply voltage, as considered in this paper.

In this section we present an ICL design for the 3D integration scenario presented in Fig. 1; interfacing a BiCMOS analogue tier operating at 2.5V and a low-power digital CMOS tier operating at 1.2V. The data rate requirement is assumed to be 0.64Gbps (10MHz sampling at a quality of 64 bits-
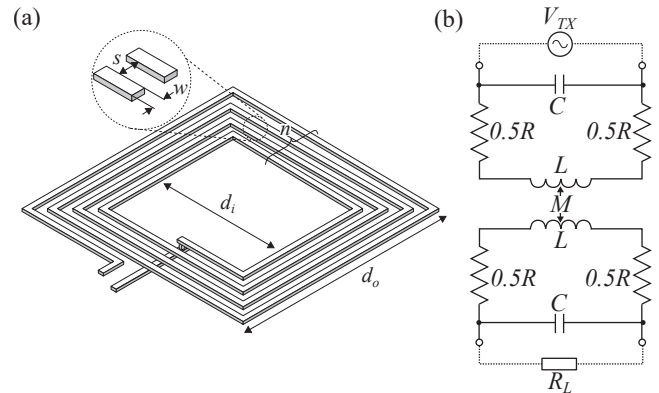

Fig. 2: (a) Monolithic square inductor layout parameters. (b) RLMC inductive coupling channel model [10].

per-sample), typical of neurosensors. As communication in this application is largely mono-directional, this paper will focus on the up-link (from analogue to digital) transceiver design, however the entire design and analysis process could be equally applied in the opposite direction.

B. Architecture Using an Inductive Coupling Link

1) Coil Layout: The first stage in the ICL design process is determining a pair of coil layouts for establishing EM coupling between tiers. As square-spiral coils offer the highest inductance per unit area (compared to hexagonal, octagonal and circular monolithic inductors [12]), a coil of this type will be considered. Fig. 2(a) shows a monolithic square inductor annotated with its primary layout parameters: outer dimension d_o, number of turns n, trace width w and spacing s. To ensure the accuracy of our modelling assumptions, in this paper, the silicon verified $200\,\mu m$ inductor layout from [13] is used with geometric parameters shown in Table I. For electrical modelling, the RLMC ICL channel model (proposed in [10]) shown in Fig. 2(b) is used. Here it is assumed that each coil exhibits resistance and capacitance as well as inductance, and mutual inductance between the coils. To translate the physical coil layout into a corresponding electrical channel model, physical measurements of R and L (from the authors of [13]) and simulated values of M and C (obtained using

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Parameter	Value
n	5
w	$9.0\,\mu m$
s	$0.72\,\mu m$
d_o	$200\,\mu m$

TABLE I: Physical inductor layout parameters.

Parameter	Value
R	$9.1\,\Omega$
L	$48\,nH$
M	$12.11\,nH$
C	$389\,fF$

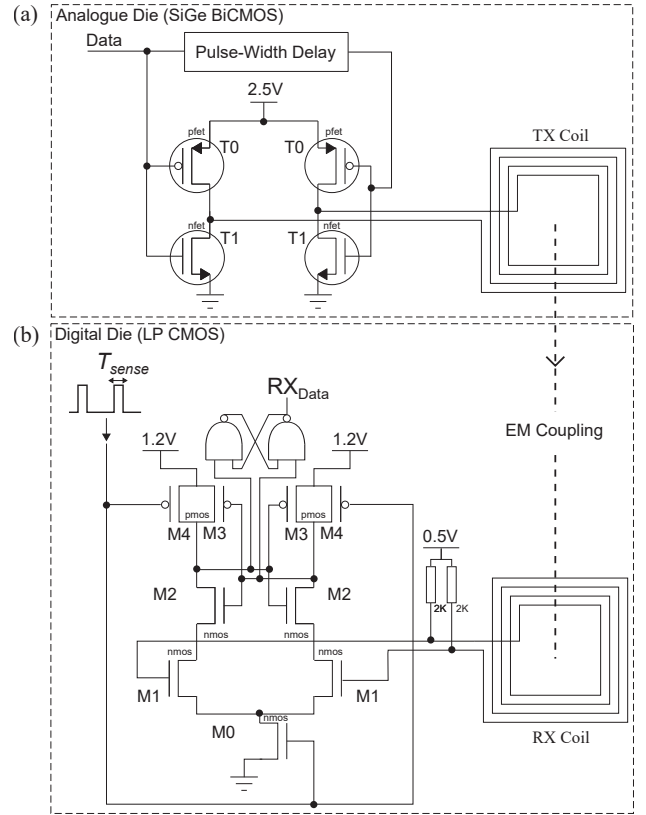TABLE II: Extracted electrical parameters.

Fig. 3: ICL transceiver implementation for heterogeneous integration of an analogue bi-CMOS and digital CMOS process.

Device	T0	T1	M0	M1	M2	M3	M4
Size (μm)	8.5	4.7	0.55	3.9	0.55	1.2	1.7

TABLE III: Transistor width selections.

CST MW Studio) are used, assuming a die thickness of $65\,\mu m$. These fitted parameters are shown in Table II. Using this inductor layout (for both Tx and Rx Coils) results in a coupling coefficient, k of 0.25.

2) Transceiver Design: For the transceiver implementation, the NRZ inductive signalling scheme presented in [10], outlined in (Section II-A) is used. This scheme is a bi-phase modulation scheme whereby transmitted current pulses represent data edges, and the polarity of the current pulse represents whether the data edge is *rising* or *falling*.

a) Transmitter: For the transmitter, this NRZ scheme can be implemented simply using the H-Bridge topology shown in Fig. 3(a). Here, a short clockwise current pulse, of a duration determined by the pulse-width delay element, will flow through the coil when the data signal transitions from $0V \rightarrow 2.5V$, representing a *rising* data edge. Conversely, a current pulse of the same duration will flow counter-clockwise through the coil when the data signal transitions from $2.5V \rightarrow 0V$, representing a *falling* data edge. The delay element can be realised using an even n-stage inverter chain (non-inverting), such that the current pulse duration is given by $nt_{p,inv}$, where $t_{p,inv}$ is the propagation delay of a single inverter.

b) Receiver: Due to EM induction, these current pulses will induce a corresponding voltage signal in the Rx coil with a magnitude determined by the coupling coefficient (k) between the two tiers. In Section II-B1, k was found to be 0.25, and hence from analysing the ICL channel model in Fig. 2, received voltage pulses with magnitudes of the order of 100mV can be expected. The receiver design, therefore must incorporate amplification in order to successfully detect the transmitted pulses. To achieve this, the low-power sense amplifier flip-flop circuit (SAFF) [14] presented in Fig. 3(b) is used, consisting of a sense amplifier is coupled to a NAND SR latch. Here the transistors, M1, form a differential amplifying pair determining the gain of the arrangement. The duration of the *pre-charge* and *evaluate* phases (defined by T_{sense}) are manually selected, depending on the operating frequency, to distinguish the received signal from extraneous noise.

For the SAFF to operate correctly, the received signal must be biased such that the transistor pair M1 operate in their saturation region. To achieve this, a bias voltage of 0.5V is selected, delivered through $2\,k\Omega$ resistors to maintain a high input impedance.

III. EXPERIMENTAL EVALUATION AND RESULTS

The proposed ICL design was experimentally evaluated using the Cadence Spectre circuit simulator. Commercial li-braries (IBM 7wl and TSMC N65) were used to simulate the design assuming equiprobable pseudo-random binary input streams with rise and fall times of $0.01 \times f$. As a comparison benchmark, nine alternative TSV-based implementations were also simulated in conjunction with the associated voltage level conversion circuitry required for them to operate. The form of these TSV-based solutions in addition to the transistor sizes used for both ICL and TSV implementations are detailed in the following subsections.

A. ICL Transistor Sizing

To ensure correct operation of the ICL, with high power efficiency, each of the transistors T0 - T1 and M0 - M4 were manually sized. Table III documents each of these transistor width selections (each uses the nominal gate length). Important design decisions include the sizing of FETs T0 and T1 to establish the transmit current pulse magnitude and ensure symmetricity of the system (T0 and T1 were sized at $8.5\,\mu m$ and $4.7\,\mu m$ respectively) and the sizing of M1 ($3.9\,\mu m$) to determine the amplification in the SAFF arrangement.
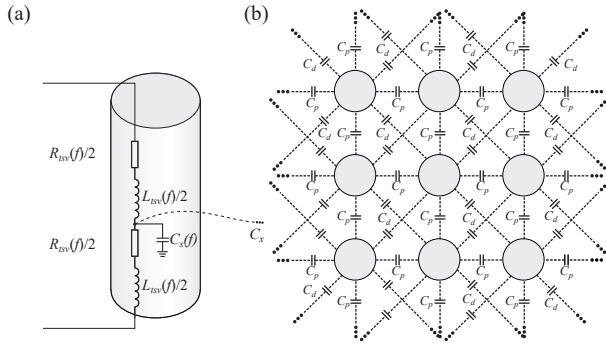
Fig. 4: (a) Electrical TSV model (where C_x denotes the coupling connections shown in (b)). (b) Coupling capacitance values in an n × n TSV square array.

B. Comparison Against Through Silicon Vias

To establish a benchmark for power comparisons, a selection of TSV-based alternative designs were also evaluated. As TSVs have a smaller area footprint than inductive coupling links, to maintain fair comparison, our study was performed on an iso-area basis with a budget of $0.052\,\text{mm}^2$ (the estimated footprint of the proposed ICL). For the TSV-based benchmarks to make use of the full area allowance, scenarios of 1:1 replacement (TSVs to ICLs) in addition to $1{:}n^2$ replacement, where each ICL is replaced by an $n \times n$ array of through silicon vias with the same area footprint were investigated. For fair comparison, we considered the aggregate data rate for the interface such that, in the case of an $n \times n$ array, the data rate through each via, f_{tsv}, is equivalent to f/n^2, reducing power consumption. Three different TSV styles were considered ($32\,\mu\text{m}$ TSVs [15] at $180\,\mu\text{m}$ pitch, $15\,\mu\text{m}$ TSVs [16] at $75\,\mu\text{m}$ pitch, and $15\,\mu\text{m}$ TSVs [16] at $30\,\mu\text{m}$ pitch) in addition to three different TSV routing patterns (outlined in Section III-B2) resulting in a total of nine TSV-based designs.

1) TSV Modelling: In order to model TSV parasitics for subsequent analysis, the electrical model shown in Fig. 4 (a), proposed by Weerasekera *et. al*, was used [17]. Here, it is assumed that each via exhibits resistance, $R_{tsv}(f)$, and inductance, $L_{tsv}(f)$, between its own terminals, in addition to self-capacitance, $C_s(f)$, and coupling capacitance between vias (each of which are frequency dependant). In this paper, as shown in Fig. 4 (b), we consider two coupling capacitances namely *planar coupling* in the x or y direction, $C_p(f)$, and *diagonal coupling* $C_d(f)$. To determine representative values for each of these parameters, finite element modelling software (CST MW Studio) was used. Parameters were obtained for the various literature-based TSV sizes and pitches outlined above, which are detailed in Table IV in addition to the extracted RLC fitted values at a frequency of 1GHz.

2) TSV Routing: Fig. 5 illustrates the three different TSV routing patterns which were considered in this work. In case (a) the full $n \times n$ TSV array is utilised for signal carrying TSVs and hence the signal is multiplexed n^2 ways such that each TSV is clocked at $1/n^2$ of the data frequency. Whilst
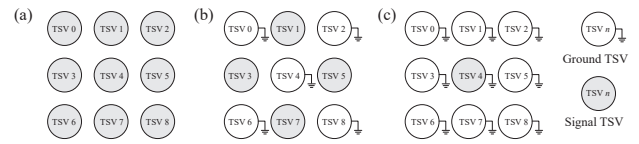

Fig. 5: (a) S-S-S, (b) G-S-G, and (c) Isolated TSV routing patterns.

TABLE IV: TSV modelling parameters for each TSV array style. Extracted at 1GHz.

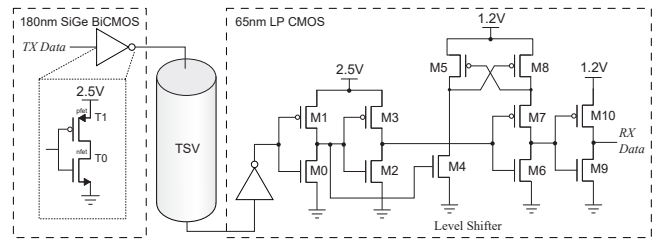| Style	Description	Parameters (at 1GHz)
[a]	$32\,\mu\text{m}$ TSVs [15] at $180\,\mu\text{m}$ pitch	$R_{tsv} = 0.529\,\Omega$, $L_{tsv} = 97.2\,\text{pH}$, $C_s = 51.8\,\text{fF}$, $C_{cx,y} = 51.8\,\text{fF}$, $C_{cdiag} = 42.6\,\text{fF}$
[b]	$15\,\mu\text{m}$ TSVs [16] at $75\,\mu\text{m}$ pitch	$R_{tsv} = 0.952\,\Omega$, $L_{tsv} = 1.01\,\mu\text{H}$, $C_s = 50.4\,\text{fF}$, $C_{cx,y} = 19.8\,\text{fF}$, $C_{cdiag} = 17.5\,\text{fF}$
[c]	$15\,\mu\text{m}$ TSVs [16] at $30\,\mu\text{m}$ pitch	$R_{tsv} = 0.952\,\Omega$, $L_{tsv} = 1.473\,\mu\text{H}$, $C_s = 76.8\,\text{fF}$, $C_{cx,y} = 24.3\,\text{fF}$, $C_{cdiag} = 19.0\,\text{fF}$

Fig. 6: TSV test configuration including drive inverters conjunction with a 3 stage voltage level converter.

this may seem like the most effective way to utilise the available area, and hence the most power efficient strategy, it is often advised that, to reduce coupling between neighbouring vias, especially at high frequencies, grounded vias should be inserted periodically within the array [18]. This leads to the ground-signal-ground (G-S-G) pattern shown in case (b). Finally, we also considered the case of a single signal carrying TSV (1:1 ICL to TSV replacement), shown in (c).

3) Voltage Level Conversion: As the two processes considered for integration in this paper have different supply voltages, additional level shifting circuitry is required when performing integration using TSVs. For experimental validation, level shifters were implemented in the 65nm tier, due to its favourable power efficiency. To model this level conversion, the push-pull level conversion circuit presented in Fig. 6 was used. This design was selected as it maintains very low quiescent power consumption by ensuring that there is never a constant path from either supply voltage to ground. For the implementation of this level shifter, each transistor (M0-M10) was sized with nominal length, 60nm, and width of 200nm to manage uni-directional signal conversion from 2.5V.

C. Results

Using the aforementioned TSV models, the proposed ICL design, and the 9 equivalent TSV based alternatives were simulated at a range of operating frequencies between 200 MHz
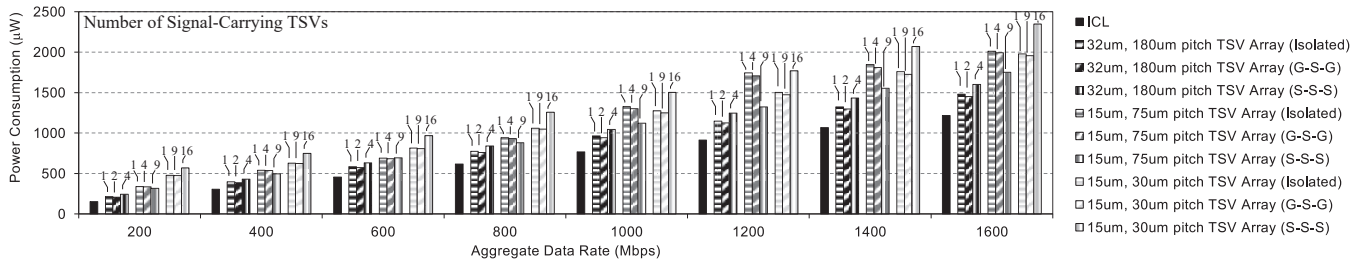
Fig. 10: Power consumption vs aggregate data-rate for each interface style whilst simulating communication between a 2.5V 180nm analogue BiCMOS die and a 1.2V 65nm LP CMOS digital die.
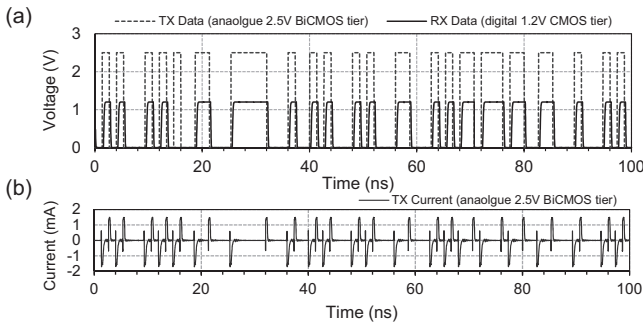

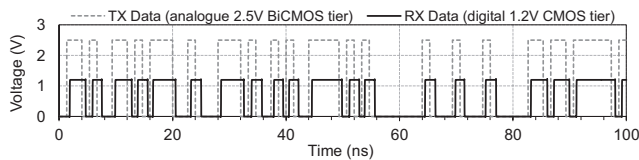Fig. 7: Operation of the proposed ICL transceiver, with intrinsic level conversion, at 0.64GHz.

Fig. 8: Operation of the proposed CMOS level shifter implementation in conjunction with a $35\,\mu m$ TSV link, at 0.64GHz.
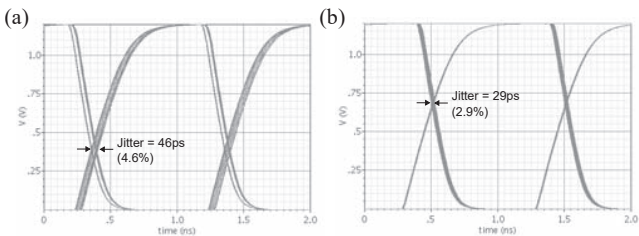

Fig. 9: Eye diagram illustrating jitter *RX Data* at 1GHz using (a) The proposed ICL and (b) A $32\,\mu m$ TSV.

and 1.6 GHz (selected to mimic typical data-rate requirements of closed-loop neuromodulators), to ascertain the power consumption of each approach. The following sub-sections document our results.

1) Functional Verification: Initially, the functionality of the proposed ICL design was assessed. Fig 7 shows the SPICE simulation results of the transceiver's operation. Here, the top trace (Fig. 7(a)) shows the transmitted and received data signals being communicated between the analogue (2.5V BiCMOS) and digital (1.2V CMOS) tiers with only 0.63ns

latency. Additionally, Fig. 7(b) highlights the operation of the proposed transceiver design, showing the pulsed transmitter current (1.4mA pulses in 0.11ns durations). Fig. 8 shows the operation of the TSV model and voltage level conversion circuitry presented in Fig. 6. Again, the level conversion between dies operates correctly with a latency of 0.58ns.

2) ICL Reliability: Having established that both designs operate as expected, the reliability of the proposed ICL was evaluated. An eye diagram showing the jitter in the received signal (*RX Data*) when using the ICL to transmit data at 1GHz is presented in Fig. 9(a). Fig. 9(b) also shows the received signal whilst using a single $32\,\mu m$ TSV for comparison. Whilst it is evident that the TSV outperforms the contactless ICL (due to reduced RC parasitics), the ICL still exhibits high reliably with only 4.6% jitter in the received signal at 1GHz (the maximum frequency which would likely be required for neural data). The BER whilst using the proposed ICL was also simulated, and found to be in the order of 10^{-15}. Considering the data-rate requirements of the application, assuming continuous operation, this equates to approximately 2 bit-flip errors per month. Considering the analogue nature of the source data (and the associated errors likely introduced in analogue-to-digital conversion), this level of communication error is insignificant and therefore, the results demonstrate sufficient reliability for use in closed-loop neuromodulators.

3) ICL and TSV Bandwidth Comparison: Following this, the bandwidth of each approach was evaluated and the results are shown in Table V. Here, it can be observed that the bandwidth achieved by the proposed ICL is 1.6 GHz, beyond which the RC delay of the coil resistance and coil capacitance causes detrimental inter-symbol interference in the received signal. The aggregate bandwidths of each of the TSV-based approaches (incorporating voltage level conversion circuitry) were also analysed. It can be observed that the TSV-based solutions exhibit much higher achievable bandwidths than the proposed ICL, again due to their reduced RC parasitics. Whilst bandwidth is an important consideration, typical neuro-sensors generate less than 1Gbps of data meaning that the bandwidth of the proposed ICL is still ample for the application considered.

4) ICL and TSV Latency Comparison: The latency of all 10 approaches was also evaluated for an aggregate data-rate of 0.64 Gbps and the results are shown in Table V. It can

TABLE V: Bandwidth, latency and energy per bit values for ICL and TSV based integration approaches.

Integration Method	Aggregate Bandwidth	Average Latency (at 0.64Gbps)	Energy Per Bit
Inductive Coupling Link (ICL)	1.6 GHz	0.72ns	0.85pJ/bit
32 μm TSVs [15] at 180 μm pitch[1]			
In Isolation	4.3 GHz	0.31ns	1.03pJ/bit
G-S-G	8.5 GHz	0.61ns	0.94pJ/bit
S-S-S	11.5 GHz	0.62ns	1.05pJ/bit
15 μm TSVs [16] at 75 μm pitch[1]			
In Isolation	3.8 GHz	0.46ns	0.99pJ/bit
G-S-G	8.6 GHz	0.76ns	0.90pJ/bit
S-S-S	16.2 GHz	0.78ns	1.12pJ/bit
15 μm TSVs [16] at 30 μm pitch[1]			
In Isolation	3.8 GHz	0.50ns	1.29pJ/bit
G-S-G	24.6 GHz	0.89ns	1.25pJ/bit
S-S-S	42.1 GHz	0.94ns	1.40pJ/bit

be observed that the proposed ICL operates with low latency (0.72ns), of a similar magnitude to the TSV-based approaches which must incorporate voltage level conversion circuitry.

5) ICL and TSV Power Comparison: Finally, the power consumption of each approach was evaluated for a range of data-rates typical of implantable neuro-modulators. The results are shown in Fig. 10. Here, the x-axis represents the aggregate throughput of the approach (in the case of an $n \times n$ TSV array, this is equal to $n^2 \cdot f_{tsv}$) and the y-axis shows the total power consumption of each link. Results are presented for all 9 TSV-based approaches and the total number of signal carrying TSVs in each design is marked above each bar.

Of the TSV-based approaches, we can observe that the larger, 32 μm, TSVs perform better than the smaller 15 μm TSVs in terms of power consumption, likely due to the reduced parasitic capacitances between vias of this size. It can also be observed from Fig. 10 that the use of G-S-G routing is broadly more power efficient than the other routing approaches at the investigated operating frequencies (due to the trade-off which exists between the clock frequency of each via, and the amount of additional voltage conversion circuitry). Additionally, results demonstrate that in all 10 cases, for each of the examined data-rates, the proposed ICL design operates with the lowest power consumption, outperforming the TSV-based approaches by an average of 36.7%. This is due to the additional power overhead introduced in voltage level conversion between the two IC tiers when using through silicon vias. Table V shows the best-case energy per bit consumed whilst using each approach. It can be observed that the proposed approach consumes less energy than the benchmark TSV solutions by between 5.6% (15 μm TSVs at 75 μm pitch with G-S-G routing) and 39.3% (15 μm TSVs at 30 μm pitch using S-S-S routing).

IV. Conclusions

This paper presents an ICL transceiver for low-power 3D integration of stacked digital (LP CMOS) and analogue (BiCMOS) dies for use in closed-loop implantable neuro-

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[1]Additional voltage level conversion circuitry (required for interfacing the two tiers) is incorporated in these simulation results.

modulators. The adoption of inductive coupling means that standard fabrication processes can be used without alteration, improving yield when compared to TSVs. In addition to this, the contactless nature of the ICL provides intrinsic voltage level conversion, avoiding the power overheads of supplementary voltage level converters between dies. The proposed transceiver design is experimentally validated through SPICE simulation and was found to operate with high reliability (BER $< 10^{-15}$) and low latency (0.72ns) at data rates up to 1.6 Gbps. Additionally, whilst the achievable bandwidth per area of ICLs is much lower than TSVs, for data rates typical of neuromodulator applications the ICL design consumed on average 36.7% less power than the nine alternative TSV-based designs explored in this paper, making it ideally suited for applications in this domain.

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