NBTI Aged Cell Rejuvenation with Back Biasing And Resulting Critical Path Reordering for Digital Circuits in 28nm FDSOI

Ajith Sivadasan[1,2], Riddhi Jitendrakumar Shah[1,2], Vincent Huard[1], Florian Cacho[1]
[1]STMicroelectronics – 850 rue Jean Monnet, 38926 Crolles, France
Contact: ajith.sivadasan@st.com

Lorena Anghel[2]
[2]TIMA, 46, avenue Félix Viallet, 38031 Grenoble, France

***Abstract*— Increasing demands from Autonomous Driving and IoT markets are pushing the need for products with advanced CMOS nodes that guarantee a high level of performance and at the same time having to comply with industrial regulatory standards like ISO26262, AEC-Q100 etc. Implementation of NBTI & DiR Reliability models for 28nm FDSOI, developed in-house, are fundamental means to evaluate the reliability of digital IPs during the design phase. Process, Temperature, Voltage, Workload based Aging are mission profile parameters traditionally taken into account for design margin evaluations and critical path pruning. A precise critical path selection methodology is highly important considering the In-situ monitor Insertion and Critical Path Replica generation strategies to be applied to Runtime Reliability assessment with the vision to move towards dynamic wear out management solutions. This paper recommends the consideration of the silicon technology feature of back biasing as an important parameter while selecting Critical Paths for circuits fabricated with FDSOI process. Back biasing is an add-on feature of this technology with ABB (adaptive back biasing) techniques having been used to compensate for PVT variations or aimed at a gain in the overall digital circuit performance. This technique is now being increasingly applied to aging mitigation. The back-biasing gain for an aged digital IP is quantified while performing design stage Gate Level Analysis yielding interesting insights on its impact on the operational frequency determining critical path rankings.**

Keywords*— *NBTI, Back/Body Biasing, Aging, Critical Path, Reliability

I. PROBLEM STATEMENT

Reliability evaluation of digital circuits makes use of in-situ monitors that raise flags whenever the path delay exceeds a certain limit as depicted in [1,5 & **Fig. I-1**]. But the area penalty imposed by their insertion calls for an efficient critical path selection algorithm that takes into account all the variation of Process, Temperature, Voltage and Workload that influence the reliability of an IP. 28nm FDSOI technology [3] is a planar technology for use in high reliability markets like Automotive, Space and IoT leveraging the back biasing capability and the technology specific NBTI & DiR models [4] Aging models for design stage reliability estimations. Adaptive Body Bias (ABB) [5,2 & **Fig. I-1**] has shown to increase the overall performance of an IP. But, quantifying this gain at the standard cell level and its repercussions on the critical path rankings needs evaluation to enable a more accurate reliability estimation for 28nm FDSOI.

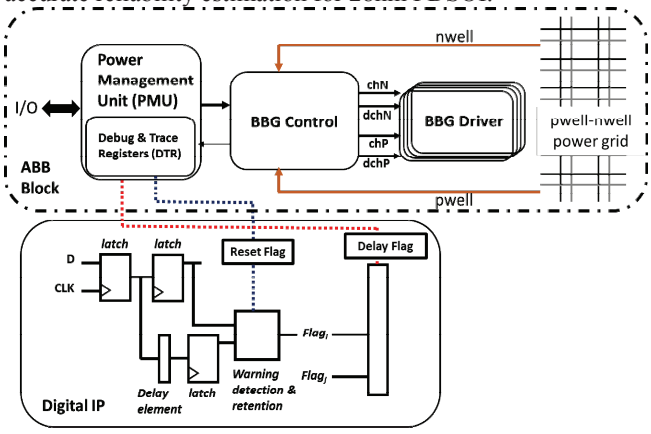

Fig I-1. Aging Mitigation with Adaptive Body Biasing (ABB)

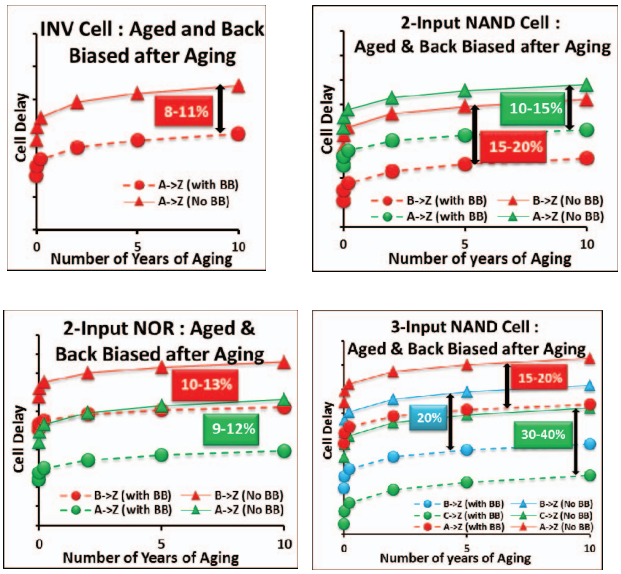

Figure I-2 Aged Standard Cell Delays with & without bias

II. HIERARCHICAL ANALYSIS

A. Standard Cell Level Analysis

The cell delay values for fresh/aged cells before and after back biasing, obtained from the SPICE level aging simulations of standard cells with input signals of 50% input signal probability are presented in **Fig. I-2**. An average of 10% gain in operational speed (or decrease in cell delay) is observed between a cell which is back biased by $\pm V_{BBmax}$ and the one which is not. From the current technology specific standard cells and their models, this back bias gain in performance is not observed to vary significantly with aging of the cells. This translates into a complete mitigation of NBTI induced aging experienced by cells for at least 5 years with back biasing at $\pm V_{BBmax}$ provided that the mission profile IP operating conditions depending on process, voltage, temperature, and workload remain constant.

B. Critical Path Level Analysis

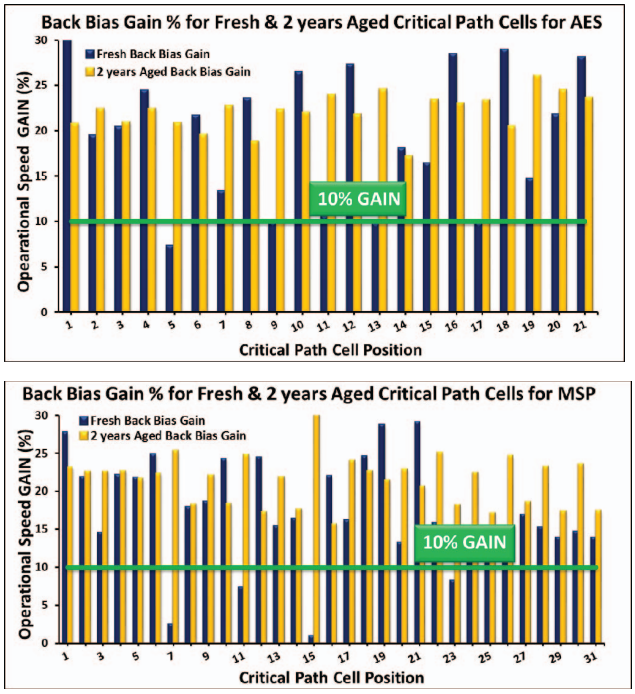

Figure II-1 Bias Gain for AES & MSP Critical Path Cells

The path and design level analysis is performed on two test cases, hardware implementation of AES (Advanced Encryption Standard) and open source MSP microcontroller [6]. The results obtained from Gate level analysis of the Critical Path (in **Fig II-1**) for both designs correlate with the results from the earlier presented cell level analysis.

C. Design Level Critical Path Analysis

Application of back biasing on the MSP design results in reordering of the criticality of the frequency determining paths, depicted in **Table 1.** for the first 10 probable critical paths for both fresh and aged design. Back biasing when applied to a 2 year aged design to compensate for NBTI degradation, changes the critical path rankings of the design.

Table 1 Path Reordering of 10 Probable Critical Paths

Fresh Path Rank (reference)	1	2	3	4	5	6	7	8	9	10
2yrs Aged Back Biased Critical Path Reordering	1	2	6	4	3	8	9	5	11	13

For design level analysis, the evaluation is restricted to 100 critical paths owing to the area overhead constraint imposed by the insertion of performance monitors. 10% gain in operational speed with back biasing of standard cells reflects into elevation of 10% new paths to higher levels of criticality for AES and which rises up to 35% for a complex MSP design with a much higher gate count (**Fig. II-2**) just after two years of aging.

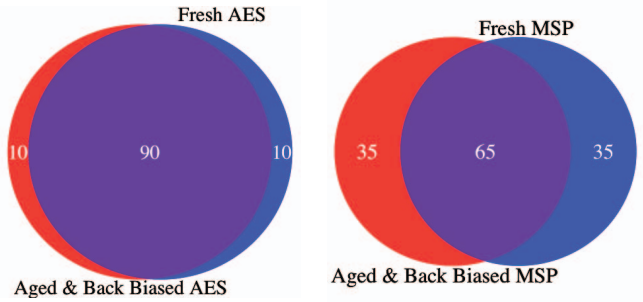

Figure II-2 Probable Critical Path Distribution between Fresh Design & Back Biasing a 2yr Aged Design

CONCLUSION

Back Biasing is an important add-on technology feature of 28nm FDSOI which helps in regulating the performance or compensating for variability of an IP without much area overhead. This paper successfully justifies the need to consider potential critical path reordering while selecting critical paths for replication or in-situ monitor insertion, which is fundamental to overall digital IP reliability assessment of FDSOI based circuits. Power penalty associated with back biasing is to be expected to achieve the expected gain.

REFERENCES

[1] Lorena et al (2016). Early system failure prediction by using aging in situ monitors: Methodology of implementation and application results, IEEE VLSI Test Symposium (VTS), 2016

[2] P.Mora et al (2015). 28nm UTBB FDSOI product reliability/performance trade-off optimization through body bias operation, IEEE International Reliability Physics Symposium (IRPS)

[3] X. Federspiel et al (2012). 28nm node bulk vs FDSOI reliability comparison, IEEE International Reliability Physics Symposium (IRPS)

[4] Huard, V et al,(2015). Technology Scaling and Reliability: Challenges and Opportunies, IEDM

[5] M. Blagojević et al (2016). A fast, flexible, positive and negative adaptive body-bias generator in 28nm FDSOI, IEEE Symposium on VLSI Circuits (VLSI-Circuits), 2016

[6] O. Girard. (2010). [Online]