Compact Modeling of Carbon Nanotube Thin Film Transistors for Flexible Circuit Design

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Abstract—Carbon nanotube thin film transistor (CNT-TFT) is a promising candidate for flexible electronics, because of its high carrier mobility and great mechanical flexibility. An accurate and trustworthy device model for CNT-TFTs, however, is still missing. In this paper, we present a SPICE-compatible compact model for CNT-TFT circuit simulation and validate the proposed model based on fabricated CNT-TFTs and Pseudo-CMOS circuits [1][2]. The proposed CNT-TFT model enables circuit designers to explore design space by adjusting device parameters, supply voltages and transistor sizes to optimize the noise margin (NM) and power-delay product (PDP), which are the key merits for larger scale CNT-TFT circuits. We further propose a design framework to effectively optimize the NM and PDP to facilitate greater automation of flexible circuit design based on CNT-TFTs.

Index Terms—Carbon nanotube, thin-film transistors, SPICE, Pseudo-CMOS, robust design, design automation.

I. INTRODUCTION

Carbon nanotube (CNT) random network is promising for high-performance flexible thin film transistors (TFTs), as shown in Fig. 1, because of its high carrier mobility $(25 \ cm^2/Vs)$, mechanical flexibility, and solution-compatible processes [3]. Recently developed CNT sorting methodologies in [4][5] enable high-purity semiconducting CNTs and dense CNT networks, which leads to a higher carrier mobility and lower operation voltages. Comparisons among different TFT technologies are shown in Table I, which indicates that CNT-TFT is promising for high-performance low-power flexible applications [6][7][8]. In addition to merits of low-cost manufacturing such as low-temperature and solution-compatible processes, CNT-TFT is recently emerging as an ideal candidate for low-cost wearables and internet of things (IoT) nodes [9].

While CNT-TFT is promising for a wide range of applications, an accurate and yet simple compact model for CNT-TFTs is still missing. Previously reported analysis for CNT-TFTs [3] only focuses on the linear region and does not reflect mobility dependency on the gate voltage and contact effect at source/drain terminals. For CNT random network, the charge transport characteristic is dominated by tube-tube junctions [3][10]. Due to the complexity of the CNT random network, it is infeasible to model all tube-tube junctions using Monte Carlo simulations [11]. In this paper, we propose a compact model based on the measurement data and provide validation results of the model with fabricated CNT-TFT devices as well as Pseudo-CMOS logic circuits. The proposed model is implemented in the Verilog-A language, and is compatible with SPICE to explore the design space for Pseudo-CMOS circuit implementations [1][2]. We plan to release this model

Device Type	Amorphous	Metal-	SAM	Polymer	Carbon
(TFT)	Si	Oxide	Organic	Organic	Nanotube
Drocoss	$\sim 250^{\circ}\mathrm{C}$	$\sim 150^{\circ}\mathrm{C}$	$\sim 100^{\circ} C$	Room	Room
Tomporatura				tempera-	tempera-
remperature				ture	ture
Process Technology	Lithography	Lithography /Roll-to- roll	Shadow mask	Ink-jet	Solution/ shadow mask/roll- to-roll
Feature Size (µm)	~ 8	$\sim 2-5$	~ 50	~ 50	$\sim 2-5$
Stable	N-type	N-type	P-type	P-type	P-type
Device Type	wype	retype	1 -type	I -type	1 -type
Supply Volt-	~ 20	~ 5	~ 2	~ 40	$\sim 1-2$
age (V)	20			10	- 1 2
Mobility (cm ² /Vs)	~ 1	~ 10	~ 0.5	~ 0.05	~ 25

TABLE I: Comparisons among different TFT technologies



Fig. 1: Flexible CNT TFT Circuits [12].

to allow designers to explore CNT-TFT based flexible circuits and evaluate their potentials. The main contributions of this paper are summarized as follows:

- Developing an accurate SPICE-compatible compact model for CNT-TFTs, which is thoroughly validated using transistor and circuit measurements
- Exploring the design space based on the developed model to analyze the noise margin (NM) and power-delay product (PDP) for flexible circuit design
- Proposing an optimization framework, which enables effective optimization of the NM and PDP for large-scale CNT-TFT flexible circuits

The rest of this paper is organized as follows: Section II provides device details and model derivations for CNT-TFTs; Section III elaborates CNT-TFT model validation against transistor and circuit measurements; Section IV analyzes CNT-TFT circuits and explores the design spaces for NM and PDP optimization; Section V draws the conclusion.

II. COMPACT MODELING OF CNT-TFT

A. CNT-TFT Properties

The cross section of the CNT-TFT is illustrated in Fig.1, where a bottom gate structure is used. The bottom gate structure enables a denser CNT network for better performance. For TFT technologies, there is only either N or P type of stable devices, as illustrated in Table I. CNT-TFTs usually exhibit P-type characteristics and the fabrication of stable N-type CNT-TFTs remains a longstanding challenge [13]. In our analysis, therefore, we focus on P-type CNT-TFTs and mono-type circuit design such as Pseudo-CMOS to accommodate material and device limitations of CNT-TFTs.



Fig. 2: Measured CNT-TFT I-V curve and mobility dependency on gate voltages.

B. Observations

To investigate the effective mobility of the CNT-TFT, a low source drain voltage ($V_S = 0V$ and $V_D = -0.5V$) is chosen to make sure that the device is in the linear region. The measured I-V curve is shown in the top part of Fig. 2. The bottom part of Fig. 2 shows the effective mobility μ_{eff} , where the p-type MOSFET model is used to perform its derivation: $\mu_{eff} = g_m L/(WC_{ox}V_{SD})$ and $g_m = \partial I_{SD}/\partial V_{SG} = \mu_{eff}C_{ox}V_{SD}W/L$, where W is the gate width, L is the gate length, C_{ox} is the gate unit capacitance, V_{SG} is the source gate voltage and V_{SD} is the source drain voltage. Notice that the polarities of voltages and currents are opposite to those used in conventional N-type analysis. From Fig. 2, we observed that the effective mobility μ_{eff} is enhanced as the V_{SG} is relative small. However, as V_{SG} becomes larger, μ_{eff} starts to degrade.

C. Analysis and Assumptions

Similar mobility dependency phenomenon has been observed in OTFT and a-Si TFT [14], and the most accepted theories are based on charge drift in the presence of taildistributed traps (TDTs) and variable range hopping (VRH) [10][15]. We therefore establish the CNT-TFT model based on TDTs and VRH theories which, to be shown in the following, can well capture the behaviors of CNT-TFTs.



Fig. 3: CNT-TFT intrinsic model with contact resistances.

1) Mobility Enhancement: Both theories indicate the field enhancement of the mobility :

$$\mu = \begin{cases} \mu_0 (V_G - V_{th})^{\gamma}, & \text{N-type TFT} \\ \mu_0 (V_{th} - V_G)^{\gamma}, & \text{P-type TFT} \end{cases}$$
(1)

, where V_{th} is the threshold voltage, γ is the field enhancement factor for mobility and μ_0 is defined as the effective mobility when $|V_G - V_{th}| = 1$, as illustrated in Fig. 2. This mobility enhancement assumption explains the increase of the effective mobility at a low V_{SG} .

2) Contact Effect: The degeneration of mobility at high V_{SG} can be explained by the contact resistances R_S and R_D at source/drain terminals, as shown in Fig. 3. These resistances result in effective source-gate voltage/source-drain voltage drops: $\tilde{V}_{SG} = V_{SG} - R_S \tilde{I}_{SD}$, $\tilde{V}_{SD} = V_{SD} - (R_S + R_D) \tilde{I}_{SD} = V_{SD} - R_C \tilde{I}_{SD}$, where $R_C = R_S + R_D$ and the current with contact effect is denoted as \tilde{I}_{SD} . The derivations are not presented here for simplicity and the contact effect can be illustrated as follows:

$$\tilde{I}_{SD} \approx \frac{WC_{ox}\mu}{L\{1 + kR_C(V_{th} + V_{SG})\}} \{(V_{th} + V_{SG}) - \frac{1}{2}V_{SD}\}V_{SD}$$
(2)

$$\frac{I_{SD}}{I_{SD}} \approx \frac{\tilde{\mu}}{\mu} = \frac{1}{1 + kR_C(V_{th} + V_{SG})}; \ k = \frac{W}{L}C_{ox}\mu \tag{3}$$

From Eq. (3), we can conclude that contact resistances lead to a mobility reduction with a factor of $1/(1+kR_C(V_{th}+V_{SG}))$ and it becomes more significant as V_{SG} increases, which explains the degeneration of the effective mobility with a high V_{SG} as shown in Fig. 2.

D. Model Derivations

We first establish the intrinsic current model based on the mobility enhancement assumption, then extend the model to capture parasitics and second order effects.

1) Intrinsic Current Model: We therefore integrate the mobility enhancement assumption Eq. (6) into the p type charge drift model Eqs. (4)-(5) to derive the intrinsic current model inspired by [14]:

$$I_{SD(x)} = Q_{CH}(x)v; \ v = u_{eff} \frac{\partial V(x)}{\partial r}$$
(4)

$$Q_{CH}(x) = WC_{ox}(V_{th} - V_G + V(x))$$
(5)

$$u_{eff} = \mu_0 (V_{th} - V_G + V(x))^{\gamma}$$
(6)

Since the current is constant in the channel [16], integrating along the channel $\int_{x=0}^{x=L} I_{SD}(x) dx$ yields:

$$I_{SD} = \frac{k}{(\gamma + 2)} \{ (V_{th} - V_{GS})^{\gamma + 2} - (V_{th} - V_{GD})^{\gamma + 2} \}$$
(7)

where k is defined as $\frac{WC_{ox}\mu_0}{L}$. Similar to MOSFET, we divide Eq. (7) into two regions: 1) linear region, and 2) saturation

region. Applying the Taylor expansion and keep the first and second order terms, we can then simplify the formula as:

$$I_{SD} \approx \begin{cases} k' \{ (V_{th} - V_{GS}) - \frac{1+\gamma}{2} V_{SD} \} V_{SD}, \ V_{DS} > V_{GT} \\ \frac{k'}{(\gamma+2)} (V_{th} - V_{GS})^2, \ V_{DS} \le V_{GT} \end{cases}$$
(8)

$$k' = k (V_{th} - V_{GS})^{\gamma}; \ V_{GT} = V_{GS} - V_{th}$$
 (9)

Notice that Eq. (8) becomes a conventional MOSFET model when $\gamma = 0$. This is because the main difference between the CNT-TFT intrinsic model, Eq. (7) and the MOSFET model is the mobility enhancement dependency on the gate voltage. This inherent connection between Eq. (7) and the MOSFET model leads to a major advantage: we can readily include second-order effects, such as channel length modulation, into Eq. (7) taking advantage of mature MOSFET theories.

2) Extending the Intrinsic Model: To further enrich the capability of the CNT-TFT intrinsic model, we incorporate the channel length modulation $1 + \lambda V_{SD}$ into Eq. (7) and the limiting function $f_{\text{lim}}(V_G, V)$ is added to provide smooth transitions between the sub-threshold region and the above-threshold region [16]:

$$I_{SD} = \frac{k}{\gamma + 2} (f(V_G, V_S)^{\gamma + 2} - f(V_G, V_D)^{\gamma + 2}) (1 + \lambda V_{SD}) \quad (10)$$

$$f_{\rm lim}(V_G, V) = SS \ln[1 + \exp(\frac{V_{th} - V_G + V}{SS})]$$
(11)

where λ is the channel length modulation factor and SS is related to the sub-threshold slope. We also summarize the simplified analytical model in Table II, which can be used to analyze CNT-TFT based circuits and provide more design intuitions.

TABLE II: Simplified Analytical Model for CNT-TFTs

	$V_{GS} \le V_{th}$	$V_{GS} > V_{th}$
$V_{DS} \le V_{GT}$	$\frac{k'}{(\gamma+2)}(V_{th} - V_{GS})^2$	$\frac{k}{(\gamma+2)} \left\{ (SS \exp(\frac{V_{th} - V_{GS}}{SS}))^{\gamma+2} \right\}$
		$-(SS\exp(\frac{V_{th}-V_{GD}}{SS}))^{\gamma+2}\}$
$V_{DS} > V_{GT}$	$k'\{(V_{th} - V_{GS})V_{SD}$	$-\frac{k'}{(\gamma+2)}(V_{th}-V_{GD})^2$
	$-\frac{1+\gamma}{2}V_{SD}^{2}$	

3) Contact Resistance and Gate Capacitance: We add two series resistances R_S and R_D to account for the contact effect as shown in Fig. 3. Two lumped capacitors C_{GS} and C_{GD} are added as well to characterize the transient behavior of the CNT-TFT circuits. Due to the large device sizes (hundreds of μm scale), two lumped capacitors are sufficient accurate to capture the transient responses of CNT-TFT circuits. Gate source/drain parasitic capacitors C_{GSO} and C_{GDO} are also included to improve the accuracy.

$$C_{GS} = C_{GCS} + C_{GSO}; \ C_{GD} = C_{GCD} + C_{GDO};$$
(12)
$$C_{CSO} = C_{GDO} = C_{or} W L_{or};$$
(13)

$$C_{GCD} = \partial Q_{CH} / \partial V_{GD} \approx \begin{cases} 1/2C_{ox}WL \text{ Linear} \\ 0 \text{ Saturation/Cutoff} \end{cases}$$
(14)

$$C_{GCS} = \partial Q_{CH} / \partial V_{GS} \approx \begin{cases} 1/2C_{ox}WL \text{ Linear} \\ 2/3C_{ox}WL \text{ Saturation} \\ 0 \text{ Cutoff} \end{cases}$$
(15)

where L_{ov} is the gate source/drain overlap. C_{GCS} and C_{GCD} are implemented as voltage controlled capacitors in Verilog-A. The final equivalent circuit model is shown in Fig. 3 and all equations can be implemented in Verilog-A for the SPICE simulation.

III. MODEL VALIDATION

In this section, we compare the SPICE CNT-TFT simulation results with measured source-drain current versus gate voltages (I-V) curves, Pseudo-CMOS inverters' voltage transfer curves (VTCs) and ring-oscillator's transient waveforms.





Fig. 4: Model validation for I - V and transconductance curves.

1) I-V Validation: We first examined the proposed model with the measured I-V and transconductance curves. Both linear and logarithmic scales are shown in Fig. 4. The model prediction well matches the device measurement reflecting both the mobility enhancement and contact resistance caused degeneration as shown in the Fig. 4. A wide range of $V_{GS} \in [-2, 0]V$ and $V_{DS} \in [-4, 0]V$, covering sub-threshold, linear and saturation, are investigated, as illustrated in Fig. 5. The excellent match between model predictions and measurement data further confirm the validity of the above-mentioned model derivations and assumptions.



Fig. 5: Model validation for I - V curves.

2) Parameter Extraction: We extract model parameters out of 52 fabricated CNT-TFTs, where a Gaussian distribution is assumed for process variations. All extracted parameters are summarized in Table III, where the mean value μ and standard deviation σ are provided.

TABLE III: Parameters extracted from 52 fabricated CNT-TFTs

Model Parameter	Notation	$[\mu, \sigma]$ Unit
Channel Length	L	[25, -] um
Channel Width	W	[125, -] um
Gate S/D Overlap	L_{ov}	[10, -] <i>um</i>
Gate Unit Capacitance	C_{ox}	$[200, -] nF/cm^2$
Threshold voltage	V_{th}	[0.5, 0.102] V
Sub-threshold Swing	SS	[0.28, 0.0388] V/dec
Effective Mobility	μ_0	$[25.69, 0.19] \ cm^2/Vs$
Contact Resistance	R_C	[1531, 291] Ω
Channel Length Modulation	λ	$[0.064, 0.0185] V^{-1}$
Factor of Gate Dependent mobility	γ	[0.20, 0.116] (-)

B. Circuits Validation

Beside single devices, the model must be able to predict the circuit level behaviors with a sufficient accuracy. We therefore

compare the SPICE simulation results with the measured voltage transfer curves (VTC) and ring-oscillator's waveform.

1) Introduction to Pseudo-CMOS: Pseudo-CMOS is a design style proposed to address design challenges of monotype TFT circuit design [1][2], which has been proven a robust design style and has been widely used for flexible digital, analog, and power circuits [17][18][19]. Compared to conventional mono-type digital design styles, such as the diode-load or resistive-load designs, Pseudo-CMOS offers better noise margin and provides post-fabrication tunability at the cost of an additional power rail V_{SS} . There are two topologies of Pseudo-CMOS: depletion (Pseudo-D) type and enhancement (Pseudo-E) type. We focus on the Pseudo-D type since it is more suitable for our depletion devices [2]. A Pseudo-D inverter consists of three power rails, V_{DD} , V_{SS} and GND, and four transistors M_{1-4} , as shown in Fig. 6.



2) VTC Validation: A typical voltage transfer curve (VTC) of an inverter is shown in Fig. 7 and here we focus on V_{SP} , $V_{I/OH}$ and $V_{I/OL}$, which determine the noise margin (NM) for digital circuits. In Fig. 8 (Left), we compare the SPICE simulated voltage transfer curves (VTCs) and small signal gain with actual measurements, where solid lines are SPICE simulations and dots are measurements. Both VTC and small signal gain simulations match closely with the circuit measurements over a wide range of supply voltages V_{DD} , from 0.8V to 1.6V. Despite minor discrepancies in low supply voltages, the proposed model accurately predicts the V_{SP} , $V_{I/OH}$ and $V_{I/OL}$. Furthermore, Monte Carlo simulation is performed to illustrate various VTCs under process variations, based on extracted device parameters as shown in Table III. From Fig. 8 (Right), we can see that the SPICE simulation can accurately predict the variation of the V_{SP} of the VTCs, where bold lines are simulation results using the mean values in Table III.

3) Transient Validation: We validated our transient model using the Pseudo-D based five-stage ring-oscillator's measured waveform. As shown in Fig. (9), the SPICE simulation result well captures the oscillation frequency and the amplitude compared with the measurement data.

In summary, the results of both DC and transient simulations indicate that the proposed SPICE CNT-TFT model can accurately predict both device and circuit level behaviors.

IV. NOISE MARGIN, POWER-DELAY ANALYSIS AND DESIGN EXPLORATION

To further enable large-scale flexible circuit design, we thoroughly analyze the key merits for digital circuits, includ-



Fig. 8: Left: Measured and simulated VTCs and small signal gains; Right: 26 measured VTCs and Monte Carlo simulation.



ing NM, power and delay, and develop a systematic design methodology to facilitate design automation for CNT-TFT flexible circuits. In this section, we first analyze how device parameters, transistor sizes and supply voltages affect NM and PDP for Pseudo-D digital circuits. Based on insights derived from this analysis, we propose a design framework to optimize the NM and PDP.

A. Noise Margin Analysis

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A Pseudo-D inverter consists of two stages, as illustrated in Fig. 6. Since the first stage dominates the overall inverter VTC, for simplicity our NM analysis focuses on the first stage.

a) Derivation: A typical VTC of an inverter is shown in Fig. 7 and the NM is defined as $NM = \min(V_{OH} - V_{IH}, V_{IL} - V_{OL})$. We use the following approximations to simply the derivations: 1) $V_{OH} \approx V_{DD}$, $V_{OL} \approx GND$; 2) $V_{IH/L} \approx V_{SP} \pm \frac{V_{DD}}{2Gain} \approx V_{SP}$. Such simplifications are reasonable resulting in negligible errors. As shown in Fig. 8, the VTCs are almost rail to rail and the gains are very high (≥ 50) even with a V_{DD} at 0.8V, which leads to a negligible $\frac{V_{DD}}{2Gain}$. Therefor, the simplified analytical NM model can be expressed as:

$$VM = \min(V_{OH} - V_{IH}, V_{IL} - V_{OL})$$

$$\approx \min(V_{DD} - V_{SP}, V_{SP})$$
(16)

$$V_{SP} = V_{DD} + V_{th} (1 - \gamma^{+2} \sqrt{\alpha}), \ \alpha = W_2 / W_1.$$
(17)

$$(V_{DD} - V_{SS})/2 \ge^{\gamma+2} \sqrt{\alpha} V_{th}; \tag{18}$$

where $\alpha = W_2/W_1$ is the transistor size ratio of M_2/M_1 and V_{SP} is derived through the current equivalent at the switching point using the saturation model in Table II. Eq. (18) ensures that $M_{1/2}$ are in the saturation region at V_{SP} . Compared to the mean value of 26 measured VTCs, the analytical NM model can predict the NM for Pseudo-D inverters within an error $\leq 6.25\% V_{DD}$ even at a low supply voltage $V_{DD} = 0.8V$.



b) Analysis: In Figs. 11 and 12, we analyze the relationship among NM, transistor sizes, V_{th} and supply voltages. The simulation results show that: 1) properly adjusting transistor sizes can effectively improve the NM; 2) an optimal ratio α_{opt} to assure the maximum NM can be accurately predicted by Eq. (19) which is determined by the ratio of V_{DD}/V_{th} ; 3) the maximum achievable NM is slightly less than $V_{DD}/2$ due to the imperfect $V_{OL/H}$. To ensure $V_{OL} \approx 0$ and $V_{OH} \approx V_{DD}$, the constraints for V_{DD} and V_{SS} are given in Eq. (20). Simulation results further confirm our analysis results, where $V_{DD} - V_{OH} \le 0.05V$ and $V_{OL} \le 0.05V$ with Eq. (20) being satisfied.

$$\alpha_{opt} = (1 + \frac{V_{DD}}{2V_{th}})^{\gamma+2}$$
(19)

$$V_{DD} - V_{OH} \approx 0 \\ V_{OL} \approx 0 \\ \} \Leftrightarrow \begin{cases} V_{DD} \ge 2V_{th} \\ -V_{SS} \ge 2V_{th} \end{cases}$$
(20)

B. Power and Delay (P&D) Analysis

In this section, we analyze the trade-offs among power, delay and NM for Pseudo-D circuits [20]. According to [2], we use the following default transistor sizes: $W_1 = W_{min} =$ $5\mu m$, $W_2 = W_3 = W_4 = 15\mu m$ in the analysis. And, we define t_{p0} as the propagation delay of a Pseudo-D inverter with these default sizes.

a) Power Analysis: For the total power P_{tot} , it consists of two parts: static power P_{stat} and dynamic power P_{dyn} . We ignore the direct path power dissipation during switching P_{dp} , which is negligible comparing to P_{stat} and P_{dyn} .

$$P_{tot} \approx P_{stat} + P_{dyn}; \ k_i = \frac{W_i C_{ox} \mu_0}{L}$$
 (21)
Output High

$$P_{stat} \approx \frac{\overline{D_H}}{2} V_{th}^{\gamma+2} \{ k_2 (V_{DD} - V_{SS}) + k_4 V_{DD} \}$$
Output Low
(22)

$$+ \underbrace{\frac{D_L}{2} V_{th}^{\gamma+2} \{k_1(V_{DD} - V_{SS}) + k_3 V_{DD}\}}_{Stage1}}_{P_{dyn} \approx f\{\underbrace{C_{L,1}(V_{DD} - V_{SS})^2}_{Stage1} + \underbrace{C_{L,2}(V_{DD})^2}_{C_{L,2}(V_{DD})^2}\}}$$
(23)

where f is the frequency, $D_{L/H} \approx 1/2$ is the fraction of the duration when output is low/high in each period and $C_{L,1/2}$ is the equivalent load capacitance at node V_{IM}/V_{OUT} , as indicated in Fig. 10. To improve accuracy, Miller effects are incorporated as well:

$$C_{L,1} = \overbrace{2C_{GDO,1}}^{\text{Miller Effect}} + C_{GDO,2} + C_{G,4}; C_{L,2} = \overbrace{2C_{GDO,3}}^{\text{Miller Effect}} + C_{G,1} + C_{G,3}$$

$$(24)$$

$$C_G \approx C_{GSO} + C_{GDO} + 2/3C_{ox}WL$$

$$(25)$$

Since CNT-TFTs are in the depletion model, the leakage current $I_{leak} \propto V_{th}^{\gamma+2}$ is determined by V_{th} , which dominates the static power. The dynamic power is a function of the frequency, supply voltage and total capacitance [21].

b) Delay Analysis: For the propagation delay t_p , we use the equivalent RC approximation [20]:

$$t_p = \frac{0.69}{2} \{ \overbrace{C_{L,1}(R_{eq,1} + R_{eq,2})}^{Stage1} + \overbrace{C_{L,2}(R_{eq,3} + R_{eq,4})}^{Stage2} \}$$
(26)

$$R_{eq,1} \approx \frac{3}{4k_1} \frac{V_{DD} - V_{SS}}{(V_{DD} + V_{th})^{2+\gamma}}; \ R_{eq,2} \approx \frac{3}{4k_2} \frac{V_{DD}}{V_{th}^{\gamma+2}}$$
(27)

By setting the k_1 to $k_{3/4}$ and $V_{SS} = 0$ in $R_{eq,M1}$, we can get $R_{eq,M3/4}$. Notice that $R_{eq,M1/3/4}$ decreases as the supply voltage V_{DD} increases; however, $R_{eq,M2}$ behaves opposite. This is because zero- V_{gs} connection will limit the current to a small value $(I_{M,2} = k_2 V_{th}^{\gamma+2})$ during switching, leading to a large equivalent resistance. This also confirms the validity of ignoring P_{dp} .



Fig. 15: W_2 vs. PDP and NM.

c) Design Space Exploration: First, we investigate how supply voltages affect the delay and power. We observed that simply increase the V_{DD} cannot improve the propagation delay as shown in Fig. 13, which is counter-intuitive to conventional wisdom. This is because $R_{eq,M2}$ increases as the supply voltage and $R_{eq,M2}$ is much larger (~ 10X) than $R_{eq,M1/3/4}$, as shown in Fig. 14, preventing from further improving of the stage delay. As a result, the delay increases as V_{DD} becomes higher, due to the dominant $R_{eq,M2}$. This phenomenon indicates that Pseudo-D is more suitable for low voltage design, which can benefit from a better PDP. For V_{SS} , a large negative V_{SS} will increase the delay and power; however, it leads to a better NM as illustrated in Fig. 15.

After identifying $R_{eq,M2}$ as a critical part for power and delay, we analyze the impact of W_2 on power, delay and NM. We observed that W_2 can be used to explore the trade-off between power and delay as show in in Fig. 16. A larger W_2 can lead to a smaller delay but higher power consumption. Furthermore, W_2 will also affect the NM, as shown in Fig. 15, and the optimal values of W_2 for NM and PDP are different. Thus, trade-off between NM and PDP should be evaluated during the circuit design stage.

C. NM and PDP Optimization

Based on the analysis in Section IV-B, we conclude that supply voltages and transistor sizes influence the *PDP* significantly for Pseudo-D circuits. Furthermore, to assure a good NM, transistor sizes and supply voltages have to satisfy certain constraints stated in Section IV-A. Hence, we can formulate a constrained optimization problem to optimize the PDP while meeting the NM requirement for Pseudo-D circuits:

minimize
$$PDP(W_{1-4}, V_{SS})$$
 given NM_0, V_{th}, V_{DD}
subject to $\min(V_{DD} - V_{SP}, V_{SP}) \ge NM_0 \Leftrightarrow$ Eq. (16)
 $(V_{DD} - V_{SS})/2 \ge^{\gamma+2} \sqrt{\alpha} V_{th}; \Leftrightarrow$ Eq. (18)
 $V_{DD} - V_{OH} \le \delta, V_{OL} \le \delta; \Leftrightarrow$ Eq. (20)
 $W_i \ge W_{min} = 5 \ \mu m$

The above optimization determines transistor sizes and V_{SS} given specific NM_0 , V_{th} and V_{DD} . Using Lagrange multipliers and gradient decent, we can solve the above constrained optimization and optimized results for different NM_0 are summarized in Table IV. Compared to the default design in Fig. 15, the optimized results show $\sim 3X$ improvement for PDP with the same NM = 0.3 V and supply voltages. Considering V_{th} and V_{DD} as design parameters, we can achieve $\sim 6X$ improvement with device and circuit cooptimization. Although our exemplar formulation above uses the PDP as the optimization target, it can be easily modified for power or delay optimization. In summary, this proposed design framework can effectively optimize the PDP (or just power or delay) while satisfying the NM specification.

TABLE IV: Pseudo-D Optimization $V_{DD} = 2 V$, $V_{th} = 0.5 V$, $\delta = 0.05$

NM_0	W_1	W_2	W_3	W_4	V_{SS}	PDP
0.3V	$5.0 \mu m$	$19.4 \mu m$	$5.0\mu m$	$5.0 \mu m$	-1.00V	1.97 pJ
0.5V	$5.0 \mu m$	$27.4 \mu m$	$5.0 \mu m$	$5.0 \mu m$	-0.97V	2.03pJ
0.8V	$5.0\mu m$	$44.0\mu m$	$5.2 \mu m$	$5.4 \mu m$	-0.76V	2.24pJ

V. CONCLUSION

In this paper, we present a SPICE-compatible CNT-TFT model to support CNT-TFT flexible circuit design. The model has been derived and validated based on 52 fabricated CNT-TFTs and 26 Pseudo-D inverters. Based on the proposed model, we further analyze how device parameters, supply voltages and transistor sizes affect the NM and PDP of Pseudo-D circuits. Finally, a constrained optimization procedure is proposed to optimize the PDP while meeting the NM specification. The proposed optimization methodology can be easily extended to more complicated logic gates and library cells, which can further enable greater automation of large-scale flexible circuit design based on CNT TFTs.

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