Enhanced Analog and RF IC Sizing Methodology using PCA and NSGA-II Optimization Kernel

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Abstract—**State-of-the-art design of analog and radio frequency integrated circuits is often accomplished using sizing optimization. In this paper, an innovative combination of principal component analysis (PCA) and evolutionary computation is used to increase the optimizer's efficiency. The adopted NSGA-II optimization kernel is improved by applying the genetic operators of mutation and crossover on a transformed design-space, obtained from the latest set of solutions (the parents) using PCA. By applying crossover and mutation on variables that are projections of the principal components, the optimization moves more effectively, finding solutions with better performances, in the same amount of time, than the standard NSGA-II optimization kernel. The proposed method was validated in the optimization of two widely used analog circuits, an amplifier and a voltage controlled oscillator, reaching wider solutions sets, and in some cases, solutions sets that can be almost 3 times better in terms of hypervolume.**

Keywords—Electronic Design Automation, Sizing Optimization, Analog and Radio-Frequency Integrated Circuits, Multi-Objective Evolutionary Optimization, Principal Component Analysis.

I. Introduction

Albeit modern integrated circuits (IC) being mostly implemented using digital circuitry, analog and radio-frequency (RF) circuits are still the base for most interfaces and transceivers, and, therefore, are subject to continuous research efforts that push the boundaries of their performance and power efficiency in state-of-the-art applications and integration technologies. However, unlike digital circuits where most of design stages are automated using established tools and methodologies, the shortage of computer-aided-design (CAD) tools for electronic design automation (EDA) of analog and RF IC blocks is the major contributor to their bulky development cycles, leading to long, iterative and error-prone designer's intervention along the entire course of the design flow [1].

This paper focuses on improving the efficiency of automated circuit sizing, one of the major design task in analog and RF ICs, where the sizes of the circuit's devices are dimensioned to achieve the required performance figures. Optimization-based techniques using the circuit simulator to ensure accurate performance evaluation are the most common approach to automate this design task, with several commercially available solutions, e.g., Cadence's Virtuoso GXL [2] or MunEDA's DNO/GNO [3]. In this context, this paper describes an optimization method that improves the effectiveness of the optimization of analog and RF IC sizing. An innovative combination of principal component analysis (PCA) [4] and evolutionary computation, more specifically the non-dominated sorting genetic algorithm II (NSGA-II) [5], is used in this work to improve the optimization process efficiency.

The optimization kernel's improved performance is achieved by applying the genetic operators of mutation and crossover on a transformed design-space, obtained from the latest set of solutions (the parents) using PCA. By applying crossover and mutation on a variable encoding where the search directions are sorted by the variance found in the parents, the optimization moves more effectively in a twofold: (1) it can explore directions with higher variance (the controls for the current specifications); and (2), it can hold the low variance directions (keeping the invariables of the design) among parents. As a result, the optimization finds solutions with better performances in the same amount of time than standard optimization kernel.

The underline idea of why the transformed space allows the optimizer to find better solutions faster relates to the fact that the design parameters available to the designer are actually mostly related to the device's physical design (width, length, diameter, area, perimeter, etc.) than to the electrical behaviour (gm, inductance, capacitance, etc.). Therefore, some can be redundant for a given circuit and set of specifications. When the optimizer operates on a transformed space that capture those redundancies, its performance is increased for the particular problem.

The paper is organized as follows. In Section II, a brief state-of-the-art review on the optimization techniques applied to automate the sizing of analog and RF ICs is presented, some feature reduction techniques previously applied in automatic learning are overviewed, and, the innovative contributions of this work discussed. In Section III, the proposed multi-objective sizing optimization is described, and in Section IV, it is compared to standard NSGA-II in the sizing optimization of an amplifier and a voltage controlled oscillator, and, finally, in Section V, the conclusions are addressed.

II. Related Work and Contributions

As the optimization-based methods cement as the correct approach to automate analog and RF IC sizing, the variety of tools and techniques proposed in the last years covering several other aspects intrinsically related with sizing, e.g., yield, aging or layout parasitics, show that design automation tools are

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evolving. Research community has progressively focused on improving the efficiency and accuracy of these methodologies, with some of the most remarkable methods focusing on improving the reliability and robustness of the ICs [6][7], and others on accounting for layout inducted parasitics during the sizing optimization loop [8][9], for example. With some addressing general analog and RF circuit design [6], and others addressing sub-classes of circuits and/or components, where RF circuits, and more specifically, RF integrated passive devices deserve a special attention [9][10].

Evolutionary optimization and, particularly, the NSGA-II kernel, is widely used in many fields of application, including EDA, showing excellent performance and robustness [11]. NSGA-II is an evolutionary optimization scheme that operates over a set of candidate solutions to the optimization problem (also referred as population), and simulates natural evolution. It relies on bio-inspired operators such as mating, crossover, mutation and environmental pressure to explore the design space, and, ultimately find better solutions, as summarized in Fig 1.

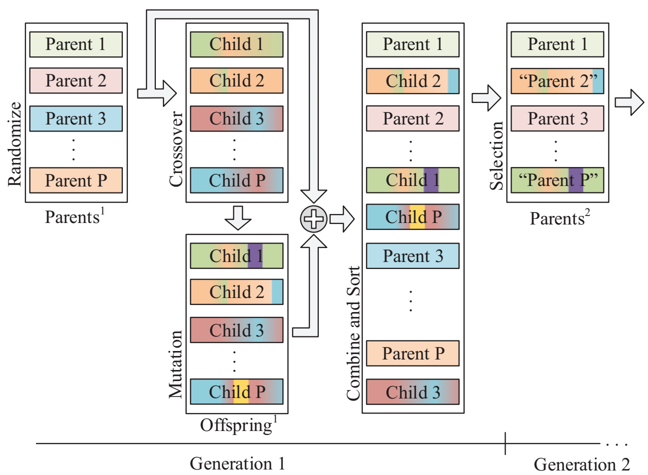

Fig. 1. Evolutionary optimization overview: NSGA-II.

The optimization starts from a set of randomly generated individuals. It is an iterative process, and, in each iteration (also referred as a generation) new solution vectors (i.e., the children or offspring) are obtained from the current population (i.e., the parents) by the application of the operators of mating, crossover and mutation. Mating is the process of selecting a pair of parents for breeding, crossover combines randomly selected sets of information from each parent to produce new children, and, mutation applies a random change in the children's genetic information. Afterwards, the offspring's fitness, which measures the quality of the solution, is evaluated. In the context of analog and RF IC sizing, the fitness evaluation is done using circuit simulation to obtain the circuits' performance. Offspring and parents are then ranked together using non-dominated sorting and crowding distance. The non-dominated-sorting procedures ranks the solutions by their Pareto dominance, which defines that solution A is not dominated by solution B if $\exists m\colon f_m(A) < f_m(B)$, where $f_m(X)$ is one of the objective functions i.e., non-dominated or Pareto solutions are better than other solutions in at least one objective, and, crowding distance metric that provides a density measure. Finally, environmental pressure is applied, discarding the less fit.

As the design parameters for the devices provided in the PDK by the foundries are in general for all kinds of circuits and specifications, it can be expected some redundancy or correlation of the design variables for a specific application and target specifications. Therefore, feature reduction techniques commonly used in data science, are a powerful tool to exploit this fact, drastically increasing the optimization performance [12]. The simplest and more commonly used dimensionality reduction technique is PCA, which finds a linear orthogonal projection for the data that captures variance maximally. In other works, the method was originally to assist decision makers in the visualization of the design variables [13][14], and more recently, has been integrated in optimizers to reduce the number of objectives considered [15][16]. Linear Discriminant Analysis [17] and Proper orthogonal decomposition [18] or Multidimensional scaling [19] also aim at finding a low- dimensional representation of the data, and like PCA, also work better for datasets containing linearly correlated variables.

In this work PCA is considered. PCA is commonly used as a dimensionality-reduction technique to underline variation, and, bring out patterns and correlation between variables in data, as it is often useful to represent data in terms of its principal components (PC) rather than on its original axis. In short, PCA is based on a linear transformation of the data to an orthonormal base that maximizes the variance of each dimension. The base is computed from the eigenvectors of the covariance matrix of the centered data. Where the variance represented in the direction of each eigenvector is given by its corresponding eigenvalue. Dimensionality reduction is achieved by truncating the components associated to less variance. Algorithm 1 summarizes the PCA procedure for dimensionality reduction.

Algorithm 1 PCA dimensionality reduction procedure

input: X[P][N] *//data*
  P *//number of samples*
  N *//sample size*
  K //number of principal components to retain
output: Y[P][K]

#define $B := X - \mu$ //centering data
#define $S := \dfrac{1}{P-1} B^T B$ *//co-variance matrix*
#define $[V, \Lambda]$:= eigenanalysis($B^T B$) // $B^T B = V \Lambda V^T$,
  // where V is an unitary matrix with the orthonormal eigenvectors as
  // columns and Λ is the diag. matrix with the corresponding eigenvalues
  sort-columns(V, "descending order" of d)
  truncate(V, K)
  return Y[P][K]:= BV

Where X is the data matrix formed by P samples of N-dimensional data, μ the estimator for the mean of the data. Fig. 2 illustrates the several PCA steps in a simple 2D dataset generated by a 2D multivariate normal distribution. The data is first centered by removing the mean (Fig. 2 (b)), and the eigenvectors and eigenvalues of the variance-covariance matrix S are computed, the first provides the principal directions, whereas the second provides the variance associated with that direction (Fig. 2 (b)). Therefore, by sorting the eigenvectors (columns of V) by the order of their corresponding eigenvalue, the transformation matrix from the original space to the principal components of Fig. 2 (c) is obtained. Dimensionality-reduction is obtained be removing the columns of V, i.e., ignoring the components corresponding to directions of fewer or no variance (Fig. 2 (d)).

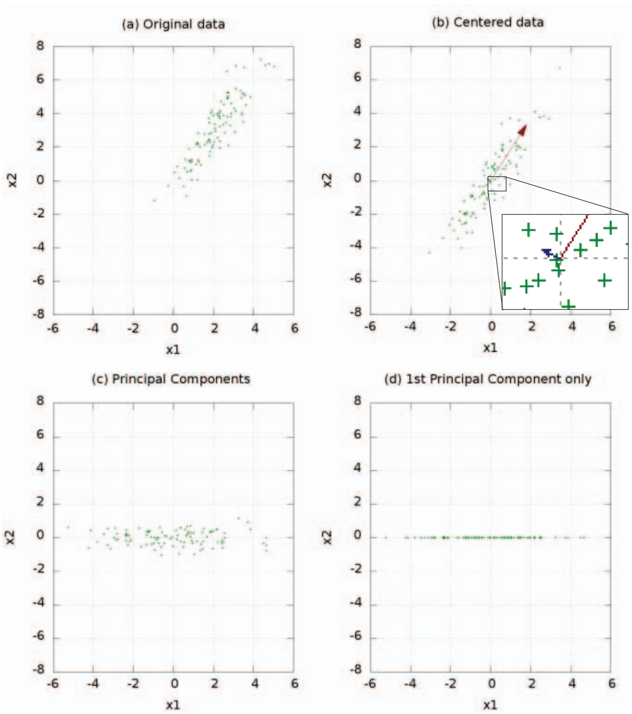

Fig. 2. PCA illustration. (a) Original data, (b) Centered data; (c) Principal components. (d) Data using only the principal component.

To conclude, the major contributions of this work to the state-of-the-art of the field are: 1) a novel formulation for multi-objective sizing optimization that combines PCA in the genetic encoding of a NSGA-II kernel; 2) exploit the redundancy of design parameters to reduce the total number of loop-iterations required. As simulation-based sizing is the most widely accepted approach, the savings in terms of computational effort are immense, especially for CPU-intensive analysis, e.g., transient or steady-state; 3) integrate both variance analysis and feature reduction with the necessity of having all the original design variables available, as they are mandatory for simulation-based performance evaluation; 4) the generality of the developed EDA methodology is proved in the optimization of two widely use and widely different types of circuits, i.e., analog amplifiers and RF voltage-controlled oscillators.

III. Multi-Objective Sizing Optimization on a Localy Tranformed Space

As introduced, in an optimization-based sizing, the kernel finds a set of S sizing solutions, each, defining the design variables (i.e., devices' widths, lengths, number of fingers or inductors' widths, number of turns, etc.). The kernel solves the constrained multi-objective problem defined in (1), where x is the vector of N design variables, $g(x)$ the J constraint functions and $f(x)$ the M objective functions, where the mapping from IC design specifications to this formulation is done according to the definitions in [6].

$$\begin{aligned} &\text{find } x \text{ that minimize } f_m(x) && m = 1,2,\ldots M \\ &\text{subject to } g_j(x) \geq 0 && j = 1,2,\ldots J \\ &x_i^L \leq x_i \leq x_i^U && i = 1,2,\ldots N \end{aligned} \tag{1}$$

To implement the system, a genetic representation of the solution domain, i.e., the genotype and phenotype of the solutions, must be defined. In analog and RF IC sizing the common approach is to use the devices' sizes to encode genotype, as they define the design space and are suitable for the parameterizations needed for the circuit simulator, which is later used to obtain the circuits' "traits", i.e., the phenotype. However, this encoding of the solution space does not exploit any of the relationships from the devices' parameters that are derived from their physical implementation when mapped to the electrical properties, e.g., *gm*, capacitance, inductance, etc. Neither it explores how some devices' parameters are more relevant towards some performances figures only, as designers tend to do manually. Moreover, while it ensures that all points in the feasible space can be represented, it usually define a search space that is mostly unfeasible.

Therefore, the proposed approach, schematized in Fig. 3, uses PCA on the parents at each generation, before generating the offspring with the genetic operators of crossover and

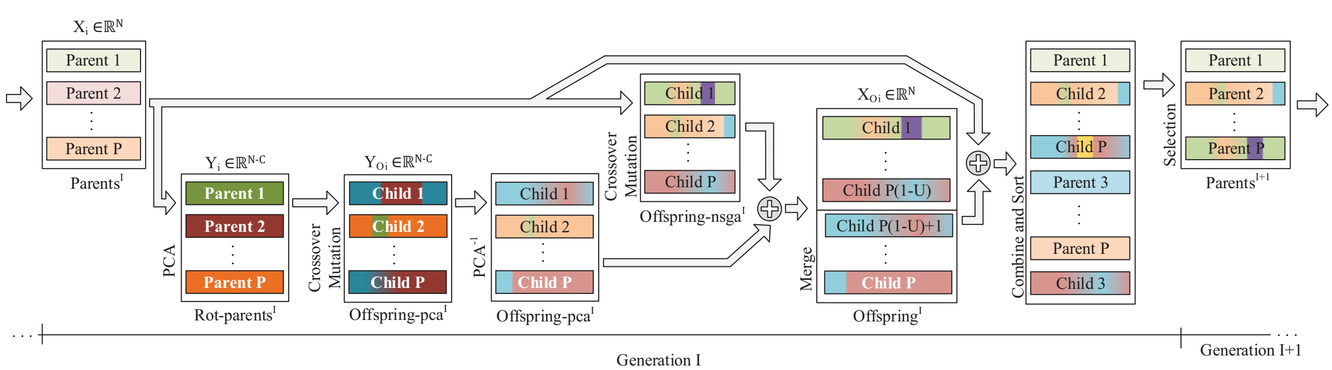

Fig. 3. Overview of the proposed NSGA-II based optimization.

mutation. These are now applied over the principal components, instead of, on the circuit's parameters. This way, the optimizer can take advantage of the powerful insights brought by PCA to produce an encoding that emphasizes both the directions of higher variability, to help the optimizer explore the solution space faster, and, the directions of invariability, helping the optimizer to hold the problem's invariants and consequently increasing the feasibility rate of offspring after crossover. The produced offspring is then transformed back to the original design space, with all the parameters required for the accurate circuit simulation.

The parents data matrix, X, is a $P \times N$ matrix with the rows being each parent design variables. In addition to transform the input data to have zero empirical mean, due to the wide ranges of analog and RF IC design variables, it is essential for the algorithm to execute properly that the all design variables are scaled to the same ranges. If the data is not normalized, then, variables which account values of a lower magnitude compared to other variables will not carry any weight on the process of finding the principal directions. Therefore, the normalized data matrix B from Algorithm 1 is redefined according to (2). Where *min*() and *max*() of a matrix ($n\times m$) return a row-vector ($1\times m$), with the minimum and maximum value of each of the matrix's columns respectively, and $\boldsymbol{e} = (1,\ldots,1)^T$ a column-vector ($n\times1$) filled with ones.

$$B = X' - \mu(X')$$
$$\text{with} \quad X' = \big(X - e\min(X)\big)R^{-1} \tag{2}$$
$$\text{and} \quad R = diag\big(\max(X) - \min(X)\big)^{-1}$$

To avoid divisions by zero, if the range of some variable i is zero, the ranges defined in the original optimization, x_i^L and x_i^U are considered. The eigenvalues and eigenvectors are obtained as in Algorithm 1, and, the parents transformed to the PC space also as in Algorithm 1. As the simulated binary crossover [20] and polynomial mutation [21] operators require variable ranges to operate, the range of the variables in the transformed space is determined L^1-norm of the corresponding base vector according to (3).

$$y_i^U = \frac{1}{2}\left|v_i\right|_1 \tag{3}$$
$$y^L = -y^U$$

Because the matrix V, the eigenvectors of the variance-covariance matrix is obtained from the singular value decomposition (SVD) of B, it is unitary and real, the inverse transformation is obtaining simply by transposing V. Therefore, the transformation of the offspring from the transformed space to the original space is given by (2), where Y_O, is the $P \times K$ matrix with each row represent a children in the PC space, and X_O, is the $P \times N$ matrix of the offspring in the original space.

$$X_O = \big(Y_O V^T + \mu(X')\big)R + e\min(X) \tag{4}$$

The proposed scheme to merge the proposed PCA transformation with NSGA-II is summarized in Algorithm 2, and is defined with 2 parameters: U, the PCA use rate U, and C, the number of removed components.

Algorithm 2 NSGA-II with PCA Encoding Procedure

```
input: P //population size
       G //number of generations
       C //removed components
       U //PCA use rate
       x^L, x^U //up and lower bounds for the variables
output: List<sizing> parents
1.  #define List<sizing> parents := New P random sizing solutions
2.  generation:= 0
3.  while generation < G
4.    #define X[P][N] := listToMatrix (parents)
5.    #define X'[P][N] := normalize (X) // eq. (2)
6.    #define [Y[P][N-C],V[N][N-C]] := PCA(X')
7.    #define [y^L, y^U] := ranges(V) // eq. (3)
8.    #define List<sizing> rot-parents := matrixToList(Y)
9.    #define List<sizing> offspring-nsga := genetic-operators(parents, x^L, x^U)
10.   #define List<sizing> offspring-pca := genetic-operators(rot-parents,
                                                            y^L, y^U)
      //transform back to the design space
11.   #define Y_O[P][N-C] := listToMatrix(offspring-pca)
12.   #define X_O[P][N] := reconstruct (Y_O) //eq.(4)
13.   offspring-pca := matrixToList(X_O)
      //merge the population randomly selecting (in average) U*P
      // elements from Offspring-pca and (1-U)*P from Offspring-nsga
14.   #define List<sizing> offspring := merge(U, offspring-pca,
                                              offspring-nsga)
15.   offspring = Evaluate(offspring) // using the circuit simulator
      // Non-Dominated-Sorting and Crowding-Distance-Selection
16.   parents := Selection(Parents & Offspring)
17.   generation++
18. end while
```

IV. Test Cases

The proposed method was implemented and used, as proof of concept, in the optimization of the single stage amplifier with gain enhancement using voltage combiners proposed in [22] and the LC-voltage controlled oscillator used in [23].

A. Optimization of the Amplifier

The single stage amplifier with gain enhancement using voltage combiners (SSAMP), whose schematic is shown in Fig. 4., loaded with a 6pF capacitor was optimized to both maximize the Figure-of-Merit (FOM) and DC Gain (GDC) in a 3.3V 130 nm process and circuit simulations done with ELDO. The design variables and corresponding ranges are shown in Table II, and, the detailed target specifications are presented in Table III.

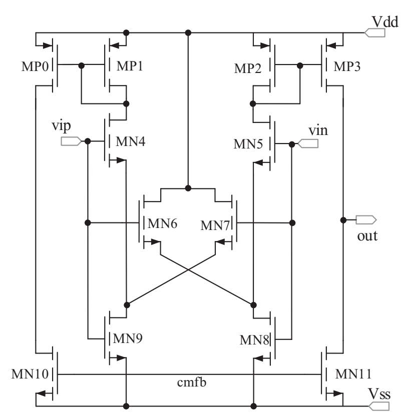

Fig. 4. Single stage amplifier with gain enhancement using voltage combiners' circuits schematic.

TABLE II. SSAMP VARIABLES AND RANGES

Variable (Unit)	Min.	Grid	Max.
l0, l1, l4, l6, l8, l10 [nm]	340	10	1000
w0 w1 w4 w6 w8 w10 [μm]	1	0.1	100
nf0, nf1, nf4, nf6, nf8, nf10	1	2	8

The variables l0, w0, and nf0 are the length, width and number of fingers of MP0 and MP3; l1, w1, and nf1 of MP1 and MP2; l4, w4 and nf4 of MN4 and MN5; l6, w6 and nf6 of MN6 and MN7; l8, w8, and nf8 of MN8 and MN9; l10 w10 and nf10 of MN10 and MN11.

TABLE III. SSAMP SPECIFICATIONS

	Measure	Target	Units	Description
Objectives	GDC	Max.	dB	Low-Frequency Gain
	FOM	Max.	MHz.pF/mA	$FOM = \frac{Gbw \times C_{Load}}{Idd}$
Constraints	Idd	≤ 350	μA	Current Consumption
	GDC	≥ 50	dB	Low-Frequency Gain
	GBW	≥ 30	MHz	Unity Gain Frequency
	PM	≥ 60	°	Phase Margin
	FOM	≥ 1000	MHz.pF/mA	$FOM = \frac{Gbw \times C_{Load}}{Idd}$
	OV[1]	≥ 50	mV	Overdrive Voltages (V_{GS}-V_{TH})[3]
	OV[2]	≥ 100	mV	Overdrive Voltages (V_{GS}-V_{TH})[3]
	D[1,2]	≥ 50	mV	Saturation Margin of the PMOS Device (V_{DS}-V_{DSat})[3]

[1] Applies to: MP0, MP1, MP2 and MP3; [2] Applies to: MN4, MN5, MN6, MN7, MN8, MN9, MN10 and MN11; [3] For PMOS devices the overdrive is Vt – Vgs and delta is Vdsat – Vds

To study the impact those parameters in the optimization results, 10 runs with each parameter set were executed with a population of 64 elements and 100 generations. The execution time of the each optimization of the amplifier is around 2 minutes. Table IV show the average hyper-volume (HV) improvement w.r.t. to standard NSGA-II, and in Fig. 5 the Pareto fronts for NSGA-II and the ones obtained with the best parameter sets are plotted.

TABLE IV. HV RATIO[a] FOR THE SSAMP AS A FUNCTION OF THE PCA USE RATE (U) AND THE NUMBER OF REMOVED COMPONENTS (C)

U \ C	0	2	5	8	11
0.25	2.16	1.24	1.04	1,43	**2.26**
0.50	**2.91**[b]	0.70	1.61	1.87	1.84
0.75	**2.79**[b]	0.57	1.20	1.02	1.19

[a] Ratio between the average of the hyper-volume from 10 runs for each parameter set and the standard NSGA-II implementation, larger is better; [b] Parameter sets with Pareto fronts shown in Fig.5.

While PCA is commonly used as a feature reduction tool, and in this work, that aspect was kept, the best results are obtained when using all the principal components. Unlike its traditional application, here the main contribution of PCA is in re-encoding the design variables using the covariance found in the currently best set of solution, hence the components with few variance, work to fine tune the solution, while the components with high variance work to explore the search space. When the number of components used is reduced, the performance initially worsens. Eventually, the number of components is small enough that the search space size is effectively reduced increasing performance once again, however, in this example the ability to fine tune solutions is lost.

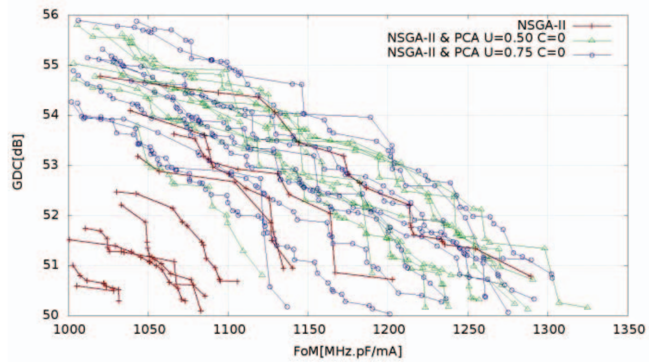

Fig. 5. Pareto fronts from the SSAMP optimization, for NSGA-II, NSGA-II & PCA U=0.50 C=0 and NSGA-II & PCA U=0.75 C=0. Large values are better.

B. *Optimization of a Voltage Controled Oscillator*

The LC-Voltage Controlled Oscillator (VCO) circuit, whose schematic is shown in Fig. 6, was optimized with a 1 pF load capacitance for a 1.2V 130 nm RF process targeting both minimum phase noise (PN) and power consumption (P). The design variables and corresponding ranges are shown in Table V, and, the detailed target specifications are presented in Table VI. The circuit simulations were done in ELDO RF and each optimization took around 40 minutes.

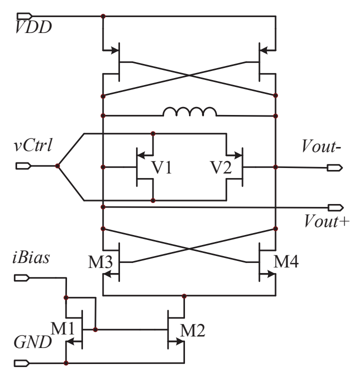

Fig. 6. LC-Voltage Controlled Oscilator's circuit schematic.

TABLE V. LC-VCO VARIABLES AND RANGES

Variable (Unit)	Min.	Grid.	Max.	Variable (Unit)	Min.	Grid.	Max.
l1, l3, l5, lvar [nm]	120	10	1000	nf1, nf3, nfvar	4	2	16
w1 w3 w5 wvar [μm]	1	0.1	10	nf5	4	2	32
outd [μm]	90	0.01	290	ib [mA]	0.1	0.1	5

The variables l1, w1, and nf1 are the length, width and number of fingers of M1 and M2; l3, w3, and nf3 of M3 and M4; l5, w5 and nf5 of M5 and M6; lvar, wvar and nfvar of V1 and V2; outd is the outer diameter of the inductors, and ib the value of the bias current.

TABLE VI. LC-VCO SPECIFICATIONS

	Measure	Target	Units	Description
Objectives	PN	Min.	dBc/Hz	Phase Noise Measured @ 1 MHz
	P	Min.	mW	Power Consumption
Constraints	Idd	≤ 6	mA	Current Consumption
	OF	≥ 2.4;≤2.4835	GHz	Oscillation Frequency
	OVS	≥ 100	mV	Output Signal Amplitude
	PN	≤ -100.0	dBc/Hz	Phase Noise@ 1 MHz
	OV[1]	≥ 80	mV	Overdrive Voltages (V_{GS} - V_{TH})[2]
	D[1]	≥ 50	mV	Saturation Margin (V_{DS} - V_{DSat})[2]

[1] The constraint applies to: M1, M2, M3, M4, M5 and M6; [2] For PMOS devices the overdrive is Vt – Vgs and delta is Vdsat – Vds

3 runs with each parameter set were executed with a population of 64 elements and 100 generations, like before. Tables VII shows the average HV improvement w.r.t. to standard NSGA-II, and in Fig. 7 the Pareto fronts obtained with for NSGA-II and the parameter sets $^{(U,C)}$ (0.25, 5) and (0.50, 0) is shown. Again, and despite the differences in the function, devices and specifications of the target circuit, the proposed method can be used to consistently improve the effectiveness of the optimization, reaching solutions with improved power consumption and improved phase noise.

TABLE VII. HV RATIO[a] FOR THE TWO STAGE AMPLIFIER AS A FUNCTION OF THE PCA USE RATE (U) AND THE NUMBER OF REMOVED COMPONENTS (C)

U \ C	0	2	5	8	11
0.25	1.05	1.03	**1.08**[b]	1,04	1.04
0.50	**1.07**[b]	1.06	**1.07**	1.06	0.99
0.75	1.05	1.03	**1.06**	0.98	0.93

[a] Ratio between the average of the hyper-volume from 3 runs for each parameter set and the standard NSGA-II implementation, larger is better; [b] Parameter sets with Pareto fronts shown in Fig.7.

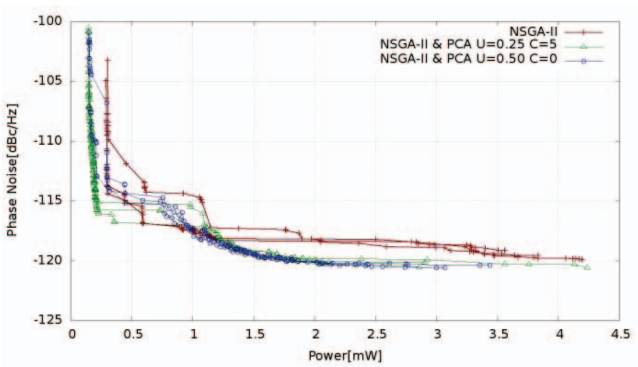

Fig. 7. Pareto fronts from the LC-VCO optimizaiton, for NSGA-II, NSGA-II-PCA U=0.25 C=5 and NSGA-II-PCA U=0.5 C=0. Small values are better.

V. CONCLUSION

The automatic analysis of the correlations between all design variables over the optimal design trade-offs is used in this work to accelerate analog and RF IC sizing optimization. PCA is here used, for the first time, to re-encode the design variables, creating a more meaningful search space, w.r.t. the target circuit and specifications. The proposed method was validated in the optimization of two widely used and remarkably different circuits, an amplifier and a VCO. Reaching, in both cases, wider solution sets, and an improving from 8% to 290% in terms of hypervolume.

Moreover, the proposed use of PCA for variable re-encoding, in the scope of stochastic optimization, was applied together with the NSGA-II evolutionary kernel, but it is suitable to be applied with any optimization method that maintains a set of solutions, as it is the case of many single and most multi-objective optimization algorithms.

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