Degradation Analysis of High Performance 14nm FinFET SRAM

Daniël Kraak Innocent Agbo Mottaqiallah Taouil Pieter Weckx[1,2] Stefan Cosemans[1] Francky Catthoor[1,2] Said Hamdioui
Delft University of Technology
Mekelweg 4, 2628 CD Delft, The Netherlands
{D.H.P.Kraak, I.O.Agbo, M.Taouil, S.Hamdioui}@tudelft.nl

[1]imec vzw., Kapeldreef 75, B-3001, Leuven, Belgium
[2]Katholieke Universiteit Leuven, ESAT, Belgium
{Pieter.Weckx, Francky.Catthoor}@imec.be

***Abstract*—Memory designs usually add design margins to compensate for chip aging; this may lead to yield and performance loss (in case of overestimation) or reduced reliability (in case of underestimation). This paper analyzes the impact of aging on cutting edge high performance 14nm FinFET SRAM using a calibrated aging model; it does not only analyze the impact of the SRAM's components individually, as it is the case in prior work, but it also investigates the contribution of the interaction of these components while considering different workloads; both the overall metric of the memory (i.e., the access time) as well as metrics of individual components (e.g., sensing delay for the sense amplifier) are examined. The results show that it is crucial to consider not only the aging of all individual components, but also their interaction in order to provide accurate prediction of aging effects; considering only aging of single/individual components leads to either too optimistic or pessimistic results. For example, using our approach (which includes the components interaction) results approximately in 9.1% degradation of memory access time (for three years of aging), while using the traditional approach (based on adding the impact of individual components) results in 7.3% increase only; a relative difference of 25%, for which the timing and the address decoder components are the main contributors. With respect to individual components, the sense amplifier is the most fragile one (e.g., its offset voltage spec. degrades up to 58%.)**

***Index Terms*—Reliability, aging, SRAM, FinFET**

I. Introduction

The continuous downscaling of CMOS technology has significantly improved the performance and functionality of integrated circuits. However, this impacts the reliability negatively due to increased impact of *time-zero* and *time-dependent* variability [1], [2], [3]. Time-zero variation (or process variation) is caused by imperfections during production. As a result, circuits have different characteristics than the intended ones. Time-dependent variations are variations that occur during the lifetime. It includes *environmental variations*, such as supply voltage and temperature fluctuations, and *aging variations* due to, for instance, *Bias Temperature Instability* (BTI). In order to guarantee the required quality in terms of low failure rates and lifetime at optimal design, it is necessary to properly assess the effects of these variabilities for any electronic component, such as SRAM which is the topic of this paper.

Previous studies on SRAM reliability analysis have mainly focused on the impact of aging on memory cell array [4], [5], [6], [7], [8], [9]; only limited work has been published on the degradation of the memory peripheral circuitry; examples are sense amplifier [10] and timing circuit [11]. The published works consider appropriate metrics for the circuit under investigation; e.g., noise margins for the memory array, sensing delay for the sense amplifier, etc. Nevertheless, understanding and estimating the aging of each individual component does not mean that the impact on the overall memory reliability is straightforward to identify; not only because it is difficult to estimate the effects of the degradation of individual components on the operation of the memory as a whole, but also because the degradation of a component will be (potentially considerably) affected by the degradation of another one. To the best of our knowledge, there are only two works which tried to address this limitation and investigate the impact of aging, while considering the interaction between multiple components or the whole memory [12], [13]. The authors in [12] investigated the impact of aging on the interaction between the memory cell and sense amplifier; the analysis does not include important circuits such as the timing circuit and address decoder. On the other hand, the authors in [13] investigated the effects of aging on a complete $28\,\mathrm{nm}$ SRAM circuit, but did not examine how the interaction between components contribute to their mutual degradation and did not explore the stochastic nature of aging.

This work investigates the impact of aging on a high performance, state-of-the-art, $14\,\mathrm{nm}$ FinFET complete SRAM using a calibrated atomistic BTI model; we perform a detailed analysis of the impact of aging on the *overall* memory (i.e., the access time), on each memory component (using their appropriate metrics), and of the contribution of the interaction of the components both to the overall memory degradation as well as to the degradation of individual components. In short, this paper distinguishes itself from the prior work in the following aspects: a) it uses a full 14nm high performance FinFET SRAM design (1kB) based on a "realistic industrial-strength" circuit design, b) it examines the contribution of the *interaction* between the different components on aging of individual components as well as on the whole memory system, c) it uses *calibrated* aging models which significantly improve the accuracy of the results.

The rest of the paper is organized as follows. Section II discusses the simulation setup. Section III presents the obtained results. Finally, Section IV concludes the paper.

978-3-9819263-0-9/DATE18/©2018 EDAA

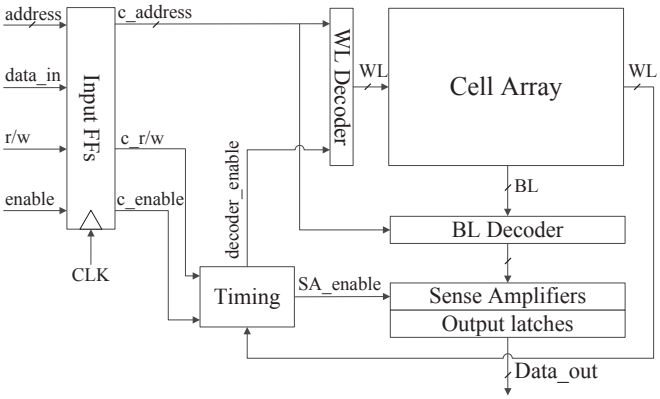

Fig. 1: Block diagram of memory.

II. Simulation Setup

First the used memory model for aging analysis is discussed. Then, the metrics evaluated during the analysis and the proposed analysis methodology, respectively, are addressed.

A. Memory Model

The memory model used for the analysis is a high performance memory from imec, implemented in FinFET $14\,\mathrm{nm}$ technology; such memories are typically deployed in L1 caches. The memory has a size of $1\,\mathrm{kB}$ and a logical word length of $32\,\mathrm{bits}$. It is able to run at a frequency of $2\,\mathrm{GHz}$ under worst-case conditions. Figure 1 depicts a block diagram of the memory, with relevant components. The functionality and specifications of these components are as follows:

- **Input Flip-Flops**: the memory is controlled through the input flip-flops. The *address* signal contains the memory address of the read/write operation. The *enable* signal specifies whether the memory should perform an operation or remains idle. The *r/w* signal selects the type of operation (read or write).
- **Cell Array**: the cell array consists of a grid of 128 rows by 64 columns. It is implemented using high performance cells with a 1:2:2 ratio (1 fin for the pull-up transistor, 2 fins for the pass-gate as well as for the pull-down).
- **WL Decoder**: the wordline (WL) decoder selects the appropriate row in the cell array based on the input address.
- **BL Decoder**: the bitline (BL) decoder selects the appropriate columns in the cell array based on the input address.
- **Timing**: the timing circuit is the main driver of the memory. It provides timed control signals to other components during operation (e.g., enabling the WL decoder). It makes use of a WL detect scheme, to detect the activation of one of the wordlines.
- **Sense Amplifiers**: the sense amplifiers amplify the generated bitline swing on the bitlines to generate full-swing read values. They are implemented using latch-type sense amplifiers. Each of the two critical pull-down transistors are implemented using 16 fins.
- **Output latches**: the output latches hold the read value. They are controlled by the sense amplifiers and are implemented using SR latches.

When a read operation is performed, the timing circuit is activated by the *enable* signal. Meanwhile, the selected address is applied to the WL and BL decoders to select the respective rows and columns of the cell array. Subsequently, the timing circuit activates the WL decoder using the *decoder_enable* signal. Note that the timing circuit allocates sufficient time before it activates *decoder_enable*; this ensures that all logical paths in the WL decoder have finished propagating when a new address is selected. Once the timing circuit detects the activation of the wordline using its WL detect scheme, it keeps the wordline activated for a certain period to provide enough time for the memory cells to discharge the bitlines. Finally, the timing circuit enables the *SA_enable* signal to trigger the sense amplifiers and amplify the differential voltage on the bitlines to digital values.

B. Metrics

The analysed metrics are divided into an overall memory metric and component metrics. The overall metric evaluates the degradation of the memory as a whole, while the component metrics evaluate the memory components.

Overall Metric

The overall metric used is the *read access time*. The read access time is the delay between starting the read operation and the operation being completed. It is measured as the delay between the rising edge of the clock and the data appearing at the memory's output. Typically, the access time of a read operation is higher than that of a write operation; in a read operation, the sense amplifier is activated after the wordline activation, while in a write operation the cell is already written during the wordline activation. Therefore, we consider the read access time only.

Component Metrics

We define one or more metrics for the most important components of the memory. The components include the sense amplifier, the memory cell, and the address decoder. Other components such as the precharge circuitry and write drivers are not part of this study, as their performance is less critical. For instance, the logic of the precharge circuitry is relatively simple and has a wide operation window. Each component and its metric(s) are discussed briefly next.

Memory Cell: we use the metrics *bitline swing* and *read noise* to evaluate the memory cell's performance. The bitline swing metric is illustrated in Figure 2. SAenable presents the enable signal of the sense amplifier, BL/BLBar the voltage swing on the differential bitline pair connected to the accessed cell, and SA_Out/SA_outbar the differential output signal of the sense amplifier. The metric bitline swing is defined as the differential voltage on the bitlines generated by the memory cell at the moment the sense amplifier is enabled. It is shown as ΔV_{BL} in the figure. It is measured at the inputs of the sense amplifier.

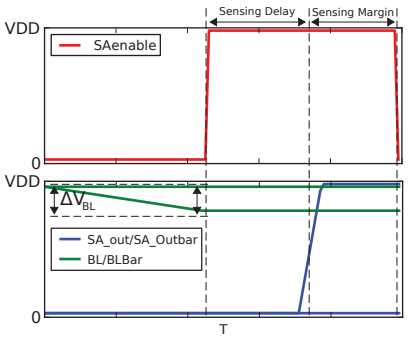

Fig. 2: Metrics sensing delay, sensing margin, and bitline swing (ΔV_{BL}).

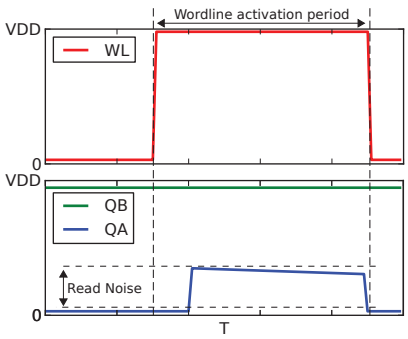

Fig. 3: Metric read noise.

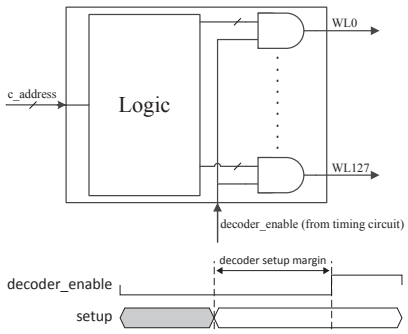

Fig. 4: Metric decoder setup margin.

The metric read noise is illustrated in Figure 3. Here, WL is the wordline activation signal, and QA/QB are the internal nodes of the memory cell. The read noise is defined as the maximum disturbance of the low internal node of the memory cell during the wordline activation period. During a read operation, the wordline is activated and the internal nodes of the cell are exposed to the precharged bitlines. As a result, the internal node holding a logic 0 is charged and its voltage rises. If this disturbance is too high, the cell might flip.

Sense Amplifier: we use the metrics *sensing delay*, *sensing margin* [13], and *offset voltage specification* to evaluate the sense amplifier's performance. The sensing delay and sensing margin are also illustrated in Figure 2. The sensing delay is defined as the time between the enabling of the sense amplifier and the output of the sense amplifier being ready. The sensing margin is defined as the time between the sense amplifier output being ready and the disabling of the sense amplifier.

Besides, the sensing delay and sensing margin, the offset voltage is also an important metric of the sense amplifier. The offset voltage is defined as the differential input voltage that results in a differential output voltage of zero. Due to process variation and aging, each SA has a different offset voltage [14]. The offset voltage determines the minimum bitline swing (ΔV_{BL} in Figure 2) required to perform a successful read operation. We evaluate the sense amplifier's offset voltage using the *offset voltage specification* metric from [14]. The offset voltage spec. is defined as the minimum amount of bitline swing that should be generated on the sense amplifier's inputs in order to achieve a target failure rate f_r. In this work we use a target failure rate of f_r=10^{-9}.

Address Decoder: we use the metric *decoder setup margin* to evaluate the performance of the address decoder. It is defined as the minimum time between the WL decoder setup signals being ready and the activation of the decoder enable signals, as illustrated in the bottom part of Figure 4. We illustrate this metric using a simplified diagram of the WL decoder as shown at the top part of Figure 4. The WL decoder is controlled by the timing circuit. AND-gates in the final stage of the decoder ensure that a wordline can only be activated when the decoder is enabled. In case the delay of the decoder logic exceeds the time that the enable_decoder is activated, a wrong wordline might be activated. Hence, the *decoder setup margin* is the minimum time between the setup signals of the AND-gates being ready and the activation of the enable_decoder signal.

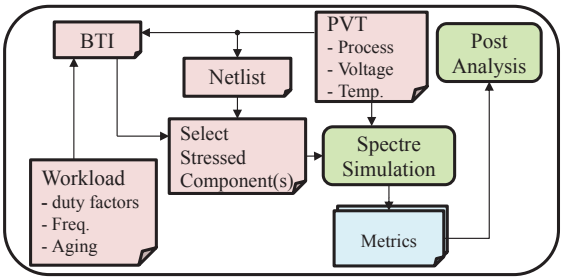

Fig. 5: Proposed methodology.

C. Methodology

Figure 5 shows the proposed methodology used to analyze the impact of aging/BTI on the memory. The methodology performs Monte Carlo simulations using Spectre during which process variation and BTI are injected into the netlist of the memory. During each Monte Carlo iteration the metrics discussed in the previous section are measured. Finally, post-analysis is performed on the measured metrics to determine their average and spread. To model BTI, the atomistic model presented in [15] is used. It takes into account the workload dependency, which is modelled by the duty factors and frequencies of the transistors [16], [17]. To simulate the memory netlist, the PTM $14\,\mathrm{nm}$ FinFET LSTP library [18] is used, which we calibrated with commercial $14\,\mathrm{nm}$ libraries to match their transfer curves.

One of the key features of the methodology is that it first injects aging/BTI into individual components. This makes it possible to analyze the individual impact of aging of each component or their combined impact. This work distinguishes between the following components: the memory cells, the sense amplifiers, the address decoder (consists of both the WL and BL decoders), and the timing circuit. Subsequently, the combined aging of all components (i.e., the whole memory is aged) is analyzed. Finally, it should be noted that the proposed methodology is generic and could also be used to analyze the impact of aging on other designs and circuits.

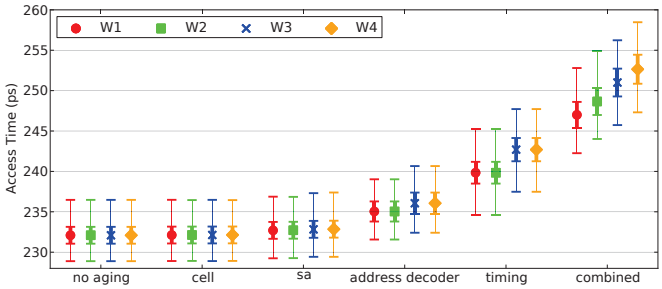

Fig. 6: Impact of aging on the read access time of the memory.

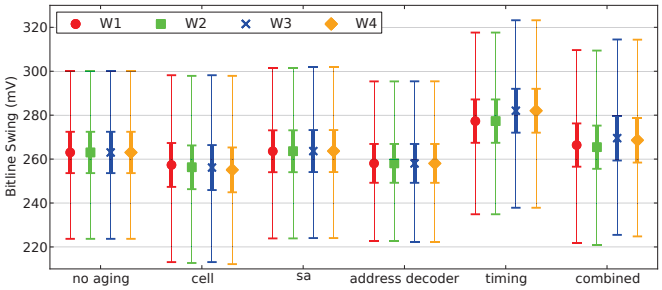

Fig. 7: Impact of aging on bitline swing.

III. Results

A. Performed experiments

The methodology of Figure 5 is used to analyze the impact of aging on the overall metric as well as the component metrics. First, simulations without aging (only process variation) are performed followed by simulations for three years of aging (also with process variation). The memory is aged at a temperature of 85 °C and a nominal supply voltage of 0.8 V. For the aging, four different workloads are used. They can be described with the following March algorithms:

- W1: ⇑(w0, r0, i^8, w1, r1, i^8)
- W2: ⇑(w0, r0, i^8)
- W3: ⇑(w0, r0, w0, r0, i, w1, r1, w1, r1, i)
- W4: ⇑(w0, r0, w0, r0, i)

Workloads W1 and W2 (W3 and W4) assume that 20% (80%) are memory instructions and that the memory is idle (i) for 80% (20%) of the time. Their difference is that W1 (W3) has a balanced workload for the memory cells and read/write circuitry, while W2 (W4) has an unbalanced workload. What all workloads have in common is that they iterate over all 256 memory addresses. Hence, each address is selected/stressed an equal amount of time.

We perform 1000 Monte Carlo simulations for the analysis. During each Monte Carlo iteration, a read from address zero is simulated, of which the memory cells have been initialized with zeroes. During this read operation, all metrics (discussed in the previous section) are measured. To evaluate the decoder setup margin, an address transition from 255 to 0 is simulated.

B. Results

Overall Metric

Figure 6 shows the impact of aging on the read access time for all four workloads. The mid-point of the markers shows the average value, the horizontal inner edges the sigma spread, and the outer edges the observed minimum and maximum values from simulation. Several cases are shown along the x-axis. First, the case without aging is shown, which only shows the impact of time-zero variability. Subsequently, cases are shown where only the memory cells (cell), sense amplifier (sa), address decoder, or timing circuit are aged. Finally, the combined aging case is shown.

The figure reveals that the degradation of the cell and sense amplifier have a marginal impact on the access time, while the degradation of the address decoder and timing circuit have a higher impact. The impact of the sense amplifier is marginal, since its delay is only a small fraction of the total access time. Consequently, the impact of the cell is also marginal, since its aging mainly impacts the sense amplifier. The high impact of the address decoder is caused by the degradation of the gates that drive the wordlines. As a result, the activation of the respective wordline is delayed, which in turn delays the whole memory operation. The timing circuit has the highest impact on the access time degradation, because it has the longest paths. Hence, increasing cumulative delays along these paths result in its high impact. At time-zero, i.e., no aging, the average access time is 232 ps and it increases up to 253 ps (∼9.1% increase) for the combined aging case for workload W4. When only the address decoder, timing circuit, or output latches and buffers age, the average access times equal 236 ps (4 ps increase), 242 ps (10 ps increase), and 235 ps (3 ps increase), respectively. Hence, the combined aging case results in a significantly higher increase in delay (21 ps) than when taking the sum of the added delays (17 ps, ∼7.3% increase). This happens due to the dependencies between the components.

Comparing the workloads with the low (W1 and W2) and high access rates (W3 and W4) reveals that workloads that access the memory more often give a higher degradation, as they stress the logic paths of the address decoder and timing circuit more often. Therefore, they give a higher degradation and, thus, a higher access time. Moreover, we conclude that balancing of the read/write values is less important than the activity rate of the memory, as the degradation of the access time is dominated by the address decoder and timing circuit.

Component Metrics

Memory Cell: Figure 7 shows the impact of aging on the bitline swing. Aging of the cell causes a degradation in its pull-down and pass transistors while aging of the address decoder causes a degradation of the pass transistors of the column selectors. Hence, the degradation of these components reduces the bitline swing. Aging of the timing circuit causes a delayed activation of the sense amplifiers and, therefore, the cells get more time to discharge the bitlines. Hence, the degradation of the timing circuit increases the bitline swing. Due to this compensating behavior of the aged timing circuit, we even observe that for the case combined aging the average bitline swing increases (up to 2.5% increase) compared to the average bitline swing at time-zero (no aging). However, due

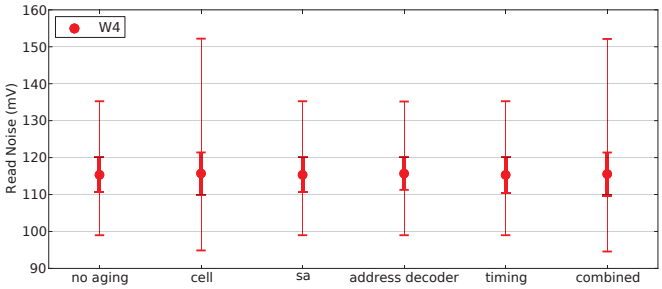

Fig. 8: Impact of aging on read noise.

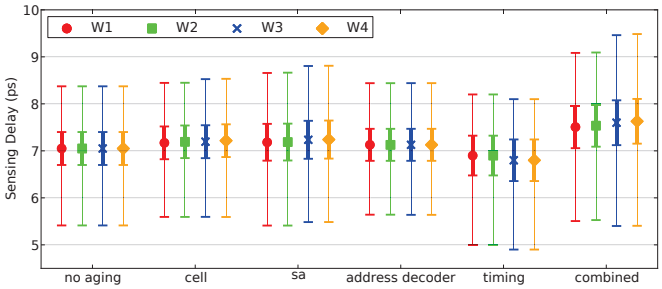

Fig. 9: Impact of aging on sensing delay.

to an increase in spread of the distributions, the minimum observed bitline swings of the combined case are lower for workloads W1 and W2 (up to 1.2% decrease) compared to time-zero and marginally higher for W3 and W4 (up to 0.8% increase). This shows the importance of considering the impact of aging on the statistical distributions of metrics, rather than only considering average values.

Figure 8 shows the impact of aging on the read noise for workload W4. The figure clearly shows that the read noise is only impacted by the degradation of the cell; the same trend was observed for all other workloads. Note that the read noise is mainly determined by the strength ratio of the pass gate and pull-down transistors of the cell. Therefore, the aging of the peripheral logic does not impact the read noise, which contradicts the findings of study [13]. They claim that the read noise increases due to peripheral logic aging, as the wordline is activated longer. However, when we simulate a cell access, we observe that the read noise reduces over time as the pull down transistor of the node holding the zero discharges the bitline.

Sense Amplifier: Figure 9 shows the impact of aging on the sensing delay. The figure reveals that the degradation of the sense amplifier, cell, and address decoder increase the sensing delay, while the degradation of the timing circuit improves the sensing delay. Aging of the sense amplifier increases the sensing delay, mainly due to the degradation of the pull down tranistors of its cross-coupled inverters. Aging of the memory cells and address decoders reduce the generated bitline swing at the input of the sense amplifier. For the cell this is caused by the degradation of its pull-down and pass transistors. For the address decoder it is caused by the degradation of the bitline decoders, which are implemented with pass transistors. Thus, their degradation decreases the bitline swing, which negatively impacts the sensing delay. Degradation of the timing circuit improves the sensing delay, as aging in the timing circuits delays the activation of the sense amplifiers. Therefore, the memory cells have more time to discharge the bitlines, thus reducing the sensing delay. However, the timing circuit is unable to fully compensate for the degradation of the sensing delay caused by the other components. As a result, the combined case has a higher sensing delay (up to 8.2% increase for the average sensing delay) than at time-zero.

Figure 10 shows the impact of aging on the sensing margin. The figure shows that the degradation of the sense amplifier, cell, and address decoder decrease the sensing margin, while aging of the timing circuit improves the sensing margin. Degradation of the sense amplifier, cell, and address decoder worsens the sensing margin, as these circuits increase the sensing delay. The degradation of the timing circuit improves the sensing margin, as it not only leads to a larger bitline swing, but also delays the deactivation of the sense amplifier. Due to the long logic paths in the timing circuit, the deactivation of the sense amplifier is delayed significantly. As a result, the combined case has a higher sensing margin (up to 21% increase) compared to time-zero.

TABLE I: Impact of aging on sense amplifier's offset voltage.

Workload	No Aging	W1	W2	W3	W4
Offset Voltage Spec. (mV)	38.2	47.5	55.5	50.0	60.2

Table I contains the sense amplifier's offset voltage spec. at time-zero and for three years of aging for the four workloads. The table shows that the offset voltage is very susceptible to unbalanced workloads (W2 and W4), which aligns with the study in [14]. Unbalanced workloads cause an unbalanced degradation of the transistors in the sense amplifier and, therefore, they increase its offset voltage. As a result, the offset voltage spec. increases in the worst-case by ∼58% for workload W4. Moreover, in the best-case (balanced workload W1) the offset voltage spec. increases ∼24.3%. We observed in the previous section that the minimum bitline swings were either lower or marginally higher than at time-zero. This clearly shows that the degradation of the timing circuit is unable to compensate for the sense amplifier's degradation. Hence, sufficient margin for the bitline discharge should be added to the design, as otherwise incorrect read values may be generated.

Address Decoder: Figure 11 shows the impact of aging on the decoder setup margin. The figure reveals that the decoder setup margin is not impacted by the degradation of the memory cells and sense amplifiers. Furthermore, the figure shows that the degradation of the address decoder decreases the decoder setup margin, as the logic paths of the WL decoder become slower, while the degradation of the timing circuit improves it, as the activation of the WL decoder is delayed. As a result, the average decoder setup margin increases even up to 1.6% for combined aging for workloads with a high access rate (W3 and W4) as compared to time-zero. However, due to an increase in spread, the minimum observed margin is significantly lower (∼6% lower in the best-case).

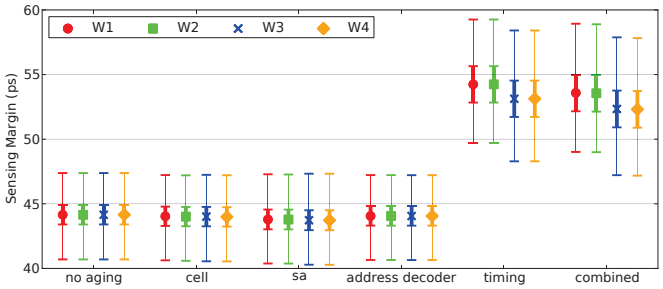

Fig. 10: Impact of aging on sensing margin.

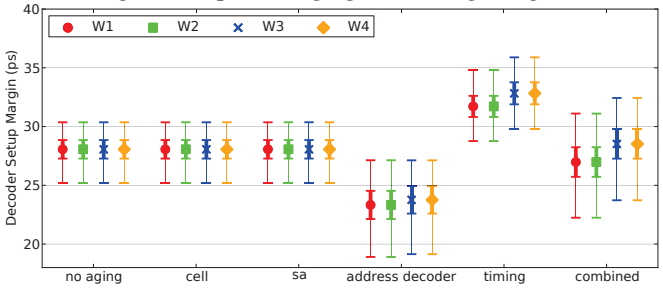

Fig. 11: Impact of aging on decoder setup margin.

C. Discussion

Based on the results of this study we make the following observations w.r.t FinFET SRAM reliability estimation:

Interaction: the reliability of a memory system is a *global* problem and it is crucial to consider the impact of aging on the *interaction* of *all* components in order to obtain accurate predictions; considering only the impact of *individual* components leads to either too pessimistic or optimistic results (observed for both the overall metric and the component metrics). Therefore, for example, combined aging of all components (including their interactions) resulted in 9.1% degradation of memory's access time, while adding the impact of each individually aged component resulted in an increase of only 7.3%. A limitation of our work is that it did not explore the impact of aging on the overall memory's robustness/reliability; that is an ongoing task.

Component sensitivity: our case study (1KB, high performance FinFET SRAM) reveals that the degradation of the timing circuit and address decoder have the highest impact on the overall memory access time. For bigger memories, it is expected that the timing circuit becomes the dominant factor for the access time degradation, as the time needed to activate the wordline by the address decoder will be a smaller fraction of the whole operation period.

Stochastic nature of aging: investigating only the average impact of aging is misleading (due to the stochastic nature of reliability failure mechanisms such as BTI), and may even lead to incomplete conclusions. In several cases we observed that the average values of metrics improved as compared to time-zero, while, due to an increase in spread, the minimum/maximum values of metrics worsened. For example, for the address decoder the average decoder setup margin improved with up to 1.6%, while the minimum margin worsened with at least 6%.

IV. Conclusion

This work clearly shows that it is important to consider not only aging of all memory components, but also their mutual interaction. This allows designers to optimize guardbands and have accurate predictions of the degradation of circuits. As a result, circuits have a higher performance, yield, and reliability.

References

[1] S. Hamdioui, D. Gizopoulos, G. Guido *et al.*, "Reliability challenges of real-time systems in forthcoming technology nodes," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2013*, March 2013, pp. 129–134.

[2] S. Borkar, "Microarchitecture and design challenges for gigascale integration," in *Intl. Sympos. on Microarchitecture*, Dec 2004, pp. 3–3.

[3] K. Kang, S.P. Park, K. Roy *et al.*, "Estimation of statistical variation in temporal nbti degradation and its impact on lifetime circuit performance," in *2007 IEEE/ACM International Conference on Computer-Aided Design*, Nov 2007, pp. 730–734.

[4] S.V. Kumar, K.H. Kim, and S.S. Sapatnekar, "Impact of nbti on sram read stability and design for reliability," in *7th International Symposium on Quality Electronic Design (ISQED'06)*, March 2006, pp. 6 pp.–218.

[5] S. Khan, I. Agbo, S. Hamdioui *et al.*, "Bias temperature instability analysis of finfet based sram cells," in *2014 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2014, pp. 1–6.

[6] B. Cheng, A.R. Brown, and A. Asenov, "Impact of nbti/pbti on sram stability degradation," *IEEE Electron Device Letters*, vol. 32, no. 6, pp. 740–742, June 2011.

[7] S.V. Kumar, K.H. Kim, and S.S. Sapatnekar, "Impact of nbti on sram read stability and design for reliability," in *7th International Symposium on Quality Electronic Design (ISQED'06)*, March 2006, pp. 6 pp.–218.

[8] A. Bansal, R. Rao, J.J. Kim *et al.*, "Impacts of nbti and pbti on sram static/dynamic noise margins and cell failure probability," *Microelectronics Reliability*, vol. 49, no. 6, pp. 642 – 649, 2009, iMAPS-CPMT Poland 2008. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271409000894

[9] A. Gebregiorgis, M. Ebrahimi, S. Kiamehr *et al.*, "Aging mitigation in memory arrays using self-controlled bit-flipping technique," in *The 20th Asia and South Pacific Design Automation Conference*, Jan 2015, pp. 231–236.

[10] R. Menchaca and H. Mahmoodi, "Impact of transistor aging effects on sense amplifier reliability in nano-scale cmos," in *Thirteenth International Symposium on Quality Electronic Design (ISQED)*, March 2012, pp. 342–346.

[11] H.I. Yang, S.C. Yang, W. Hwang *et al.*, "Impacts of nbti/pbti on timing control circuits and degradation tolerant design in nanoscale cmos sram," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 6, pp. 1239–1251, June 2011.

[12] I. Agbo, M. Taouil, S. Hamdioui *et al.*, "Read path degradation analysis in sram," in *2016 21th IEEE European Test Symposium (ETS)*, May 2016, pp. 1–2.

[13] J. Kinseher, L. Hei, and I. Polian, "Analyzing the effects of peripheral circuit aging of embedded sram architectures," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2017*, March 2017, pp. 852–857.

[14] I. Agbo, M. Taouil, S. Hamdioui *et al.*, "Quantification of sense amplifier offset voltage degradation due to zero-and run-time variability," in *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2016, pp. 725–730.

[15] B. Kaczer, T. Grasser, P.J. Roussel *et al.*, "Origin of nbti variability in deeply scaled pfets," in *2010 IEEE International Reliability Physics Symposium*, May 2010, pp. 26–32.

[16] B. Kaczer, S. Mahato, V.V. de Almeida Camargo *et al.*, "Atomistic approach to variability of bias-temperature instability in circuit simulations," in *2011 International Reliability Physics Symposium*, April 2011, pp. XT.3.1–XT.3.5.

[17] P. Weckx, M. Simicic, K. Nomoto *et al.*, "Defect-based compact modeling for rtn and bti variability," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, April 2017, pp. CR–7.1–CR–7.6.

[18] "Predictive technology model," http://ptm.asu.edu/.