A Circuit-Design-Driven Tool with a Hybrid Automation Approach for SAR ADCs in IoT

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***Abstract*—A circuit-design-driven tool with a hybrid design automation approach for asynchronous SAR ADCs in IoT applications is presented. To minimize the circuit design time while still being able to maintain ADC performance, the hybrid approach allocates automation and manual effort properly for each block: fully-synthesized control logic, highly-automated DAC and S&H circuit, library-based comparator and template-based layout generation. A user interface governs the automated design flow from specification and circuit implementation to layout generation. Two prototypes are generated using the proposed flow in 40nm CMOS: an 8b 32MS/s and a 12b 1MS/s SAR ADC. The measured and the simulated ADC performance are in good agreement, showing the robustness of the proposed method. At 1V supply, two chips consume 187μW and 16.7μW, achieving 30.7fJ/conversion.step and 18.1fJ/conversion.step respectively.**

***Index Terms*—Hybrid, Design Automation, SAR ADC**

I. Introduction

Many wireless sensor nodes (WSN) in the IoT/IoE applications (e.g., BLE and IEEE 802.15.4) require Analog-to-Digital Converters (ADCs) with moderate resolution (8∼12bit) and speed (∼MS/s). To achieve an optimum performance, each ADC has to be customized, increasing the design cost and time. To overcome this issue, circuit design automation is desired for ADCs to minimize design cost while still maintaining performance.

Circuit design automation started with relatively simple analog cells, e.g., Operational Amplifiers (OP-AMP) [1]. However, the design automation for ADCs is cumbersome due to its more complicated architecture, larger scale circuitry as well as more sophisticated signal processing between analog and digital domain. Prior-art tried to apply one single automation method to the whole ADC. [2] replaces the traditional analog circuitry with pure digital gates so that the whole ADC can be integrated in the digital synthesis flow. However, the resolution and the performance are limited due to the architecture. [3] synthesizes a $\Sigma\Delta$ ADC using a library-based approach and standard P&R for layout. Although all the analog components are still manually designed, the power efficiency is yet behind state-of-the-art. Among the numerous ADC architectures, the Successive Approximation Register (SAR) ADC is very popular for WSNs thanks to its excellent power efficiency [4]. [5] introduced a compile method for only the layout generation of the SAR ADC. [6] introduces a systematic design method on schematic level for a SAR ADC, but large differences between simulation and measurement results are observed (>10×). Alternatively, instead of applying an identical automation approach for all the circuits, a circuit-design-driven tool based on a hybrid automation approach for SAR ADCs is introduced in this work, allowing different automation approaches for each circuit. In this way, through balancing automation level and customization, the design time due to repetitive labor work is reduced while maintaining the ADC performance.

The remainder of the paper is organized as follows: Section II introduces the architecture of the SAR ADC and the hybrid automation approach. The implementation details of the automation tool and the circuits are presented in section III. The measurement results are shown in section IV and the conclusions are drawn in section V.

II. Architecture

Fig. 1 shows the block diagram of a conventional N-bit SAR ADC which includes 4 main blocks: S&H, comparator, control logic and Digital-to-Analog Converter (DAC). In each SAR conversion, the Sample&Hold (S&H) samples the analog input on the capacitors inside the DAC. Using the comparator and the logic, the DAC output will approximate the sampled input voltage in N comparisons through a Successive-Approximation algorithm. In addition, asynchronous operation is adopted to avoid the power hungry high frequency clock (N×f_s) [4].

To optimize the automation method for each block, the 4 basic blocks of a SAR ADC are analyzed from two aspects: analog-oriented/digital-oriented and manual/automated (Fig. 1). Analog-oriented implies that the circuit is physically constrained (by noise, mismatch) and expertise is required to properly optimize the circuit, which may require manual effort. Digital-oriented implies that the circuit is less physically constrained and can be abstracted and synthesized more easily without loosing performance. Specifically, the control logic can be synthesized using the standard synthesis flow inherently. In addition, the DAC capacitor array can be automated: the DAC capacitance value is computed automatically according to the noise and matching requirements as shown

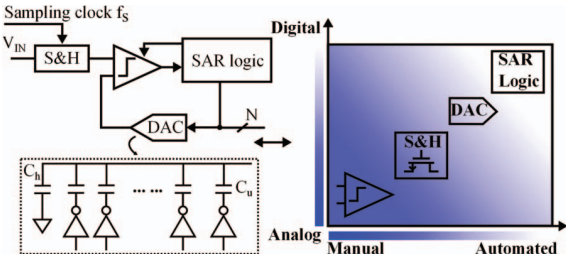

Fig. 1. The block diagram of a SAR ADC and illustration of its sub-blocks.

later. Moreover, thanks to the regularity of the DAC layout, the DAC layout design can be automated through programming. The S&H circuit together with the ADC input capacitances, influences the ADC bandwidth. To reduce design time while maintaining performance, a hybrid approach is used by tuning only the critical devices as shown later. The ADC performance is very sensitive to comparator non-idealities (e.g., offset error, noise, layout asymmetry), and therefore comparator design needs more attention and manual effort. In this design, the comparator uses a library-based method for performance.

In addition, a proper layout is very important for ADCs to achieve a satisfactory performance, which is usually very time consuming. The traditional Place&Route (P&R) in the standard digital flow minimizes the manual layout effort of digital circuits by automatic P&R [3]. However, this can cause problems for analog circuits, which are sensitive to layout non-idealities (e.g., parasitics, asymmetries, and IR drops), and thus may degrade ADC performance. Alternatively, template-based layout generation is introduced for circuits for sufficient geometric regularity, which will be explained later.

The proposed design flow can automate a SAR ADC design in 6 steps (Fig. 2): Users can provide the ADC specification (resolution N, sampling rate f_s, ...), which will be translated into requirements for the sub-blocks (e.g., noise, capacitance, ...). After that, each sub-block is generated automatically using their corresponding method. Finally, the layout of all the sub-blocks will be assembled using a geometrical template as shown later and the performance of the generated ADC is verified through simulations using extracted view. This process will end when the ADC performance reaches the design target. Otherwise, further optimization is still possible by returning to the third step and fine tuning the parameters of sub-blocks.

III. Automation Tool Implementation

As mentioned before, the circuit design starts with translating the high level ADC specifications into the sub-block requirements (Fig. 2), which is automated through an equation-based method. In particular in step 2 of Fig. 2, the resolution sets the noise floor, determining the noise budget for each noise source, e.g., the kT/C noise and the comparator noise. After that, the total input capacitance of the ADC can be computed from the kT/C noise requirement. At the same time, the input signal range of the ADC can be set ($\frac{2C_{DAC}}{C_{DAC}+C_h}$VDD) by adjusting the ratio between the DAC capacitance C_{DAC} and the attenuation capacitance C_h (Fig. 1). The resolution will indicate also the required SFDR (Spurious-Free-Dynamic-Range) for the S&H circuit. Meanwhile, the operation speed of the comparator, DAC as well as the digital control logic can be deducted from the overall ADC operation speed f_s. After that, each block will then be implemented according to the requirements, as will be described next.

A. Fully-synthesized control logic

The digital control logic of the asynchronous SAR ADC performs the binary-search algorithm and also generates an internal clock for the ADC. Therefore, in this work, the digital control logic is fully synthesized through the standard digital design flow. In particular, a monotonic switching scheme [7] is implemented to improve the power efficiency of the ADC.

B. Highly automated DAC

The charge-redistribution DAC is often chosen for SAR ADCs thanks to its good power efficiency. It consists of DAC drivers and DAC capacitors, which are automated through a script-based automation flow (Fig. 3). Equation-based method is firstly adopted to size the unit capacitor C_u with two considerations: kT/C noise and capacitor mismatch error. The two constraints result in two different unit capacitor values ($C_{u,n}$ and $C_{u,m}$), which are considered for sizing of the unit capacitor C_u. It is worthwhile to mention that for medium and low resolution ADCs, the calculated C_u is unpractically small. Therefore, a lower boundary for the C_u can be set, e.g., 300aF. On the other hand, when the ADC resolution goes beyond 10b, C_u tends to be limited by the capacitor mismatch and thus has to be sized relatively large, degrading power efficiency. Alternatively, to save power, C_u can be sized to just meet the kT/C noise, and calibration can be employed to compensate the capacitor mismatch error [8]. After selecting C_u, the DAC driver needs to guarantee that the DAC output can settle in time and is selected from a library of drivers with various strengths, matching the selected C_u and the required f_s.

A programmable cell (*Pcell*) is used for the DAC design automation and its layout generation. By programming the key parameters of the DAC, this tool enables users to provide the specification, automate the device sizing and generate the

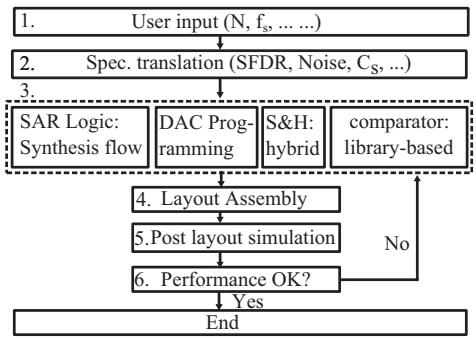

Fig. 2. Design flow of the proposed method.

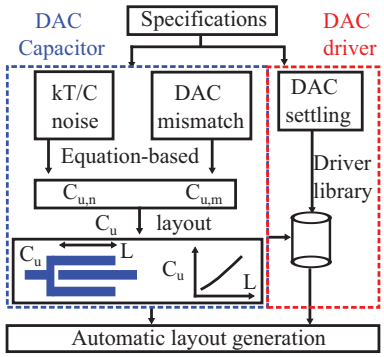

Fig. 3. The DAC design automation flow.

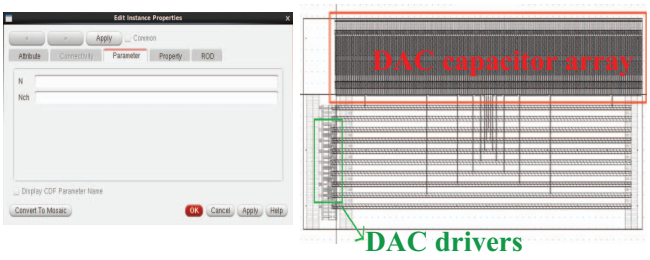

Fig. 4. GUI for DAC layout generation and a generated layout example.

layout accordingly. The Graphical-User-Interface (GUI) of the *Pcell* has two inputs (Fig. 4): N is ADC resolution and N_{ch} is the number of unit capacitors for C_h (Fig. 1) to obtain the required input signal range. C_u is customized finger capacitor as shown in Fig. 3. This allows the employment of small unit capacitance (sub-fF), and reducing the DAC area and power consumption at the same time. In addition, the unit capacitance can be approximated as linearly proportional to the overlapping length L between the top plate and bottom plate of the capacitor. Therefore, the unit capacitance can be precisely controlled by simply programming L. Moreover, this allows a fast optimization for the DAC capacitors without significantly changing the overall DAC layout. The DAC layout is automatically generated from the two parameters of the GUI of the *Pcell*, which is in *SKILL* language.

C. Hybrid automated S&H

For a given DAC capacitance, the on-resistance R_{on} of the sampling switch determines the bandwidth of the S&H. In modern CMOS technologies, the supply voltage drops below 1V, making it difficult to reach the desired bandwidth (∼MHz). Therefore, a bootstrapped circuit is used in this work as shown in Fig. 5. The circuit can be roughly divided into two parts: the devices for sampling (performance critical) and the voltage shifter (performance less-critical). Therefore, a hybrid design approach is proposed for sizing the S&H circuit (Fig. 6): the S&H will be firstly implemented (including layout) and used as the template when redesigned for a different specification. When re-designed, the less critical devices are fixed, while the critical devices are tuned for optimization. As a result, the total number of iterations needed to reach the optimum point is significantly reduced, enabling the employment of a simulation-based look-up-table (LUT) approach for the S&H

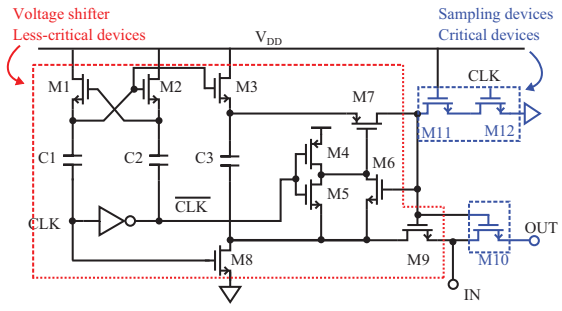

Fig. 5. The S&H circuit.

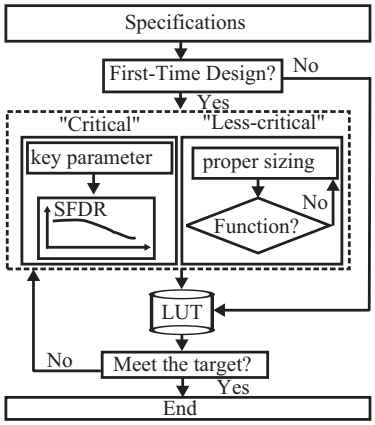

Fig. 6. The S&H design automation method.

circuit. In this way, in the next design, an approximately optimized device size can be directly selected from the LUT. Moreover, further optimization is still possible by only fine tuning the critical devices. Considering that most of the devices are fixed and only three transistors are programmed, a template-based layout generation is introduced for the S&H similarly to the DAC, which further reduces the layout design time.

D. Library-based comparator

The comparator is crucial for SAR ADCs to achieve an optimum performance in speed, noise and power efficiency. However, it is not straightforward to correlate the comparator performance with the device sizing due to its relatively complicate circuitry, non-linear operation and sensitivity to layout imperfections. Therefore, a library-based approach is introduced for the comparator design, in which comparators with different performance combinations can be selected by the computer-aided design tool when users input the specifications. In this work, a low-power architecture is preferred so that the dynamic comparator in [4] is used. The comparators in the library will have a two-dimensional index: resolution and speed. Then according to the resolution and speed requirement, the right entry in the table will be selected.

E. Template-based layout generation

The aforementioned tool for the design of the sub-blocks is developed using *SKILL* language and *Pcell* tool in Cadence. The layout generations for both sub-blocks and ADC top are both automated using a geometrical template-based method. This method allocates each sub-block according to a template, and connects the pins between each block through scripting (Fig. 7). The geometrical coordinates of all sub-blocks are parameterized and the pins location of each block are automatically adapted accordingly. This greatly saves the design time for layout, and as a result, it takes only a few seconds for the program to integrate into a DRC and LVS clean layout. After that, simulations based on extracted view can be executed to verify the performance of the ADC. Note that it is still possible to fine tune each sub-block individually to optimize the overall ADC performance using the implemented design flow.

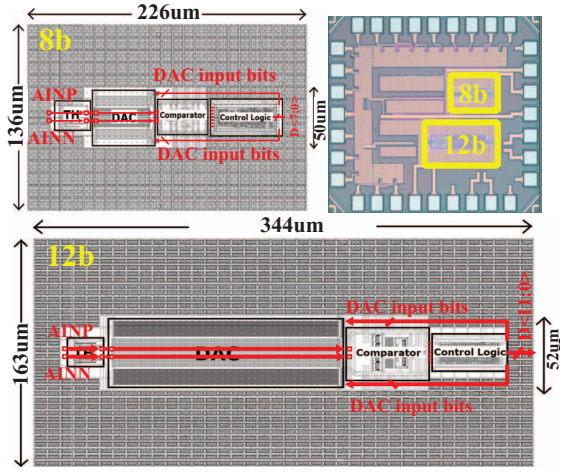

Fig. 7. The generated ADC layouts and die photo using the proposed flow.

IV. Verification with Prototypes

To verify the proposed design flow, two prototype chips with different specifications for speed and resolution are implemented in 40nm CMOS: an 8b 32MS/s and a 12b 1MS/s SAR ADC (Fig. 7). The two ADCs (Fig. 7) occupy $0.031mm^2$ and $0.056mm^2$ including decoupling capacitors in 40nm CMOS. The measured performance (Fig. 8) of the 8b ADC is comparable to the simulated results, considering that simulation results did not include non-idealities (e.g., noise and mismatches). For the 12b ADC, considering that the DAC capacitors are sized for kT/C noise instead of mismatch during design, large INL/DNL errors are measured as shown in Fig. 8, thus limiting the ADC performance. However, this error can be solved by calibration [8]. In addition, both ADCs achieve stable SNDR/SFDR up to the Nyquist frequency (Fig. 9), indicating a sufficient performance for the S&H circuits. Overall, the measured power consumption and speed match with the simulated numbers. The measured Figure-of-Merit (FoM=$\frac{\text{Power}}{2^{\text{ENOB}}\min(f_s, 2\text{ERBW})}$) for the 8b ADC is close to expectation (Table I). For the 12b ADC, the FoM is worse due to the mismatches. However, the correspondence is better than prior art.

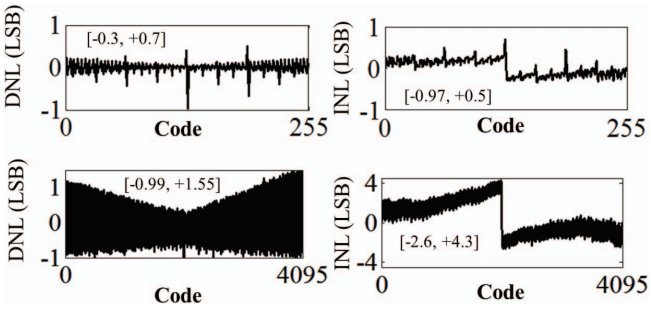

Fig. 8. The measured INL/DNL of the two ADCs.

V. Conclusions

In this work, a circuit-design-driven tool with a hybrid automation approach for SAR ADCs is proposed, with fully synthesized digital control logic, highly automated DAC and S&H circuit, library-based comparator and template-based automatic layout generation. Compared to prior-art, instead of simplifying/modifying the circuit architecture to enable synthesis, our hybrid performance-selective approach allows the employment of appropriate circuits for performance, and automation to reduce design time. In this way, the design time is reduced without compromising performance, meanwhile still keeping the possibility to control performance-critical devices through programming, enabling a balance between automation and customization.

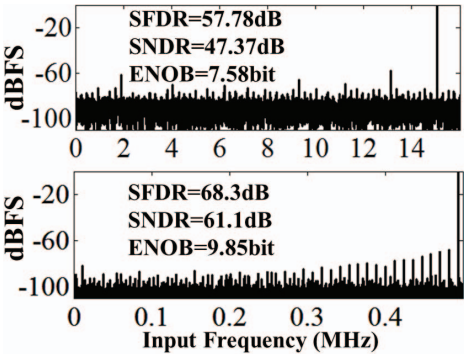

Fig. 9. Measured spectrum of the two ADCs with a near-Nyquist tone.

TABLE I
The Benchmark of the Two ADCs.

	[2]	[6]				[5]	This work			
Experiment	Meas.	Meas.	Sim.	Meas.	Sim.	Meas.	Meas.	Sim.	Meas.	Sim.
Architecture	Stochastic	SAR				SAR	SAR			
Technology (nm)	90	180		90		28	40			
Resolution (bit)	-	12		10		9	8		12	
Speed (MSps)	210	0.6		50		20	32	32	1	1
Supply voltage (V)	1.2	3.3		1		0.69	1	1	1	1
INL (LSB)	-	2.79	0.1	1.41	0.06	-	0.7	-	4.3	-
DNL (LSB)	-	5.24	0.22	2.81	0.1	-	0.97	-	1.55	-
Nyquist SNDR (dB)	29	62.7	73.9	52.1	61.9	48.84	47.37	49.3	61.1	71.6
Power (uW)	34800	328	53.5	440	155	15.87	187	192	16.7	16.8
FoM (fJ/c.s.)	7943	500	22	26.7	3.1	3.51	30.7	25.1	18.1	5.4
Meas. vs. Sim. ratio	-	22.7		8.6		-	1.2		3.4	

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