University Booth at DATE 2018

The University Booth is organised during DATE and will be located in the exhibition area. All demonstrations will take place from Tuesday, March 20 to Thursday, March 22, 2018 during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.

The University Booth programme is composed of 34 demonstrations from 14 different countries, presenting software and hardware solutions. The programme is organised in 11 sessions of 2 or 2.5 h duration and will cover the topics:

- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Future and Emerging Technologies Prototypes
- Autonomous Systems Prototypes

The University Booth at DATE 2018 invites you to find out more about the latest trends in software and hardware from the international research community.

Several demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.

More information is available online at http://www.date-conference.com/exhibition/u-booth. The University Booth programme is included in the conference booklet and available online at https://www.date-conference.com/exhibition/ub-programme. The following demonstrators will be presented at the University Booth.

ABSYNTH: A COMPREHENSIVE APPROACH TO FRONT TO BACK ANALOG BLOCK DESIGN AUTOMATION
Authors:
Abhaya Chandra Kammara S.[1], Sidney Pontes Filho[2] and Andreas König[2]
[1]ISE, TU Kaiserslautern, DE; [2]TU Kaiserslautern, DE

Timeslots:

- UB01.5 (Tuesday, March 20, 2018 10:30 - 12:30)
- UB02.5 (Tuesday, March 20, 2018 12:30 - 15:00)
- UB09.9 (Thursday, March 22, 2018 10:00 - 12:00)
- UB10.9 (Thursday, March 22, 2018 12:00 - 14:30)
- UB11.9 (Thursday, March 22, 2018 14:30 - 16:30)

Abstract: *ABSYNTH was first presented in CEBIT 2014 where complete, practical circuit sizing approaches have been shown using meta-heuristics on trusted simulators. This tool was then proven by its use in design of several cells in a research project. Here, we present the extension to our nested optimization approach that creates a symmetric and well matched layout in every step for every instance in the population of the swarm, that is extracted in our flow to provide feedback to the cost function impacting on the population update for more viable and robust circuits. The layout optimization presented in this DEMO works with Cadence Layout design tools. Our initial focus is, motivated by Industry 4.0, IoT, on cells for signal conditioning electronics with reconfigurability and Self-X features.[1] Abhaya C. Kammara, L.Palanichamy, and A. König, "Multi-Objective optimization and visualization for analog automation", Complex. Intell. Syst, Springer, DOI 10.1007/s40747-016-0027-3, 2016*

ADVANCED SIMULATION OF QUANTUM COMPUTATIONS
Authors:
Zulehner Alwin and Robert Wille, Johannes Kepler University Linz, AT

Timeslots:

- UB01.3 (Tuesday, March 20, 2018 10:30 - 12:30)
- UB06.3 (Wednesday, March 21, 2018 12:00 - 14:00)
- UB10.3 (Thursday, March 22, 2018 12:00 - 14:30)

Abstract: *Quantum computation is a promising emerging technology which allows for substantial speed-ups compared to classical computation. Since physical realizations of quantum computers are in their infancy, most research in this domain still relies on simulations on classical machines. This causes an exponential overhead which current simulators try to tackle with straight forward array-based representations and massive hardware power. There also exist solutions based on decision diagrams (graph-based approaches) that try to tackle the complexity by exploiting redundancies in quantum states and operations. However, they did not get established since they yield speedups only for certain benchmarks. Here, we demonstrate a new graph-based simulation approach which clearly outperforms state-of-the-art simulators. By this, users can efficiently execute quantum algorithms even if the respective quantum computers are not broadly available yet.*

ARCHON: AN ARCHITECTURE-OPEN RESOURCE-DRIVEN CROSS-LAYER MODELLING FRAMEWORK
Authors:
Fei Xia[1], Ashur Rafiev[1], Mohammed Al-Hayanni[2], Alexei Iliasov[1], Rishad Shafik[1], Alexander Romanovsky[1]and Alex Yakovlev[1]
[1]Newcastle University, UK; [2]Newcastle University, UK and University of Technology and HCED, IQ

Timeslots:

- UB01.1 (Tuesday, March 20, 2018 10:30 - 12:30)
- UB02.1 (Tuesday, March 20, 2018 12:30 - 15:00)
- UB10.1 (Thursday, March 22, 2018 12:00 - 14:30)
- UB11.1 (Thursday, March 22, 2018 14:30 - 16:30)

Abstract: *This demonstration showcases a modelling method for large complex computing systems focusing on many-core types and concentrating on the crosslayer aspects. The resource-driven models aim to help system designers reason about, analyse, and ultimately design such systems across all conventional computing and communication layers, from application, operating system, down to the finest hardware details. The framework and tool support the notion of selective abstraction and are suitable for studying such non-functional properties such as performance, reliability and energy consumption.*

CCF: A CGRA COMPILATION FRAMEWORK
Authors:
Shail Dave and Aviral Shrivastava, Arizona State University, US

Timeslots:

- UB05.1 (Wednesday, March 21, 2018 10:00 - 12:00)
- UB09.1 (Thursday, March 22, 2018 10:00 - 12:00)

Abstract: *Coarse-grained reconfigurable array (CGRA) can efficiently accelerate even non-parallel loops. Although scores of techniques have been developed in the past decade to map loops on CGRA PEs, several challenges in enabling acceleration of general-purpose applications on CGRAs remained unresolved, in particular, the automatic code generation for the CGRA accelerator coupled with modern processor cores. In this demonstration, we showcase CCF – CGRA compiler framework. CCF is implemented in LLVM 4.0 and includes a set of transformation and analysis passes. We show that given performance-critical loops annotated in embedded applications, how CCF extracts the loop, constructs the data dependency graph (DDG), maps it onto CGRA architecture, off-loads necessary configuration instructions for CGRA PEs, and automatically communicates data between the CPU and CGRA.*

CIJTAG: CONCURRENT IJTAG DEMONSTRATOR
Author:
Krenz-Baath René, Hamm-Lippstadt University of Applied Sciences, DE

Timeslots:

- UB01.9 (Tuesday, March 20, 2018 10:30 - 12:30)
- UB03.9 (Tuesday, March 20, 2018 15:00 - 17:30)
- UB05.9 (Wednesday, March 21, 2018 10:00 - 12:00)
- UB07.9 (Wednesday, March 21, 2018 14:00 - 16:00)

Abstract: *The flexibility of on-chip instrument access enabled by IEEE 1687 (IJTAG) has shown tremendous improvements in modern industrial designs. Due to a constantly increasing spektrum of tasks performed through 1687 networks such as performing test operations during production test, on-line test operations as well as operating health monitors the test requirements in modern designs increase dramatically with respect to test performance, responsiveness and low power. These requirements have a major impact on the design of such test infrastructures. In complex designs with large test infrastructures it might be challenging to comply with the large spectrum of requirements. Concurrent IJTAG is novel partitioning concept to a reconfigurable test infrastructure in order to enable an independent operation of different sections of the test infrastructure. The proposed demonstrator shows the first FPGA-based implementation of concurrent IJTAG test infrastructures.*

CLAVA-MARGOT: CLAVA + MARGOT = C/C++ TO C/C++ COMPILER AND RUNTIME AUTOTUNING FRAMEWORK
Authors:
João Bispo[1], Davide Gadioli[2], Pedro Pinto[1], Emanuele Vitali[2], Hamid Arabnejad[1], Gianluca Palermo[2], Cristina Silvano[2], Jorge G. Barbosa[1] and João M. P Cardoso[1]
[1]Porto University, PT; [2]Politecnico di Milano (POLIMI), IT

Timeslots:

- UB02.10 (Tuesday, March 20, 2018 12:30 - 15:00)
- UB03.10 (Tuesday, March 20, 2018 15:00 - 17:30)
- UB07.2 (Wednesday, March 21, 2018 14:00 - 16:00)

Abstract: *Current computing platforms consist of heterogeneous architectures. To efficiently target those platforms, compilers can be extend with code transformations and insertion of code to interface to runtime autotuning schemes, which tune application parameters according to: the actual execution, target architecture, and workload. We present an approach consisting of a C/C++ source-to-source compiler (Clava) and an autotuner (mARGOt). They are part of the toolflow of the FET-HPC ANTAREX project and allow parallelization, multiversioning and code transformations in the context of runtime autotuning. mARGOt is an autotuner that allows application adaptation to changing conditions and goals. Clava is a source-to-source compiler to transform C/C++ programs, including code instrumentation and integration with components such as mARGOt. We will demonstrate how to use Clava to integrate the mARGOT autotuner in an example application, and several mARGOt functionalities exposed through a Clava API.*

CODE GENEATION: USING FORMAL METHODS FOR AUTOMATIC PLATFORM-INDEPENDENT CODE GENERATION OF RUN-TIME MANAGEMENT
Authors:
Mohammadsadegh Dalvandi, Michael Butler and Asieh Salehi Fathabadi, University of Southampton, UK

Timeslots:

- UB10.7 (Thursday, March 22, 2018 12:00 - 14:30)
- UB11.7 (Thursday, March 22, 2018 14:30 - 16:30)

Abstract: *Run-Time Management (RTM) systems are used in embedded systems to dynamically adapt hardware performance to minimise energy consumption. In this demonstration, we present a framework for automatic generation of RTM implementations from platform-independent formal models. The methodology in designing the RTM systems uses a high-level mathematical language, Event-B, which can describe systems at different abstraction levels. A code generation tool is used to translate platform-independent Event-B RTM models to platform-specific implementations in C. Formal verification is used to ensure correctness of the Event-B models. The portability offered by our methodology is demonstrated by modelling a Reinforcement Learning (RL) based RTM and generating implementations for two different platforms that all achieve energy savings on the respective platforms. The generated RTM code has been integrated with the PRiME framework, a cross-layer framework for embedded power management.*

CONSTRAINED RANDOM APPLICATION GENERATION FOR FIRMWARE-BASED POWER MANAGEMENT VALIDATION

Authors:
Vladimir Herdt[1], Hoang M. Le[2], Daniel Große[3] and Rolf Drechsler[3]
[1]Universität Bremen, DE; [2]University of Bremen, DE; [3]University of Bremen, DFKI GmbH, DE

Timeslots:

- UB09.3 (Thursday, March 22, 2018 10:00 - 12:00)

Abstract: *Efficient power management (PM) is very important for modern SoCs. To handle the every rising complexity of embedded system design, power aware virtual prototypes (VPs) are employed to enable an early power analysis. Most modern SoCs implement the PM strategy in firmware (FW) due to ease of development. Validation of these strategies at VP level is crucial as undetected flaws will propagate. However, existing validation approaches are based on engineered software (SW), which might miss rare corner cases. We propose a demonstrator based on a novel approach to assess the power-versus-performance trade-off of FW-based PM. Instead of executing real SW applications, our approach makes use of workload scenarios described by a set of constraints to automatically generate SW with a specific power consumption profile. The main novelty is the modeling of scenarios based on constrained random techniques that are very successful in the area of SoC/HW functional validation.*

DISGUISING THE INTERCONNECTS: EFFICIENT PROTECTION OF DESIGN IP

Authors:
Johann Knechtel[1], Satwik Patnaik[2], Mohammed Ashraf[3] and Ozgur Sinanoglu[3]
[1]NYU Abu Dhabi, AE; [2]New York University, US; [3]New York University Abu Dhabi, AE

Timeslots:

- UB03.3 (Tuesday, March 20, 2018 15:00 - 17:30)

Abstract: *Ensuring the trustworthiness and security of electronics has become an urgent challenge in recent years. Among various concerns, the protection of design intellectual property (IP) is to be addressed, due to outsourcing trends for the manufacturing supply chain and malicious end-user. In other words, adversaries either residing in the off-shore fab or in the field may want to obtain and pirate the design IP. As classical design tools do not consider such threats, there is clearly a need for security-aware EDA techniques. Here we present novel but proven techniques for efficient protection of design IP, embedded in an industrial-level design flow using Cadence Innovus. The key idea in our work is that disguising the interconnects is supremely suitable to protect design IP, while inducing only little additional cost and providing strong resilience. We share our customized libraries with the community, and we demonstrate our design flow and its security measures.*

EMBEDDED ACCELERATION OF IMAGE CLASSIFICATION APPLICATIONS FOR STEREO VISION SYSTEMS

Authors:
Mohammad Loni[1], Carl Ahlberg[2], Masoud Daneshtalab[2], Mikael Ekström[2] and Mikael Sjödin[2]
[1]MDH, SE; [2]Mälardalen University, SE

Timeslots:

- UB02.9 (Tuesday, March 20, 2018 12:30 - 15:00)
- UB07.6 (Wednesday, March 21, 2018 14:00 - 16:00)

Abstract: *Autonomous systems are used in a broad range of applications from indoor utensils to medical application. Stereo vision cameras probably are the most flexible sensing way in these systems since they can extract depth, luminance, color, and shape information. However, stereo vision based applications suffer from huge image sizes, computational complexity and high energy consumption. To tackle these challenges, we first developed GIMME2 [1], a high-throughput, and cost efficient FPGA-based stereo vision system. In the next step, we present a novel approximation accelerator which is also compatible with GIMME2. Our accelerator tries to map neural network (NN) based image classification algorithms to FPGA by using DeepMaker which is an evolutionary based module embed in our accelerator that regenerates a near-optimal NN in term of accuracy. Then, the back-end side of DeepMaker maps the generated NN to FPGA. We will demo a GIMME2-based accelerator for image classification applications.*

EVOAPPROX: LIBRARIES AND GENERATORS OF APPROXIMATE CIRCUITS

Authors:
Lukas Sekanina, Zdenek Vasicek and Vojtech Mrazek, Brno University of Technology, CZ

Timeslots:

- UB05.7 (Wednesday, March 21, 2018 10:00 - 12:00)
- UB08.2 (Wednesday, March 21, 2018 16:00 - 18:00)

Abstract: *Our contribution deals with a fully automated functional approximation methodology for combinational digital circuits. We present open libraries of approximate circuits and tools performing desired approximations. Our approach uses a multi-objective genetic programming-based method to automatically design approximate k-bit adders and multipliers (k = 8, 12, 16, 32). All circuits can be downloaded from [1] at the level of a source code (C, Verilog, and Matlab). Several error metrics are pre-calculated and formal guarantees are given in terms of these errors. By means of an interactive web interface the user can easily find the best trade-off between the error and electrical parameters provided for 45/90/180 nm technology process. We will also demonstrate the circuit design flow developed. References: [1] http://www.fit.vutbr.cz/research/groups/ehw/approxlib/*

EWCMS: AN EMBEDDED WALK-CYCLE MONITORING SYSTEM USING BODY AREA COMMUNICATION AND SECURE LOW-POWER DYNAMIC SIGNALING

Authors:
Shahzad Muzaffar[1] and Ibrahim (Abe) M. Elfadel[2]
[1]Masdar Institute, Khalifa University of Science and Technology, AE; [2]Khalifa University of Science and Technology, AE

Timeslots:

- UB04.1 (Tuesday, March 20, 2018 17:30 - 19:30)
- UB08.1 (Wednesday, March 21, 2018 16:00 - 18:00)

Abstract: *The demo presents a novel ultra-low power, embedded, and wearable walk-cycle monitoring system with applications in areas such as healthcare, robotics, sports medicine, physical therapy, prosthesis, and animal sports. Customized shoes with sensors continuously measure the forces, and an electronic digital assistant is used to analyze the acquired measurements in real time by employing an IMU free and self-synchronizing method in order to estimate weight and study motion patterns. To achieve ultra-low power operation, the human body is used as a communication medium between the sensors and the digital assistant. The single-channel behavior of the human body is accommodated with a novel, simple yet robust single-wire signaling technique, Pulsed-Index Communication (PIC), that significantly reduces the system footprint and overall power consumption as it eliminates the need for clock and data recovery. The system prototype has been rigorously and successfully tested.*

EXPERIENCE-BASED AUTOMATION OF ANALOG IC DESIGN
Authors:
Florian Leber and Juergen Scheible, Reutlingen University, DE

Timeslots:

- UB02.4 (Tuesday, March 20, 2018 12:30 - 15:00)
- UB04.10 (Tuesday, March 20, 2018 17:30 - 19:30)
- UB05.10 (Wednesday, March 21, 2018 10:00 - 12:00)
- UB06.10 (Wednesday, March 21, 2018 12:00 - 14:00)
- UB07.10 (Wednesday, March 21, 2018 14:00 - 16:00)
- UB08.10 (Wednesday, March 21, 2018 16:00 - 18:00)
- UB09.10 (Thursday, March 22, 2018 10:00 - 12:00)

Abstract: *While digital design automation is highly developed, analog design automation still remains behind the demands. Previous circuit synthesis approaches, which are usually based on optimization algorithms, do not satisfy industrial requirements. A promising alternative is given by procedural approaches (also known as "generators"): They (a) emulate experts' decisions, thus (b) make expert knowledge re-usable and (c) can consider all relevant aspects and constraints implicitly. Nowadays, generators are successfully applied in analog layout (Pcells, Pycells). We aim at an entire design flow completely based on procedural automation techniques.This flow will consist of procedures for the generation of schematics and layouts for every typical analog circuit class, such as amplifier, bandgap, filter a.s.o. In our presentation we give an overview on such a design flow and we show an approach for capturing an analog circuit designer's strategy as an executable "expert design plan".*

FPGA-BASED HARDWARE ACCELERATOR FOR DRUG DISCOVERY
Authors:
Ghaith Tarawneh, Alessandro de Gennaro, Georgy Lukyanov and Andrey Mokhov, Newcastle University, UK

Timeslots:

- UB03.8 (Tuesday, March 20, 2018 15:00 - 17:30)
- UB10.2 (Thursday, March 22, 2018 12:00 - 14:30)

Abstract: *We present an FPGA-based hardware accelerator for drug discovery, developed during the EPSRC programme grant POETS (EP/N031768/1) in partnership with e-Therapeutics, an Oxford based drug discovery company. e-Therapeutics is pioneering a novel form of drug discovery based on analyzing protein interactome networks (https://www.youtube.com/watch?v=wQFpTtuzrgA). This approach can discover suitable drug candidates much more efficiently compared to wet lab testing but requires considerable computing power, particularly because commodity computers are generally inefficient at analyzing large-scale networks. The presented accelerator, consisting of an FPGA board with a silicon-mapped protein interactome plus accompanying software formalisms and tools, can deliver a 1000x speed up in this application compared to software running on commodity computers. We will showcase demos in which we run in-silico analysis of protein interactomes to test drug effects and visualize the results in real-time.*

GENERATING FULL-CUSTOM SCHEMATICS IN A MIXED-SIGNAL TOP-DOWN DESIGN FLOW
Authors:
Tobias Markus[1], Markus Mueller[2] and Ulrich Bruening[1]
[1]University of Heidelberg, DE; [2]Extoll GmbH, DE

Timeslots:

- UB02.2 (Tuesday, March 20, 2018 12:30 - 15:00)
- UB03.2 (Tuesday, March 20, 2018 15:00 - 17:30)
- UB04.2 (Tuesday, March 20, 2018 17:30 - 19:30)
- UB07.1 (Wednesday, March 21, 2018 14:00 - 16:00)

Abstract: *Design time is one of the precious assets in the cycle of hardware design. The top down methodology has been used in digital designs very successfully and now we also apply it for analog and mixed signal designs. Generating most of the structures automatically saves time and avoids errors. A Top Down Design Flow for Mixed Signal Designs is used which generates the schematic structure from the system RNM representation. Since the structural verilog part of the system level design will automatically generate the schematic structure it is only the functional part which is missing and has to be implemented by the analog designer. Some often used blocks can be used as an entry point to partially generate parts of the design in the schematic and furthermore even parts of the layout. We will demonstrate this design method with an example project.*

HARDENING THE HARDWARE: A REVERSE-ENGINEERING RESILIENT SECURE CHIP
Authors:
Abhrajit Sengupta[1], Muhammad Yasin[2], Mohammed Nabeel[3], Mohammed Ashraf[3], Jeyavijayan Rajendran[4]and Ozgur Sinanoglu[3]
[1]New York University, AE; [2]New York University, US; [3]New York University Abu Dhabi, AE; [4]Texas A&M, US

Timeslots:

- UB03.4 (Tuesday, March 20, 2018 15:00 - 17:30)

Abstract: *With the globalization of integrated circuit (IC) supply chain, the semi-conductor industry is facing a number of threats, such as Intellectual Property (IP) piracy, hardware Trojans, and counterfeiting. To defend against such threats at the hardware level, logic locking was proposed as a promising countermeasure. Yet, several recent attacks have completely undermined its security by successfully retrieving the secret key. Here, we present stripped-functionality logic locking (SFLL), which resists all existing attacks by hiding a part of the functionality in the form of a secret key. We leverage security-aware synthesis to develop a computer-aided design (CAD) framework that meets the desired security criterion at a minimal cost of 5%, 0.5%, and 8% for power, performance, and area, respectively. Moreover, we taped out a chip, the first such prototype of its kind, by applying our technique on an industry level processor, namely, ARM Cortex-M0 microprocessor in 65nm technology.*

IIDEAA: DESIGN SPACE EXPLORATION FOR FUNCTIONAL-LEVEL APPROXIMATION
Authors:
Marcello Traiola[1], Mario Barbareschi[2], Marcello Traiola[3] and Alberto Bosio[3]
[1]LIRMM, FR; [2]DIETI - University of Naples Federico II, IT; [3]LIRMM - University of Montpellier / CNRS, FR

Timeslots:

- UB01.7 (Tuesday, March 20, 2018 10:30 - 12:30)

Abstract: *Approximate Computing (AxC) aims at enabling the production of computing systems which can satisfy the rising performance demands and can improve the energy efficiency. AxC exploits the gap between the level of accuracy required by the users and the precision provided by the computing system, for achieving diverse optimizations. Various AxC techniques have been proposed so far for several applications and, unfortunately, existing approaches are application specific and a general and systematic methodology to automatically define approximate algorithms is still an open challenge. In this works we introduce a methodology which makes use of mutation techniques to obtain approximate versions of a given application described as a C/C++ code. We designed and implemented IIDEAA, an automatic tool exploiting (i) a source-to-source manipulation technique and (ii) an Evolutionary search engine, in order to search for the best functional approximation version of the given C/C++ code.*

IIP GENERATORS TO EASE ANALOG IC DESIGN
Authors:
Benjamin Prautsch, Uwe Eichler and Torsten Reich, Fraunhofer Institute for Integrated Circuits IIS/EAS, DE

Timeslots:

- UB01.8 (Tuesday, March 20, 2018 10:30 - 12:30)
- UB07.8 (Wednesday, March 21, 2018 14:00 - 16:00)
- UB09.8 (Thursday, March 22, 2018 10:00 - 12:00)
- UB10.8 (Thursday, March 22, 2018 12:00 - 14:30)

Abstract: *Semiconductor technology has shown significant progress over the last decades. Digital EDA (electronic design automation) allowed that this progress could be converted to high-performance digital ICs. Analog components are part of Systems-on-Chip (SoC) too, but analog EDA lags far behind. Therefore, a lot of effort was spent to automate analog IC design. Mayor results are constraint-based layout-aware optimization tools using predefined layout templates or pure automation as well as analog generators containing expert knowledge. While optimization is a holistic top-down approach, generators allow parameterized and fast bottom-up generation of critical schematic and layout parts, pre-planned by experienced designers. With IIP Generators, we follow three use cases to ease analog design: 1) design on higher hierarchy levels, 2) development of hierarchical high-level IIPs, and 3) automated design porting due to highly technology-independent blocks down to 22nm.*

OISC MULTICORE STENCIL PROCESSOR: ONE INSTRUCTION-SET COMPUTER-BASED MULTICORE PROCESSOR FOR STENCIL COMPUTING
Authors:
Kaoru Saso[1], Jingyuan Zhao[2] and Yuko Hara-Azumi[2]
[1]School of Engineering, Tokyo Institute of Technology, JP; [2]Tokyo Institute of Technology, JP

Timeslots:

- UB02.3 (Tuesday, March 20, 2018 12:30 - 15:00)
- UB05.3 (Wednesday, March 21, 2018 10:00 - 12:00)
- UB07.3 (Wednesday, March 21, 2018 14:00 - 16:00)
- UB11.3 (Thursday, March 22, 2018 14:30 - 16:30)

Abstract: *Subtract and Branch on NEGative with 4 operands (SUBNEG4) is one of One Instruction-Set Computers that execute only one type of instruction. Thanks to its simplicity, SUBNEG4 has only 1/20x circuit area and 1/10x power consumption against MIPS processor. As SUBNEG4 is Turing-complete, it is suitable for parallel computing by multiple cores, while keeping its low-power feature. Our on-going project is seeking for effective use and deployment of SUBNEG4 cores on embedded systems. Our booth will demonstrate the significant speed-up by a SUBNEG4-based many-core processor against a conventional processor, for stencil computing. Our 64-core processor efficiently handles 2D von-Neumann neighborhood stencils, e.g., wave simulation by Verlet integration and 2D Jacobi iteration, to compute 64 points simultaneously. We show that small many-core processors can be realized even with such large number of cores while achieving good speed-up for heaving computation.*

OTPG: SPECIFICATION-BASED CONSTRUCTION OF ONLINE TPGS FOR MICROPROCESSORS
Authors:
Mikhail Chupilko, Alexander Kamkin and Andrei Tatarnikov, ISP RAS, RU

Timeslots:

- UB01.4 (Tuesday, March 20, 2018 10:30 - 12:30)
- UB04.4 (Tuesday, March 20, 2018 17:30 - 19:30)
- UB09.7 (Thursday, March 22, 2018 10:00 - 12:00)

Abstract: *This work presents an approach to construction of online test program generators (TPGs). The approach is intended to use specifications of ISA presented in nML/mmuSL specification languages. They are processed by a meta-generator to obtain their binary representations supplied with meta information and a test generation core compatible with the target microprocessor. The test generation core is loaded as a binary image into the target microprocessor's memory (for experiments we're using QEMU for MIPS) and produces test cases to be processed (incl. results checking) by an executor. It should be noticed that the meta-generator and the executor are not obligatory run at the same microprocessor (especially, if it is highly incomplete). The final goal of the project is to propose a method of obtaining online TPGs for a wide range of ISAs, and to develop a mature tool implementing this method.*

POWER-AWARE SOFTWARE MAPPING OF PARALLEL APPLICATIONS ONTO HETEROGENEOUS MPSOCS
Authors:
Gereon Onnebrink and Rainer Leupers, RWTH Aachen University, DE

Timeslots:

- UB09.4 (Thursday, March 22, 2018 10:00 - 12:00)

Abstract: *Heterogeneous multi- and many-processor systems-on-chip provide the best trade-o between performance, cost, and power. One of the biggest hurdles to exploit multicore architectures from the SW side. Considering an application that has been properly partitioned into multiple concurrent tasks, and programmed in a parallel language, the process of mapping those tasks onto the processors with optimal DVFS is a huge challenge for a certain design goal. An automatic approach is needed that determines the optimal decision. A great amount of research has been conducted aiming to optimise the performance of a parallelised application. Another research track is the ESL power estimation methodology. Combining both, a novel power-aware software mapping heuristic has been implemented to develop performance and power co-optimized parallel software. This algorithm can be used to identify the gain of sophisticated power management techniques by providing the power-performance trade-off.*

PRIME: PLATFORM- AND APPLICATION-AGNOSTIC RUN-TIME POWER MANAGEMENT OF HETEROGENEOUS EMBEDDED SYSTEMS
Authors:
Domenico Balsamo, Graeme M. Bragg, Charles Leech and Geoff V. Merrett, University of Southampton, UK

Timeslots:

- UB02.7 (Tuesday, March 20, 2018 12:30 - 15:00)
- UB04.3 (Tuesday, March 20, 2018 17:30 - 19:30)
- UB06.7 (Wednesday, March 21, 2018 12:00 - 14:00)

Abstract: *Increasing energy efficiency and reliability at runtime is a key challenge of heterogeneous many-core systems. We demonstrate how contributions from the PRiME project integrate to enable application- and platform-agnostic runtime management that respects application performance targets. We consider opportunities to enable runtime management across the system stack and we enable cross-layer interactions to trade-off power and reliability with performance and accuracy. We consider a system as three distinct layers, with abstracted communication between them, which enables the direct comparison of different approaches, without requiring specific application or platform knowledge. Application-agnostic runtime management is demonstrated with a selection of runtime managers from PRiME, including linear regression modelling and predictive thermal management, operating across multiple applications. Platform-independent runtime management is demonstrated using two heterogeneous platforms.*

RECONFIGURABLE SELF-TIMED DATAFLOW ACCELERATOR
Authors:
Danil Sokolov, Alessandro de Gennaro and Andrey Mokhov, Newcastle University, UK

Timeslots:

- UB03.5 (Tuesday, March 20, 2018 15:00 - 17:30)
- UB10.5 (Thursday, March 22, 2018 12:00 - 14:30)

Abstract: *Many applications require reconfigurable pipelines to handle incoming data items differently depending on their values or the operating mode. Currently, reconfigurable synchronous pipelines are the mainstream of dataflow accelerators. However, there are certain advantages to be gained from self-timed dataflow processing, e.g. robustness to unstable power supply, data-dependent performance, etc. To become attractive for industry, reconfigurable asynchronous pipelines need a formal behavioural model and design automation. This demo will present a design flow for the specification, verification and synthesis of reconfigurable self-timed pipelines using Dataflow Structure formalism in Workcraft(https://workcraft.org/). As a case study we will use an asynchronous accelerator for Ordinal Pattern Encoding(OPE) with reconfigurable pipeline depth. We will exhibit the resultant OPE chip fabricated in TSMC90nm to show the benefits of reconfigurability and asynchrony for dataflow processing.*

REPABIT: AUTOMATED DESIGN OF RELOCATABLE PARTIAL BITSTREAMS
Authors:
Jens Rettkowski[1] and Diana Göhringer[2]
[1]Ruhr-University Bochum, DE; [2]Technische Universität Dresden, DE

Timeslots:

- UB05.8 (Wednesday, March 21, 2018 10:00 - 12:00)

Abstract: *Dynamic partial reconfiguration of FPGAs enables the replacement of hardware modules at runtime without disturbing remaining hardware modules. The standard vendor tools generate a specific partial bitstream for each reconfigurable region. Relocation generates a partial bitstream in such a way, that it can be moved to different regions. Hence, the number and the time to generate bitstreams is reduced. In this work, RePaBit is presented that automates the generation of relocatable partial bitstreams for Xilinx Vivado. TCL scripts check the compatibility of resource footprints and arrange identical partition pins in all regions for the connection of relocatable modules with the remaining design. Feedthrough routes are avoided using the isolation design flow from Xilinx. The results show an overhead of LUTs by 0.7% and a frequency reduction of only 1.5%. Nevertheless, RePaBit simplifies the design and reduces the design time as well as the needed memory for storing the partial bitstreams.*

RISC-V PROCESSOR MODELING IN IP-XACT USING KACTUS2
Authors:
Esko Pekkarinen and Timo Hämäläinen, Tampere University of Technology, FI

Timeslots:

- UB02.8 (Tuesday, March 20, 2018 12:30 - 15:00)
- UB06.8 (Wednesday, March 21, 2018 12:00 - 14:00)
- UB10.4 (Thursday, March 22, 2018 12:00 - 14:30)

Abstract: *The complexity of modern embedded system design is managed by advanced, high-level design methodologies such as IP-XACT. However, integrating IP-XACT as a part of an existing design flow and packaging legacy sources is too often inhibited by the inherit differences between IP-XACT and the traditional hardware description languages. In this work, we take an existing Verilog implementation of a RISC-V microprocessor and package it with our open-source IP-XACT tool Kactus2. The resulting IP-XACT description will be publicly available and based on the modeling experience we report the observed pitfalls in the transition from HDL to IP-XACT.*

ROS X FPGA FOR ROBOT-CLOUD SYSTEM: ROBOT-CLOUD COOPERATIVE VISUAL SLAM PROCESSING USING ROS-COMPLIANT FPGA COMPONENT

Authors:
Takeshi Ohkawa, Yuhei Sugata, Aoi Soya, Kanemitsu Ootsu and Takashi Yokota, Utsunomiya University, JP

Timeslots:

- UB05.4 (Wednesday, March 21, 2018 10:00 - 12:00)
- UB06.4 (Wednesday, March 21, 2018 12:00 - 14:00)
- UB07.4 (Wednesday, March 21, 2018 14:00 - 16:00)
- UB08.4 (Wednesday, March 21, 2018 16:00 - 18:00)

Abstract: *Distributed processing in robot-cloud cooperative system is discussed in terms of processing performance and communication performance. Cooperation of robots and cloud-servers is inevitable for realizing intelligent robots in the next generation society and industry. To improve processing performance of the cooperative system, we utilize ROS-compliant FPGA component as a robot-side embedded processing for low-power and high-performance image processing. We prepare two demonstrations. (1) Key-point Detection from camera image using Fully-hardwired ROS-Compliant FPGA component In the evaluation, the processing performance of the component is almost same as PC, while it operates at more than 10 times less power (5W), compared to PC (50W). (2) Distributed Visual SLAM using two-wheeled robot (TurtleBot3) Distributed Visual SLAM (Simultaneous Localization and Mapping) are presented as a concrete example of the robot-cloud cooperative system.*

SPANNER: SELF-REPAIRING SPIKING NEURAL NETWORK CONTROLLER FOR AN AUTONOMOUS ROBOT

Authors:
Alan Millard[1], Anju Johnson[1], James Hilder[1], David Halliday[1], Andy Tyrrell[1], Jon Timmis[1], Junxiu Liu[2], Shvan Karim[2], Jim Harkin[2] and Liam McDaid[2]
[1]University of York, UK; [2]Ulster University, UK

Timeslots:

- UB03.6 (Tuesday, March 20, 2018 15:00 - 17:30)
- UB05.6 (Wednesday, March 21, 2018 10:00 - 12:00)
- UB11.6 (Thursday, March 22, 2018 14:30 - 16:30)

Abstract: *The human brain is remarkably resilient, and is able to self-repair following injury or a stroke. In contrast, electronic systems typically exhibit limited self-repair capabilities, and cannot recover from faults. We demonstrate a bio-inspired approach to self-repair that allows an autonomous robot to recover from faults in its artificial 'brain'. Astrocytes are support cells in the human brain that interact with neurons to regulate synaptic activity. We have modelled this interaction to create a spiking neural network that can self-repair when synapses between neurons are damaged, by strengthening redundant pathways. We demonstrate a robot platform controlled by a self-repairing spiking neural network that is implemented on an FPGA. We demonstrate that injecting faults into the synapses of the network initially causes the robot to behave erratically, but that the neural controller is able to automatically repair itself, thus allowing the robot to resume normal function.*

SYSTEM-LEVEL OPERATING CONDITION CHECKS: AUTOMATED AUGMENTATION OF VERILOGAMS MODELS

Authors:
Georg Gläser[1], Martin Grabmann[1], Gerrit Kropp[1] and Andreas Fürtig[2]
[1]Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH, DE; [2]Goethe University Frankfurt, DE

Timeslots:

- UB06.1 (Wednesday, March 21, 2018 12:00 - 14:00)

Abstract: *Analog/Mixed-Signal design and verification strongly relies on more or less abstract models to make extensive simulations feasible. Maintaining consistent behavior between system model and implementation is crucial for a correct verification. This also involves the operating conditions: A faulty model might introduce false-positive verification results despite of e.g. an incorrect supply voltage or missing bias currents. We present an automated workflow for extracting these checks from a transistor-level implementation and transfer it into a given Verilog-AMS model. The correctness of our approach is proved by evaluating the model coverage between the implementation and the model. As a demonstration scenario, we use a demodulator component of a HF RFID communication system. We extract the acceptance region from the transistor-level schematic and automatically generate and integrate a model safe-guard unit for performing the operating condition check.*

T-CREST: THE OPEN-SOURCE REAL-TIME MULTICORE PROCESSOR

Authors:
Martin Schoeberl, Luca Pezzarossa and Jens Sparsø, Technical University of Denmark, DK

Timeslots:

- UB03.7 (Tuesday, March 20, 2018 15:00 - 17:30)
- UB04.7 (Tuesday, March 20, 2018 17:30 - 19:30)
- UB07.7 (Wednesday, March 21, 2018 14:00 - 16:00)
- UB08.7 (Wednesday, March 21, 2018 16:00 - 18:00)

Abstract: *Future real-time systems, such as advanced control systems or real-time image recognition, need more powerful processors, but still a system where the worst-case execution time (WCET) can be statically predicted. Multicore processors are one answer to the need for more processing power. However, it is still an open research question how to best organize and implement time-predictable communication between processing cores. T-CREST is an open-source multicore processor for research on time-predictable computer architecture. In consists of several Patmos processors connected by various time-predictable communication structures: access to shared off-chip, access to shared on-chip memory, and the Argo network-on-chip for fast inter-processor communication. T-CREST is supported by open-source development tools, such as compilation and WCET analysis. To best of our knowledge, T-CREST is the only fully open-source architecture for research on future real-time multicore architectures.*

TOPOLINANO & MAGCAD: A DESIGN AND SIMULATION FRAMEWORK FOR THE EXPLORATION OF EMERGING TECHNOLOGIES
Authors:
Umberto Garlando and Fabrizio Riente, Politecnico di Torino, IT

Timeslots:

- UB01.2 (Tuesday, March 20, 2018 10:30 - 12:30)
- UB03.1 (Tuesday, March 20, 2018 15:00 - 17:30)
- UB05.2 (Wednesday, March 21, 2018 10:00 - 12:00)
- UB06.2 (Wednesday, March 21, 2018 12:00 - 14:00)
- UB09.2 (Thursday, March 22, 2018 10:00 - 12:00)

Abstract: *We developed a design framework that enables the exploration and analysis of emerging beyond-CMOS technologies. It is composed of two powerful tools: ToPoliNano and MagCAD. Different technologies are supported, and new ones could be added thanks to their modular structure. ToPoliNano starts from a VHDL description of a circuit and performs the place&route following the technological constraints. The resulting circuit can be simulated both at logical or physical level. MagCAD is a layout editor where the user can design custom circuits, by placing basic elements of the selected technology. The tool can extract a VHDL netlist based on compact models of placed elements derived from experiments or physical simulations. Circuits can be verified with standard VHDL simulators. The design workflow will be demonstrated at the U-booth to show how those tools could be a valuable help in the studying and development of emerging technologies and to obtain feedbacks from the scientific community.*

TTOOL/OMC: OPTIMIZED COMPILATION OF EXECUTABLE UML/SYSML DIAGRAMS FOR THE DESIGN OF DATA-FLOW APPLICATIONS
Authors:
Andrea Enrici[1], Julien Lallet[1], Renaud Pacalet[2] and Ludovic Apvrille[2]
[1]Nokia Bell Labs, FR; [2]Telecom ParisTech, FR

Timeslots:

- UB02.6 (Tuesday, March 20, 2018 12:30 - 15:00)
- UB06.6 (Wednesday, March 21, 2018 12:00 - 14:00)
- UB10.6 (Thursday, March 22, 2018 12:00 - 14:30)

Abstract: *Future 5G networks are expected to increase data rates by a factor of 10x. To meet this requirement, baseband stations will be equipped with both programmable (e.g., CPUs, DSPs) and reconfigurable components (e.g., FPGAs). Efficiently programming these architectures is not trivial due to the inner complexity and interactions of these two types of components. This raises the need for unified design flows capable of rapidly partitioning and programming these mixed architectures. Our demonstration will show the complete system-level design and Design Space Exploration, based on UML/SysML diagrams, of a 5G data-link layer receiver, that is partitioned onto both programmable and reconfigurable hardware. We realize an implementation of such a UML/SysML design by compiling it into an executable C application whose memory footprint is optimized with respect to a given scheduling. We will validate the effectiveness of our solution by comparing automated vs manual designs.*

VIRTUAL PROTOTYPE MAKANI: ANALYZING THE USAGE OF POWER MANAGEMENT TECHNIQUES AND EXTRA-FUNCTIONAL PROPERTIES BY USING VIRTUAL PROTOTYPING
Author:
Sören Schreiner, OFFIS – Institute for Information Technology, DE

Timeslots:

- UB01.10 (Tuesday, March 20, 2018 10:30 - 12:30)
- UB05.5 (Wednesday, March 21, 2018 10:00 - 12:00)
- UB09.5 (Thursday, March 22, 2018 10:00 - 12:00)

Abstract: *My Phd work consists of analyzing the correct usage of power management techniques, as well as the analysis of extra-functional properties, including power and timing properties, in MPSoCs. Especially in safety-critical environments the power management gets safety-critical too, since it is able to influence the overall system behavior. To demonstrate my methodologies a mixed-critical multi-rotor system and its corresponding virtual prototype is used. The multi-rotor system's avionics is served by a Xilinx Zynq 7000 MPSoC. The hardware architecture includes ARM and MicroBlaze cores, a NoC for communication and peripherals. The MPSoC processes the flight algorithms with triple modular redundancy and a mission-critical video processing task. The virtual prototype consists of a virtual platform and an environmental model. The virtual platform is equipped with my measuring tool libraries to generate traces of the observed power management techniques and the extra-functional properties.*

WARE: WEARABLE ELECTRONICS DIRECTIONAL AUGMENTED REALITY
Authors:
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[1]University of Verona, IT; [2]EDALab Srl, IT; [3]Wagoo LLC, IT; [4]Wagoo Italia srls, IT

Timeslots:

- UB01.6 (Tuesday, March 20, 2018 10:30 - 12:30)
- UB08.6 (Wednesday, March 21, 2018 16:00 - 18:00)
- UB09.6 (Thursday, March 22, 2018 10:00 - 12:00)

Abstract: *Augmented Reality (AR) currently require large form factors, weight, cost and frequent recharging cycles that reduce usability. Connectivity, image processing, localization, and direction evaluation lead to high processing and power requirements. A multi-antenna system, patented by the industrial partner, enables a new generation of smart eye-wear that elegantly requires less hardware, connectivity, and power to provide AR functionalities. They will allow users to directionally locate nearby radio emitting sources that highlight objects of interest (e.g., people or retail items) by using existing standards like Bluetooth Low Energy, Apple's iBeacon and Google's Eddystone. This booth will report the current level of research addressed by the Computer Science Department of University of Verona, Wagoo LLC, and Wagoo Italia srls. In the presented demo, different objects emit an "I am here" signal and a prototype of the smart glasses shows the information related to the observed object.*

WIRELESS SENSOR SYSTEM WITH ELECTROMAGNETIC ENERGY HARVESTER FOR INDUSTRY 4.0 APPLICATIONS

Authors:
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[1]Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS), DE; [2]Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH, DE

Timeslots:

- UB06.5 (Wednesday, March 21, 2018 12:00 - 14:00)
- UB07.5 (Wednesday, March 21, 2018 14:00 - 16:00)
- UB08.5 (Wednesday, March 21, 2018 16:00 - 18:00)

Abstract: *An energy-autonomous and adaptive wireless multi-sensor system for a wide range of Industry 4.0 applications is presented here. By taking a holistic view of the sensor system and of the specific interactions of its components, technological barriers of individual system elements can be overcome. The energy supply of the demonstrator is realized by an miniaturized electromagnetic energy harvester, which could be easily and quickly adapted to the application-specific boundary conditions with the help of a computer assisted design process. Variations in the available energy are monitored by advanced energy management functions. The modular hardware and software platform is demonstrated by an adaptive measurement and data transmission rate. Communication takes place by means of industry 4.0 compliant standard protocols. The demonstrator was developed in the research group Green-ISAS funded by the Free State of Thuringia from the European Social Fund (ESF) under grant no. 2016 FGR 0055.*

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