DATE Best Paper Awards

Each year the Design, Automation and Test in Europe Conference presents awards to the authors of the best papers. The selection is performed by the award committee.

The **DATE 2018** best papers are:

D Track

Efficient Verification Of Multi-Property Designs (The Benefit Of Wrong Assumptions)

Eugene Goldberg[1], *Matthias Gudemann*[1], *Daniel Kroening*[1], *Rajdeep Mukherjee*[2]
1 DiffBlue, 2 Oxford University

A Track

MATIC: Learning Around Errors for Efficient Low-Voltage Neural Network Accelerators

Sung Kim, Patrick Howe, Thierry Moreau, Armin Alaghi, Luis Ceze and Visvesh Sathe
University of Washington

T Track

Low-Cost High-Accuracy Variation Characterization for Nanoscale IC Technologies via Novel Learning-based Techniques

Zhijian Pan[1], *Miao Li*[2], *Jian Yao*[2] , *Hong Lu*[2] , *Zuochang Ye*[1] , *Yanfeng Li*[2] , *Yan Wang*[1]
1 Tsinghua University, 2 Platform Design Automation, Inc.

E Track

Buffer-aware bounds to multi-point progressive blocking in priority-preemptive NoCs

Leandro Indrusiak[1], *Alan Burns*[2], *Borislav Nikolic*[3]
1 University of York, 2 University of York, 3 CISTER/INESC-TEC, ISEP, IPP

Best Paper Award Nominations

D track

HVSM: Hardware-Variability Aware Streaming Processors' Management Policy in GPUs
Jingweijia Tan, Kaige Yan
Jilin University

Sensei: An Area-Reduction Advisor for FPGA High-Level Synthesis
Hsuan Hsiao, Jason H. Anderson
University of Toronto

Multi-Bit Non-Volatile Spintronic Flip-Flop
Christopher Münch, Rajendra Bishnoi, Mehdi Tahoori
Karlsruhe Institute of Technology

Trident: A Comprehensive Timing Error Resilient Technique against Choke Points at NTC
Aatreyi Bal, Sanghamitra Roy, Koushik Chakraborty
Utah State University

An Inside Job: Remote Power Analysis Attacks on FPGAs
Falk Schellenberg[1] , Dennis Gnad[2], Amir Moradi[1], Mehdi Tahoori[2]
1 Ruhr University Bochum, 2 Karlsruhe Institute of Technology

Compact Modeling of Carbon Nanotube Thin Film Transistors for Flexible Circuit Design
Leilai Shao[1], Tsung-Ching Huang[2], Ting Lei[3], Zhenan Bao[3], Raymond Beausoleil[2], Tim Cheng[4]
1 University of California Santa Barbara, 2 Hewlett Packard Labs,
3 Stanford University, 4 Hong Kong University of Science and Technology

CAMP: Accurate Modeling of Core and Memory Locality for Proxy Generation of Big-data Applications
Reena Panda, Xinnian Zheng, Andreas Gerstlauer, Lizy John
University of Texas at Austin

HME: A Lightweight Emulator for Hybrid Memory
Zhuohui Duan, Haikun Liu, Xiaofei Liao
Huazhong University of Science and Technology

FFT-Based Deep Learning Deployment in Embedded Systems
Sheng Lin[1], Ning Liu[1], Mahdi Nazemi[2], Hongjia Li[1], Caiwen Ding[1], Yanzhi Wang[2], Massoud Pedram[2]
1 Syracuse University, 2 University of Southern California

A Faithful Binary Circuit Model with Adversarial Noise

Matthias Fuegger[1], Jürgen Maier[2], Robert Najvirt[2], Thomas Nowak[3], Ulrich Schmid[2]
1 LSV, CNRS & ENS Paris-Saclay, 2 TU Wien, 3 Université Paris Sud

A track

HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing

Tianhao Huang; Guohao Dai; Yu Wang; Huazhong Yang
Tsinghua University

GIS-Based Optimal Photovoltaic Panel Floorplanning for Residential Installations

Sara Vinco; Lorenzo Bottaccioli, Edoardo Patti, Andrea Acquaviva, Enrico Macii, Massimo Poncino
Politecnico di Torino

A Fast and Resource Efficient FPGA Implementation of Secret Sharing for Storage Applications

Jakob Stangl[1] , Thomas Lorünser[2], Sai Dinakarrao[1]
1 TU Wien, 2 Austrian Institute of Technology