A High Performance SEU-Tolerant Latch for Nanoscale CMOS Technology

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***Abstract*—This paper presents a high performance latch to tolerate radiation-induced single event upset in 45 nm CMOS technology. The latch can improve robustness by masking the soft errors utilizing Muller C-element and dual modular redundancy hardening. The power dissipation, propagation delay and reliability of the presented SEU-tolerant latch are analyzed by SPICE simulations. The results show that the presented latch provides a higher robustness and lower power-delay product than classical implementations and alternative hardened solutions.**

***Index Terms*—Transient fault, soft error, single event upset, hardened-by-design, C-element.**

I. INTRODUCTION

WITH CONTINUOUS technology scaling, supply voltage and node capacitance scale correspondingly which leads to great reduction of critical charge of internal nodes. So logic designs are becoming more vulnerable to single event upsets (SEU) [1]. Soft errors used to be a concern only for space and aero applications. As the process technology goes to nanoscale, soft errors have become an important issue at ground level as well. As we know, there are several radiation mechanisms which induce the soft errors at ground level: Alpha particles, high energy neutrons, high-energy cosmic radiation and low-energy cosmic neutron interactions with the IC materials. Although the length of the ion track and the charge cloud induced by an incident ion on silicon has remained constant, the multiple node charge collection and increasing density induce increasing soft error rate [2]. Negative bias temperature instability also increases the cross-section of the single event which leads to an increase in soft error rate [3].

In this paper, a high performance SEU-tolerance latch for nanoscale CMOS technology is presented. It will be hereinafter referred to as High Performance SEU-Tolerant (HPST) Latch. HPST latch is derived from the basic structure which has been introduced in [4]. HPST latch features a lower vulnerability to SEU than scheme in [5], [6] and [7]. HPST latch utilize redundant feedback lines and Muller C-element to mask SEUS to achieve equivalent robustness of classical TMR latch. Extensive SPICE-based fault injection simulations have been performed to evaluate and compare the reliability of various radiation hardened by design latch. The HPST latch provides lower power-delay product than schemes in [4], [5], [6] and [7] by clock gating the Muller C-element at the output. HPST latch achieve a tradeoff between performance, power and reliability.

The rest of the paper is organized as follows: Section II reviews previous hardened latches. Section III presents the principle and implementation of the proposed HPST latch. Section IV includes evaluation and comparison to various radiation hardened by design scheme. Finally, some conclusions are drawn in Section V.

II. PREVIOUS HARDENED LATCHES

There have been various kinds of SEU-tolerant latch. This section reviews TMR-latch, FERST Latch [4], DICE latch [5], Cascode Schmitt Trigger Latch [6], Separate Dual Transistor Latch [7] and Schmitt trigger inverter based latch [8].

A. TMR Latch

Triple Modular Redundancy (TMR) latch is the most commonly used latch in aerospace applications for its high reliability. In Fig.1, The circuit structure of TMR latch is depicted. TMR latch includes three identical static latches and a majority voter. TMR latch can tolerate SEU occurring in one of the identical static latches and provide complete soft error

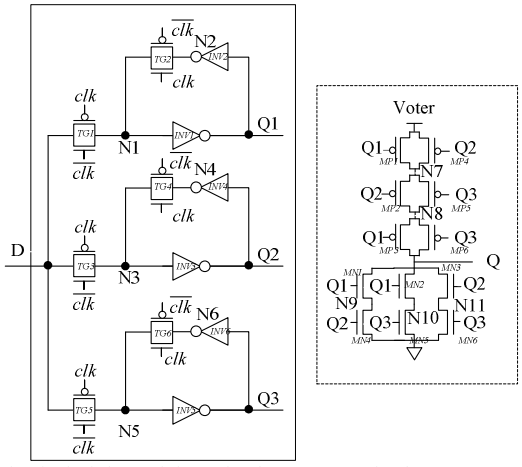

Fig. 1. Classical triple modular redundancy (TMR) latch

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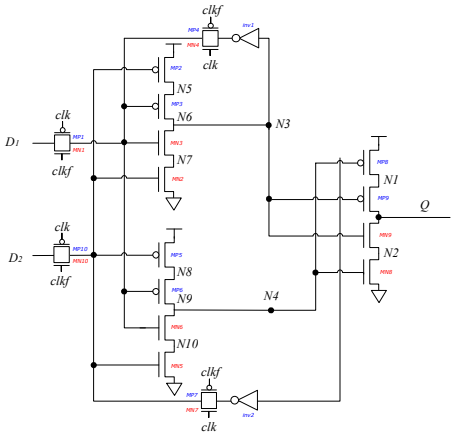

Fig. 2. Feedback redundant SEU-tolerant latch (FERST) latch

immunity. TMR latch always incurs great area overhead and power dissipation which is unacceptable in most designs.

B. *FERST Latch*

Feedback redundant SEU-tolerant latch (FERST) latch is proposed in [4].The circuit structure of FERST latch is shown in Fig.2. To mask the SEUs occurring in the internal nodes of the FERST latch, a redundant feedback path and a filtering circuit called Muller C-element are introduced. When SEU occurs, the two inputs of the Muller C-element are different, the output of the Muller C-element will keep unchanged to mask the SEU. FERST latch also incurs performance penalty because there are two C-element on the datapath from input D to output

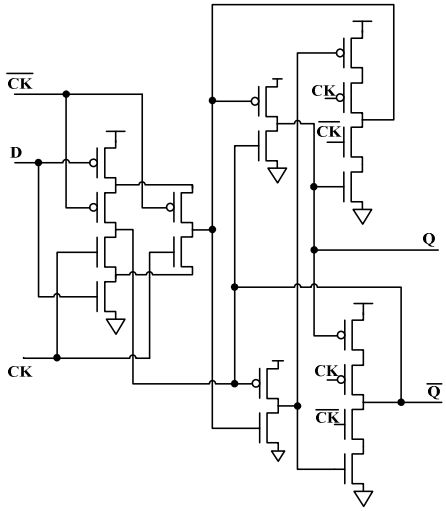

Fig. 3. Dual interlocked storage cell (DICE)

Q. The logic function of C-element is the same as inverter with a larger delay.

C. *DICE Latch*

Dual interlocked storage cell (DICE) is proposed in [5]. The circuit structure of DICE is shown in Fig.3. There are four redundant nodes in the DICE and two pairs of them hold its memory state. The DICE latch can change only when both nodes are upset at the same time. The main drawback of DICE latch is that it is only efficient for low energy particle strikes. The output of DICE latch will upset in case of high energy

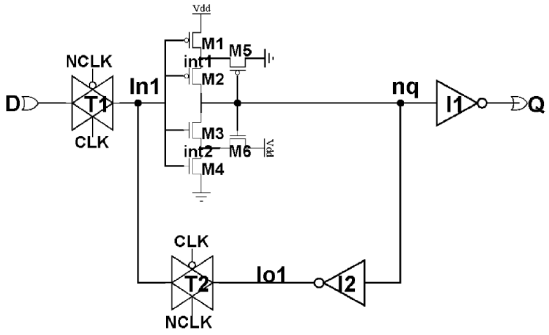

Fig. 4. Cascode Schmitt trigger (CST) latch

particle strikes because the pMOS and nMOS are separated so that they can not act as a filter.

D. *Cascode Schmitt Trigger Latch*

Cascode Schmitt trigger (CST) latch is proposed in [6]. The circuit of CST latch is shown in Fig.4. The CST latch includes

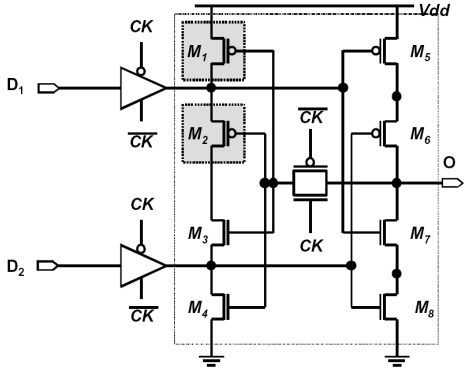

Fig. 5. Separate dual transistor (SDT) Latch

a cascode Schmitt trigger and a feedback loop. The Schmitt trigger has a large hysteresis property in voltage so that it can mask a transient pulse on the input. The feedback loop consists of an inverter I2 and a clock-controlled transmission gate T2. The CST latch has low power dissipation so that it is suitable for low power designs. The CST latch also has the drawback that it can not tolerate high energy particle strikes.

E. *Separate Dual Transistor Latch*

Separated Dual Transistor (SDT) latch is proposed in [7]. The circuit structure of SDT latch is shown in Fig.5. SDT

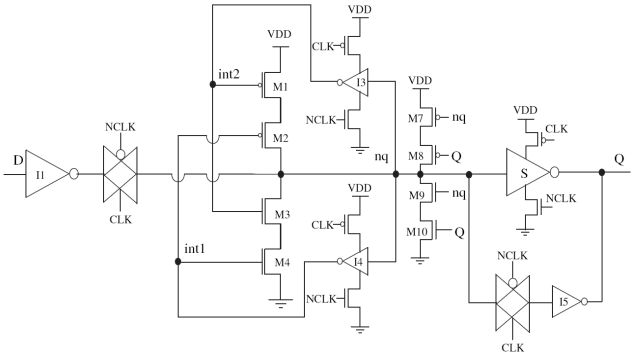

Fig. 6. Schmitt trigger inverter (STI) based latch

latch derived from standard static latch by replacing inverter with C-element. SDT latch separate the feedback lines of the latch both at the start and end points. Both nMOS and pMOS transistor are duplicated to generate two identical distinct output. The drawback of SDT latch is that upset at the output can not be tolerated.

F. Schmitt trigger inverter based latch

Schmitt trigger inverter based (STI) latch is proposed in [8]. The circuit structure of STI latch is shown in Fig.6. STI latch includes Schmitt trigger inverter, clock controlled inverters and voltage comparator. STI latch provides full nodes protection against soft error taking advantage of the hysteresis property of Schmitt trigger inverter. The voltage comparator can recover the upset node.

III. PROPOSED SEU-TOLERANT LATCH

In this section, the high performance SEU-tolerance（HPST）latch are proposed and analyzed.

A. Circuit Structure and Behavior

The SEU tolerance relies on the dual interlocked schemes with internal feedback lines and Muller C-element. The circuit structure of the proposed HPST latch is shown in Fig.7.

The HPST latch is symmetric and dual interlocked. There are three Muller C-elements in the proposed HPST latch: CE1, CE2 and CE3. CE1 consists of MP2, MP3, MN2 and MN3. CE2 consists of MP5, MP6, MN5 and MN6. CE3 consists of MP8, MP9, MPCG, MN8, MN9 and MNCG. CE3 is clocked C-element. CE1 and CE2 act as keeper to keep the correct logic value when the HPST latch is not transparent. CE1 and CE2 can mask the radiation-induced SEU occurred in the internal nodes. CE3 can block the SEU when the latch is not transparent. CE3 turns OFF to reduce power dissipation when the latch is transparent.

When CLK is ‘0’, transmission gates TG1, TG2 and TG3 turn ON and the HPST latch is transparent. CE 3 is clocked Muller C-element. MPCG and MNCG turn OFF, so CE3 turns

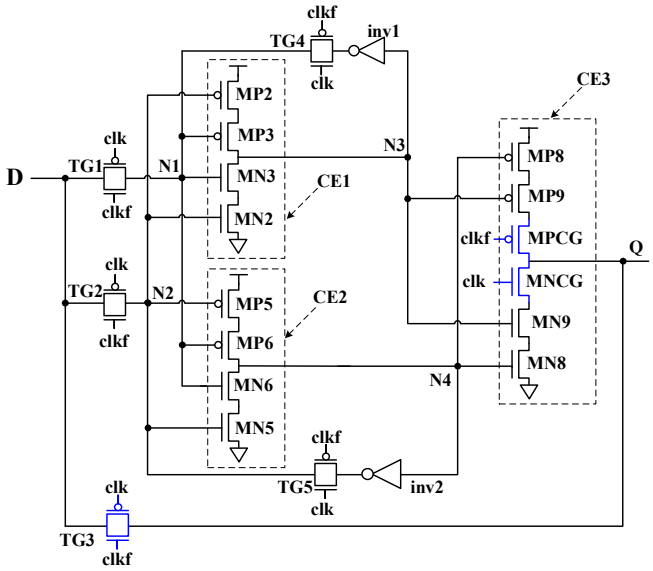

Fig. 7. Proposed high performance SEU-tolerant latch

TABLE I
THE TRANSISTOR ASPECT RATIOS

Name	$(W/L)_P$	$(W/L)_N$
TG1, TG2, TG3, TG4, TG5,	2	2
INV1, INV2	4	2
CE1, CE2, CE3	4	2

OFF to reduce power dissipation and propagation delay. D propagates to Q only through the transmission gate TG3. Transmission gates TG4 and TG5 turn OFF to avoid contention on internal nodes N1 and N2.

When CLK is ‘1’, transmission gates TG1, TG2 and TG3 turn OFF and the HPST latch is not transparent. Transmission gates TG4 and TG5 turn ON to prevent N3 and N4 from floating. There are two interlocked feedback in the HPST latch. The first feedback consists of CE1 and inv1. The second feedback consists of CE2 and inv2. The interlock of two identical feedbacks can effectively improve its robustness. CE1, CE2 and CE3 can effectively mask any particle strikes induced SEU occurring at internal nodes such as N1, N2, N3, N4. SEU occurring at N1 or N2 is masked by CE1 and CE2. SEU occurring at N3 or N4 is masked by CE3. The state noise is isolated from output noise by CE3 which can greatly improve its robustness.

The HPST latch contains C-Element which may introduce high impedence problem. For example, N3 is different from N4 when N3 is upset during the latching phase. As a result, MP8-MP9-MPCG and MNCG- MN9-MN8 are both off and the output node (Q) will keep its previous value. If the clock frequency is low enough and the leakage current of the CE3 will incur a high impedence state at the output node (Q). So the HPST latch is a good choice for high speed design.

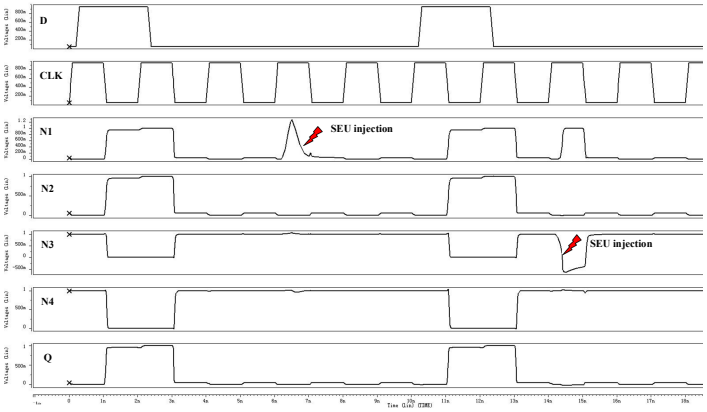

Fig. 8. SEU injection to the proposed HPST latch

B. Simulation and Fault Injection

The presented HPST latch is simulated utilizing Predictive Technology Model (PTM) provided by Nanoscale Integration and Modeling (NIMO) Group of Arizona State University [9]. As an evolution of traditional Berkeley Predictive Technology Model (BPTM), PTM is suitable for technology nodes ranging from 130nm to 16nm. the PTM can be easily customized to cover a wide range of process variation. PTM is more physical, scalable, and continuous over technology generations and

TABLE II
PERFORMANCE COMPARISON BETWEEN THE HPST LATCH AND PREVIOUS LATCHES

Latch	Q_{crit} (fc)	Area (sq)	Delay (ps)	Power (uW)	PDP (fJ)
FERST Latch in [4]	-	64	64.5440	0.51268	0.0331
Dice Latch in [5]	10.92	54	50.4790	0.73916	0.0373
TMR Latch	-	96	52.0180	0.77233	0.0402
CST Latch in [6]	7.93	38	76.7230	0.54607	0.0419
STI Latch in [8]	24.10	80	75.6220	13.51000	1.0217
SDT Latch in [7]	2.75	72	80.3330	18.09700	1.4538
Proposed HPST Latch	-	74	9.9345	0.51995	0.0052

suitable for emerging variability and reliability issues.

We choose 45nm technology model card to perform the simulation. The power supply is 1V. The clock period is 2000ps. The transition time of clock is 100ps.

The transistor aspect ratios of the proposed HPST latch are listed in Table I.

The HPST latch is transparent to transient faults occurring at the input node (D) when CLK is '0'. However, transient faults during the transparent phase of the latch do not matter since the output datum of the HPST latch is not valid. So fault injections have been done only during the latching phase of the HPST latch when CLK is '1'.

The proposed HPST latch is dual interlocked so that SEU occurring at N1 has the same impact as SEU occurring at N2. SEU occurring at N3 also has the same impact as SEU occurring at N4. Fig.8 represents the simulation results of fault injection into internal nodes N1 and N3 at different timing window. The SEU occurring at N1 will be masked by CE1 and CE2. The SEU occurring at N3 will lead to upset at N1 without impact on output Q because it is masked by CE3. The SEU fault injection shows that SEU occurring at internal nodes will not upset the output Q.

IV. LATCH EVALUATION AND COMPARISON

A. *Robustness Comparison to Alternative Solutions*

TABLE III
RELATIVE PERFORMANCE COMPARISON BETWEEN THE HPST LATCH AND PREVIOUS LATCHES

Latch	ΔArea (%)	Δ Delay (%)	ΔPower (%)	ΔPDP (%)
FERST Latch in [4]	15.63%	-84.61%	1.42%	-84.29%
Dice Latch in [5]	37.04%	-80.32%	-29.66%	-86.06%
TMR Latch	-22.92%	-80.90%	-32.68%	-87.06%
CST Latch in [6]	94.74%	-87.05%	-4.78%	-87.59%
STI Latch in [8]	-7.50%	-86.86%	-96.15%	-99.49%
SDT Latch in [7]	2.78%	-87.63%	-97.13%	-99.64%
Average	19.96%	-84.56%	-43.16%	-90.69%

As is illustrated in [4], most of the previous alternative SEU-tolerant solutions can just mitigate the SEU occurring at their internal nodes so that they are vulnerable to high energy particle striking. Only the TMR latch and FERST latch can really tolerate the SEU. The proposed HPST latch is derived from FERST latch with a better performance and lower power dissipation. The HPST latch introduces redundant feedback lines and Muller C-element to block SEUS to achieve equivalent robustness of classical TMR latch. Extensive SPICE-based fault injection simulations have been performed to evaluate and compare the reliability of various radiation hardened by design latch.

To analyze in detail the robustness of the proposed HPST latch, we have evaluated the critical charge of various harden solutions as is shown Table II. Column 1 shows the name of various latches. Column 2 shows the critical charge of various latches to evaluate the robustness. The proposed HPST latch, FERST latch and TMR latch are immune to SEU without internal nodes sensitive to high energy particle striking. The Dice latch, CST latch, STI latch and SDT latch have particular vulnerable nodes so that they are sensitive to high energy particle striking.

B. *Cost comparison to Alternative Solutions*

To analyze in detail the advantages of the proposed HPST latch, we have evaluated the area, propagation delay and power dissipation and the power-delay product of various harden solutions as is shown Table II. Column 1 shows the name of various latches. Column 3 shows the area of the circuits which has been calculated in squares (Sq) as a rough estimate [10]. Column 4, 5 and 6 show the delay, power and power-delay product (PDP). The propagation delay is measured by calculating the delay from D to Q when the corresponding latch is transparent. The power dissipation does not include power dissipation of the clock driver to provide CLK signal and CLKF signal. The clock driver belongs to the clock tree. The clock driver usually includes cascaded inverters with bigger aspect ratio. The clock driver always makes a big contribution to power dissipation.

In Table III, we report the relative cost comparison between the HPST latch and previous latches. Column 1 shows the name of various latches. Column 2, 3, 4 and 5 show the relative cost of area (ΔArea), delay (ΔDelay), power (ΔPower) and power-delay product (ΔPDP). The relative cost is evaluated as follows:

Δ = (HPST_latch – alternative_latch) / alternative_latch

Column 2 shows that the HPST latch incurs 19.96% area overhead to make a tradeoff among area, performance, power and reliability.

Column 3 shows that the HPST latch achieves 84.56% reduction on average in term of delay. The HPST latch provides high performance.

Column 4 shows that the HPST latch achieves 43.16% reduction on average in power dissipation. The HPST latch provides low power dissipation by clock gating the Muller C-element at the output.

Column 5 shows that the HPST latch achieves 90.69%

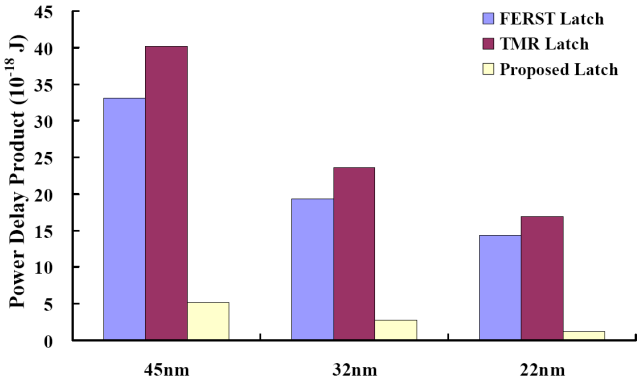

Fig. 9. Power delay product at different technology nodes

reduction on average in power-delay product.

Fig.9 represents the power delay product values at various technology nodes of 45nm, 32nm and 22nm. The proposed HSPT latch has equivalent robustness of FERST latch and TMR latch. It is evident that the amount of power delay product is reduced significantly in the proposed latch in comparison with FERST latch and TMR latch.

In a word, the HPST latch provides a higher robustness without internal nodes sensitive to high energy particle striking, as well as a lower power-delay product than previous solutions.

V. Conclusion

In this paper, we have proposed a high performance SEU-tolerance latch for nanoscale CMOS technology. The HPST latch utilizes redundant feedback lines and Muller C-element to mask SEUS with equivalent robustness of classical TMR latch. The HPST latch reduces power dissipation by clock gating the Muller C-element at the output. The HPST latch provides a higher robustness without internal nodes sensitive to high energy particle striking, as well as a lower power-delay product than previous solutions. HPST latch achieve a tradeoff among area, performance, power and reliability.

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