A Low Power and Robust Carbon Nanotube 6T SRAM Design with Metallic Tolerance

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***Abstract*—Carbon nanotube field-effect transistor (CNTFET) is envisioned as a promising device to overcome the limitations of traditional CMOS based MOSFETs due to its favourable physical properties. This paper presents a novel six-transistor (6T) static random access memory (SRAM) bitcell design using CNTFETs. Extensive validations and comparative analyses are carried out with the proposed SRAM design using SPICE based simulations. We show that the proposed CNTFET based SRAM has a significantly better static noise margin (SNM) and write ability margin (WAM) compared to a CNTFET-based standard 6T bitcell, equivalent to isolated read-port 8T cell based on CNTFET, while consuming less dynamic power. We further demonstrate that it exhibits higher robustness under process, voltage and temperature (PVT) variations when compared with the traditional CMOS SRAM cell designs. Furthermore, metallic CNTs removal technique is used considering metallic tolerance to make the proposed SRAM design more reliable.**

I. Introduction

With continuous CMOS technology scaling, device feature sizes are shrinking to unprecedented levels. This has enabled integration of a large number of devices on a chip and reduction of power through aggressive voltage scaling. However, such scaling (especially beyond 32-nm node) has also led to a significant increase in standby power dissipation, power density and process variability, which in turn affects the reliability of these circuits and systems [1]. Therefore, new materials and devices have been investigated over the years to replace the silicon based nano-scale devices.

Carbon nanotube FET (CNTFET) is a promising alternative to the conventional bulk CMOS technology [2]. Compared to CMOS technology, CNTFETs offer many favourable physical properties, such as reduced PVT variations, better gate controllability, high thermal stability and drive currents. Moreover, CNTFETs have been shown to overcome many other fundamental limitations of the traditional nano-scale silicon MOSFETs, including ultra long mean-free-path (MFP) for elastic scattering, ballistic or near ballistic transport properties in intrinsic CNT under low voltage bias to achieve the ultimate device performance [3]. Due to these advantages, CNTFETs have been designed and modelled by various industrial and academic research organizations. Examples include CNTFET devices and circuits model proposed by Stanford Nano-electronics Lab [4], CNT interconnections developed and simulated by Naeemi *et al.* [5], prototype CNTFET development and measurements by Shimadzu [6].

Memory plays an important role in modern system-on-chip (SoC) applications [7]. Hence, it is essential to develop novel SRAMs that will scale for the performance and reliability demands of future SoCs, which is currently limited by nano-scale features and properties of conventional CMOS technologies. To this end, researchers have proposed and investigated various CNTFET-based SRAM bitcells as an alternative over the years. Kureshi *et al.* [8] explored the performance of the CNTFET-based standard 6-transistor (6T) as shown in Fig. 1 (a) and compared it with that of the conventional CMOS cell at 32-nm technology node. Zhang *et al.* [9] reported a study of CNTFET-based 8-transistor (8T) memory cell with an isolated read-port as shown in Fig. 1 (b). Their work showed the advantages of CNTFET cells over the CMOS cells in terms of power consumption and the noise margin. These CNTFET based SRAM designs will be further evaluated in Section II-C.

The **contributions of this paper** are as follows: a novel reliable low power single-ended 6T SRAM bitcell design with an isolated read-port is proposed as shown in Fig. 2. The proposed design is compared with CMOS-based single-ended 6T SRAM cells and other CNTFET based SRAM cells (Fig. 1) through extensive SPICE simulations. Moreover, the PVT robustness, read/write stability and power dissipation are evaluated against standard 6T, single-ended 6T and 8T SRAM bitcells. Furthermore, to overcome the presence of metallic carbon nanotubes, a metallic tolerant single-ended 6T SRAM bitcell is proposed with metallic CNTs removal technique.

The rest of the paper is organized as follows. Section II (*A*) introduces proposed CNTFET-based SRAM bitcell, while Section II (*B*) and (*C*) present the simulation results highlighting the comparison in terms of performance, power dissipation and stability of proposed SRAM bitcell design. Section III details further enhancement of the SRAM bitcell design to improve tolerance to metallic CNTs. Finally, Section IV concludes the paper.

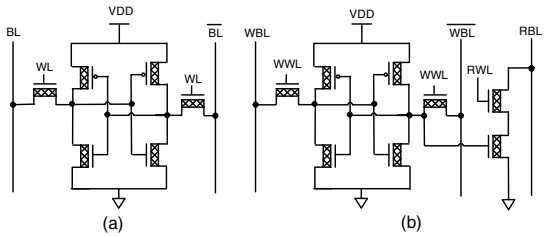

Fig. 1. Recently reported CNTFET SRAM bitcells (a) standard 6T SRAM cell [8] (b) isolated read-port 8T SRAM cell [9]

II. Proposed CNTFET-based SRAM Design

Proposed CNTFET-based SRAM structure is detailed. Using extensive SPICE simulations, the effectiveness of the

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proposed SRAM bitcell design is evaluated and then compared to other bitcell designs.

A. CNTFET-based Single-Ended 6T SRAM Bitcell

Fig. 2 shows the proposed CNTFET-based single-ended 6T SRAM bitcell with a separate read-port. As can be seen, the SRAM bitcell comprises of two cross-coupled inverters - *inverter1* and *inverter2*. The inverter pair is connected to the single bitline (BL) through the access transistor CNTN3 and the isolated read-port transistor CNTN4. The access transistor CNTN3 is controlled by the write wordline (Write_WL). The separate read port consists of transistor CNTN4 and the read assist transistor CNTRA which is shared per memory word by row in a word-oriented SRAM array design. A write assist transistor CNTWA is employed to weaken the strongly cross-coupled inverter pair since the write operation is difficult for the single-ended SRAM structure. Similarly, the write assist transistor CNTWA is shared per word and controlled by W0. Therefore, each single-ended SRAM bitcell design consists of six transistors (6T). As can be seen, two additional read and write assist transistors are shared per word.

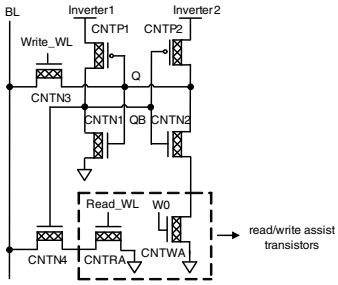

Fig. 2. Proposed single-ended 6T SRAM bitcell with read/write assist transistors

The authors in [10] showed that CMOS-based single-ended 6T SRAM bitcell offers the advantages on stability and power saving compared to the CMOS-based standard 6T and 8T SRAM bitcells. The single-ended and isolated read port structure improves the dynamic power, leakage power consumption and the read SNM. The write-ability margin (WAM) is benefited from the shared write assist transistor. The area of the single-ended 6T SRAM cell is 16% higher than standard 6T cell and 14% less compared to 8T SRAM design reported by [10]. In the next section, the advantages of proposed bitcell are shown over CMOS-based single-ended 6T SRAM bitcell.

B. Comparison between CNTFET-based and CMOS-based SRAM Bitcells

The CMOS-based SRAM designs have been shown to have issues in terms of stability and driving capability during very low power operation [11]. CNTFET, however, is expected to exhibit higher stability with aggressive technology and voltage scaling. In this section, we compare the CNTFET-based single-ended 6T SRAM bitcell with CMOS-based bitcell in terms of SNM, driving capability and robustness under PVT variations. The CNTFET bitcell is based on built-in Stanford model [4], while the CMOS cell is based on Berkeley predictive technology model (BPTM) at 32-nm technology node.

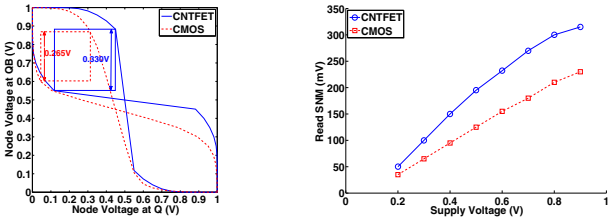

Fig. 3. (a) SNM comparisons of single-ended 6T SRAM bitcells (b) SNM variation with respect to VDD

SRAM bitcell stability is characterized by the static noise margin (SNM) criterion, defined by the minimum DC noise voltage that will flip the state of the SRAM cell [12]. Fig. 3 (a) shows the read SNM comparisons of single-ended 6T bitcell in CNTFET and CMOS. As can be seen, the CNTFET cell has higher read SNM (0.330V) compared to CMOS cell which has 0.265V read SNM at a supply voltage of 1.0V. This is because of the higher threshold voltage and lower leakage current in CNTFET compared to CMOS transistor. To demonstrate the SNM advantages of CNTFET further, Fig. 3 (b) presents the read SNM of both cells with respect to supply voltage (VDD). As expected, the CNTFET bitcell always exhibits better SNM than CMOS cell with VDD changing from 0.2V to 0.9V. At VDD = 0.2V, the read SNM of CNTFET cell is 30% higher than CMOS cell. Thus, CNTFETs offer more stability for ultra-low power memories.

To further demonstrate the SNM stability under PVT variations, Table. I shows the read SNM under temperature variation for both cells. The read SNM of both designs experience a slight decreasing trend when the temperature changes from 25°C to 100°C. The SNM of CMOS-based cell drops from 265mV to 240mV, by up to 9.5%, while such SNM decrement is only 4.5% for CNTFET cell. CNTFET demonstrates higher thermal stability, since there is only a very minor change in transconductance under temperature variations [13].

TABLE I. SNM VARIATION WITH RESPECT TO TEMPERATURE

Temperature	CNTFET	CMOS
0°C	330mV	265mV
25°C	328mV	260mV
75°C	323mV	252mV
100°C	315mV	240mV

Driving capabilities in terms of write delay and power are major indications of SRAM bitcell performance. To evaluate comparative performances, Fig. 4 shows the write delay and power variations when supply voltage (VDD) changes from 0.4V to 1.0V. From Fig. 4 (a), it can be seen that the write delay of CMOS-based cell increases dramatically in the low power region (below 0.6V), whereas CNTFET cell shows a gradual rise trend with VDD scaling. This is due to the high mobility of CNTFETs [8]. When VDD = 0.4V and 1.0V, the delay power product of CNTFET cell is 15× and 2× better than CMOS cell, respectively. Therefore, CNTFETs can provide much better performance for low power memories.

C. Comparison of CNTFET-based SRAM Bitcells

In this section, the proposed SRAM bitcell is compared with the CNTFET-based standard 6T and isolated read-port 8T [9] SRAM bitcells (shown in Fig. 1 (a) and (b)).

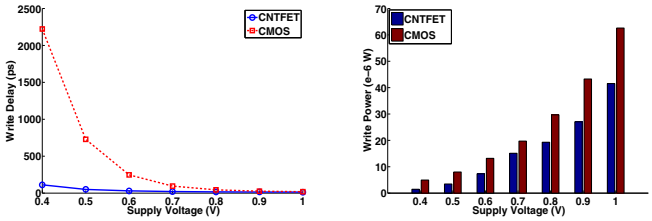

Fig. 4. (a) write delay variation with respect to VDD (b) write power variation with respect to VDD

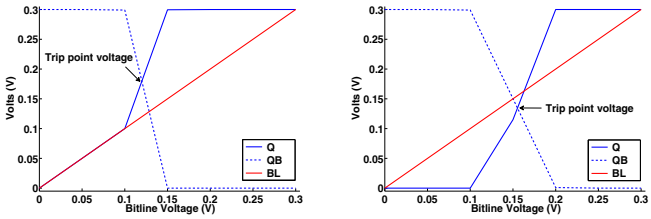

Fig. 6. (a) Write trip voltage of proposed SRAM cell (b) Write trip voltage of CNTFEI-based 8T SRAM cell at Vdd=0.3v for W1→0

Fig. 5 shows comparative read SNMs of three CNTFET SRAM bitcells (Fig. 1 and Fig. 2). The proposed CNTFET single-ended 6T cell (Fig. 2) has a better SNM than standard 6T cell and equivalent to the 8T SRAM cell. Due to the isolated read-port structure, both single-ended 6T and 8T bitcells are required to pre-charge the bitline before each read operation and data is directly sensed from the bitline. Hence, they have the same read SNM.

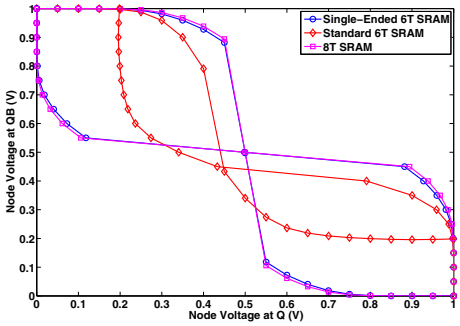

Fig. 5. SNM Comparison of CNTFET-based single-ended 6T, standard 6T and 8T SRAM Designs

During a write operation, write ability of a SRAM bitcell is best characterized using write trip voltage, which is defined as the maximum voltage on the bitline needed to flip the bitcell content [12]. Here, writing "1" into the SRAM cell while its original content was "0" (W1→0) is measured because W0→1 is easier and quicker for the single-ended 6T [10]. The writing is symmetric in 8T SRAM cell. To compare write-ability margins (WAM), Fig. 6 shows the comparative write trip voltages. As can be seen, the write trip voltage of CNTFET-based single-ended 6T SRAM is 0.18V, which is higher than 8T bitcell (0.135V) at VDD=0.3V. Hence, the write ability of proposed SRAM design is little bit less than CNTFET-based 8T bitcell. However, the 8T cell has higher probability of having an erroneous write than proposed SRAM cell, due to the bitline noise.

Table II compares the dynamic power in CNTFET-based single-ended 6T, standard 6T and 8T SRAM bitcells for different read and write operations. Due to the asymmetric structures of single-ended 6T and 8T cells, the patterns of the dynamic power dissipation are also asymmetric. Therefore, 8 cases are considered to measure the dynamic power: R1→0, R1→1, R0→1, R0→0, W1→0, W1→1, W0→1 and W0→0. For example, R1→0 stands for reading "1" from the SRAM cell when the previous output is "0". And W1→0 is to write "1" into the SRAM cell when its original content was "0". As aforementioned, read operation of single-ended 6T SRAM design is similar as 8T SRAM cell since both cells employ the separate read-port mechanism. The bitline power consumption of read operation for both cells are the same. Similarly, the write operation of standard 6T and 8T SRAM bitcells are identical. Thus, the standard 6T and 8T cells have the same bitline power dissipation for the write events. As shown in Table II, the average dynamic power dissipation of proposed SRAM cell is 40.5% less than CNTFET-based standard 6T cell and 26.6% less compared to CNTFET-based 8T cell.

TABLE II. DYNAMIC POWER DISSIPATION FOR DIFFERENT READ AND WRITE OPERATION OF SINGLE-ENDED 6T, STANDARD 6T AND 8T SRAM DESIGNS IN CNTFET

Dynamic Power (μW)	Single-ended 6T	Standard 6T	8T
R1→0	2.168	2.576	2.175
R1→1	0.103	2.834	0.112
R0→1	4.285	3.198	4.346
R0→0	3.952	3.065	4.064
W1→0	1.896	4.420	4.382
W1→1	0.110	3.988	3.972
W0→1	2.274	4.224	4.143
W0→0	2.305	4.045	4.096
average	2.13	3.55	2.90

III. PROPOSED SRAM DESIGN WITH IMPROVED METALLIC CNT TOLERANCE

Despite their advantages (highlighted in Section II), CNTFET-based SRAM cells have problems with short circuit unreliability due to their semi-conductive or metallic path between source and drain, introduced due to their unique rolled structure during fabrication or modeling.

To improve the CNTFET SRAM reliability with reduced short circuit effects, an approach is to use an array of asymmetrically correlated CNTs (ACCNT) to reduce conduction in CNTFETs [14]. Using this approach a metallic CNTs removal technique [9] can be applied to reduce the number of metallic CNTs. This approach can be a good fit for our proposed CNTFET SRAM bitcell to improve its short circuit unreliability compared to other SRAM designs since our proposed design contains asymmetric structure. Therefore, we employ metallic CNTs removal technique to improve the probability of functional transistors in our proposed CNTFET SRAM bitcell, which is further detailed in the following.

A. Probability of Functional Transistor without Metallic CNTs

According to [9], the probability of the functional transistor can be expressed as:

$$P_{transistor} = [1-(1-P_{semi})^k]^j \quad (1)$$

Here, P_{semi} is the probability that the CNT is a semiconductor, j is the number of series CNTFETs and k is the

number of parallel CNTFETs. Assume each CNTFET has one CNT. When the number of series CNTFETs increases, the probability of functional transistor ($P_{transistor}$) will be lower. Thus, j is set to 1 in the metallic CNTs removal approach to obtain the highest functional probability. Then, expression (1) becomes:

$$P_{transistor} = 1 - (1 - P_{semi})^k \quad (2)$$

Based on the layout of single-ended 6T SRAM bitcell [10], using metallic CNTs removal approach results in 3 identical transistor pairs: CNTP1-CNTP2 (inv_p), CNTN1-CNTN2 (inv_n), CNTN3-CNTWA(write) and 2 independent CNTFETs: CNTN4(read), CNTRA(read_assist). Assume every CNTFET has the same functional probability. Hence, the probability of memory cell (P_{pro_6T}) is:

$$P_{pro\_6T} = P_{inv\_p} \times P_{inv\_n} \times P_{write} \times P_{read} \times P_{read\_assist} = (P_{transistor})^5 \quad (3)$$

TABLE III. PROBABILITY OF FUNCTIONAL TRANSISTOR WITHOUT METALLIC CNTS

k	P_{semi}=90%	P_{semi}=95%
1	59.05%	77.38%
2	95.10%	98.76%
3	99.50%	99.94%
4	99.95%	99.99%
5	99.99%	99.99%
6	99.99%	100%

Using Expression (3), the probability of having functional single-ended 6T SRAM cells is calculated in Table III given a P_{semi} of 90% and 95%. The number of parallel CNTFETs varies from 1 to 6. If a limit is placed on the probability of functional SRAM cells that can be tolerated, say 99.9%, then the number of parallel CNTFETs (k) can be determined. For P_{semi}=90%, k should be no less than 4, while there should be more than two parallel CNTFETs in case P_{semi}=95%.

B. Evaluation of Metallic CNTs Tolerant SRAM Bitcell

In this section, the metallic tolerant single-ended 6T SRAM cell is compared to the original CNTFET-based cell.

TABLE IV. READ/WRITE DELAY OF SINGLE-ENDED 6T SRAM WITH METALLIC CNTS REMOVAL TECHNIQUE

k	Read Delay (e-11s)	Write Delay (e-11s)
1	2.354	1.375
2	1.798	1.423
3	1.652	1.601

Table. IV shows the read and write delay with number of parallel CNTFETs (k) increasing from 1 to 3. When k=1, it stands for the original SRAM cell. From Table. IV, we can see that the read delay decreases. This is due to the parallel connection of the CNTFETs in the metallic tolerant SRAM bitcell. Whereas, the delay of write operation rises, since the capacitance of write wordline (WWL) becomes higher when the number of parallel CNTFETs increases.

For SRAM bitcell with metallic tolerance, the overall power dissipation becomes larger because more CNTs are used to build the SRAM cell. Due to the parallel connection, the load capacitance is enlarged by the added internal capacitance of the CNTFETs. This results in larger dynamic power consumption in SRAM cell.

The parallel connection of CNTFETs in metallic removal technique does not change the stability of single-ended 6T SRAM cell. As aforementioned, the read SNM of proposed design is only affected by the ratio between CNTP1 and CNTN1. When k changes, the number of parallel CNTFETs in both CNTP1 and CNTN1 change simultaneously. Thus, the ratio remains constant and SNM maintains the same.

IV. CONCLUSIONS

A novel carbon nanotube field effect transistor (CNTFET) based single-ended 6T SRAM bitcell with a separate read-port is proposed. Our proposed design shows better robustness under PVT variation than CMOS-based single-ended 6T SRAM design and offers the advantages over CNTFET-based standard 6T and 8T SRAM bitcells in terms of performance, stability and power dissipation. Due to the presence of metallic CNTs, a metallic CNTs removal approach is applied to the proposed SRAM design to increase the probability of functional SRAM cells, by up to 99.9%. Furthermore, the proposed SRAM design with metallic tolerance is evaluated.

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REFERENCES

[1] T-C. Chen, "Overcoming research challenges for CMOS scaling: Industry directions," in *Proc. Int. Conf. Solid-State and IC Technol*, pp. 4–7, Oct. 2006.

[2] Y. Lin *et al.*, "High-performance carbon nanotube field-effect transistor with tunable polarities," *IEEE Trans. on Nanotechnology*, vol. 4, no. 5, pp. 481–489, Sep. 2005.

[3] A. Javey *et al.* "Carbon nanotube field-effect transistors with integrated ohmic contacts and high-k gate dielectrics," *Nano Letters*, vol. 4, no. 3, pp. 447–450, Sep. 2004.

[4] J. Deng, and H.-S. P. Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application - Part II: Full Device Model and Circuit Performance Benchmarking," *IEEE Trans. Electron Devices*, vol 54, pp. 3195-3205, 2007.

[5] A. Naeemi *et al.* "Performance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI)," *IEEE Electron Devices Letters*, vol 26, pp. 84-86, 2005.

[6] Shimadzu Corporation, "Carbon Nanotube: Mapping of CNT FET," *http://www.shimadzu.com/an/industry/../cnt_0105005.htm*, Last visited 15/09/2013.

[7] H. Shim, Y. Joo, Y. Choi, H. G. Lee, and N. Chang "Low-energy off-chip SDRAM memory systems for embedded applications," *ACM Trans. on Embedded Computing Systems*, vol 2, no. 1, pp. 98-130, 2003.

[8] A. K. Kureshi, and Mohd. Hasan, "Performance comparison of CNFET- and CMOS-based 6T SRAM cell in deep submicron," *Microelectronics Journal*, vol. 40, no. 6, pp. 979–982, Jun. 2009.

[9] Z. Zhang, and J. G. Delgado-Frias, "Carbon Nanotube SRAM Design With Metallic CNT or Removed Metallic CNT Tolerant Approaches," *IEEE Trans. on Nanotechnology*, vol 11, no. 4, pp. 788-798, Jul. 2012.

[10] J. Singh *et al.* "Single Ended 6T SRAM with Isolated Read-Port for Low-Power Embedded Systems," in *Proc. of 12th IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 917–922, Apr. 2009.

[11] A. Pushkarna *et al.* "Comparison of performance parameters of SRAM designs in 16nm CMOS and CNTFET technologies," in *Proc. of IEEE International SOC Conference*, pp. 339–342, 2010.

[12] E. Grossar *et al.* "Read stability and write-ability analysis of SRAM cells for nanometer technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2577–2588, Nov. 2006.

[13] S. Tans *et al.* "Room-temperature transistor based on a single carbon nanotube," *Nature*, vol 393, pp. 49–52, 1998.

[14] A. Lin *et al.* "ACCNT: A Metallic-CNT-Tolerant Design Methodology for Carbon Nanotube VLSI: Analyses and Design Guidelines," *IEEE Trans. on Electron Devices*, vol. 57, no. 9, pp. 2284–2295, Sep. 2010.