Pseudo Circuit Model for Representing Uncertainty in Waveforms

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***Abstract*—This paper introduces a novel compact implicit model for a *probabilistic set of waveforms (PSoW)* which arise as representations for uncertain signal waveforms in *Statistical Static Timing Analysis (SSTA)*. In traditional SSTA tools, signals are just represented as (distributions of) arrival time and slew. In our approach, to increase accuracy, PSoW's are used instead. However, to represent PSoW's explicitly, a very large amount of data is necessary, which can be problematic. To solve this problem, a compact implicit model is introduced, which can be characterized with just a handful of parameters. The results obtained show that the implicit model can generate real-life PSoW's with high accuracy.**

I. Introduction

Static Timing Analysis (STA) is an efficient way to estimate timing of digital integrated circuits. It derives its linear time complexity from the fact that it visits each logic gate only once, in a breadth-first order from inputs to outputs. STA derives the timing at the output of the gate from the known timing at its inputs and a given timing model for the gate and the wires at its output. Traditionally, as abstraction for delay, only arrival time and slew of the electrical signals are stored and used in the gate and wire models, as in the widely used industry standard *Non-Linear Delay Model (NLDM)* [1]. More recently, it has been recognized that this leads to unacceptable inaccuracy in modern CMOS technologies, and there is a move to more accurate gate models which store full signal waveforms instead of just delay and slew, either current (CCS) [2] or voltage (ECSM) [3].

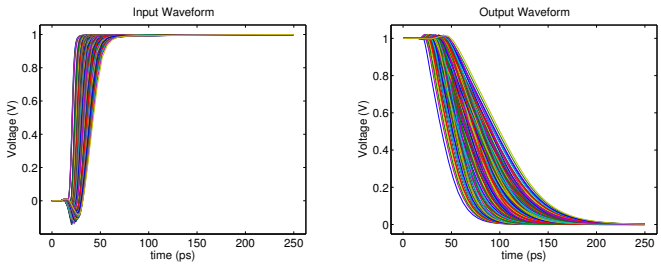
Given the large variability in the physical properties of current and future CMOS processes, there is no longer one answer to the question "what is the delay of my circuit". Rather, delay is a statistical quantity. With this understanding, methods for *Statistical Static Timing Analysis (SSTA)* have been developed. Sofar, these methods have extended the notions of arrival time and slew to distributions [4]. But, also for SSTA there is a need to increase accuracy, and use a more physical abstraction of the signals in the circuit. A logical step is to move to the statistical version of electrical waveforms, which in this paper we call *Probabilistic Sets of Waveforms (PSoW)*. The novel SSTA engine developed at the Technical University of Delft [5], [6] uses such an approach. [1]

One of the problems of using PSoW's is that it takes a large amount of data to describe them explicitly. This paper tries to overcome this problem by representing them implicitly with a small generating circuit, which is defined with only a few parameters. This is a good fit for the SSTA tool of [5], [6], as it uses gate models at the transistor level, which are evaluated using a fast, implicitly statistical SPICE-like simulator. This setup results in very accurate statistical results, without the need for slow Monte Carlo iterations.

II. Probabilistic Sets of Waveforms

PSoW's in SSTA are used to store the various output waveforms which arise due to *process, voltage and temperature (PVT)* variations in the circuit. Giving SSTA full access to signal waveforms makes it more accurate, as the behavior of a gate is very sensitive to the exact shape of the input waveform.

An example of the range of possible input and output waveforms of an inverter in a 45nm technology (from a Nangate library [7] using a predictive technology model [8]) is pictured in Fig. 1a and Fig. 1b. This result was obtained by varying the MOSFET channel length (L). The input signal was generated by feeding a simple ramp signal to two inverters with varying L, to mimic a realistic signal somewhere in a circuit. As not every value of L is equally likely, a probability is associated with every waveform.



(a) Input waveforms (b) Output waveforms

Fig. 1: PSoW for Inverter Chain

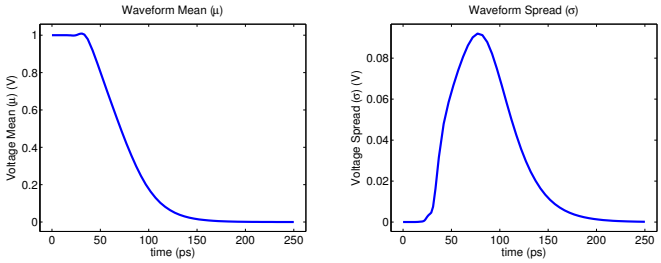
In our SSTA methodology, it is required to represent and store the PSoW's. The main challenge is the amount of data involved. There are several possible approaches to represent PSoW's:

A. Lookup Table based Representation

This is a simple explicit representation of a set of waveforms comparable to the CCS and ECSM models. Each waveform is stored as an array of time-value pairs with its probability.

B. Statistical Moments based Representation

If the PSoW is cross-sectioned vertically at a time value, there are various possible output voltages. We can obtain the mean, standard deviation (SD) and higher order statistical moments of the voltage at a time value. This results in statistical moments of the voltage as a function of time. The mean (μ) and SD (σ) of the voltage as a function of the time are shown in Fig. 2a and Fig. 2b. Instead of storing the entire PSoW, only the moment curves are stored. As



(a) Mean curve ($\mu(t)$) of PSoW (b) SD curve ($\sigma(t)$) of PSoW

Fig. 2: Mean and SD of the PSoW as a function of time

[1]This research was sponsored by the European Union and the Dutch government as part of the ENIAC/MODERN project.

compared to the lookup table based representation, this approach already requires less memory

C. Pseudo Circuit based Representation

A PSoW is the output of a standard cell. Thus, a PSoW can be represented by a circuit with PVT variations. Having the circuit and the PVT variations is sufficient to regenerate the voltage waveforms. For this reason we suggest to use an implicit circuit-like model to represent a PSoW. During SSTA, the input signals of the gate which is evaluated are then replaced by pseudo circuits. As our SSTA approach uses a fast SPICE-like simulator as basic engine, the pseudo circuit can be merged with the standard cell circuit during simulation. In this paper, we use a single pseudo circuit configuration with just a few parameters. Since the pseudo circuit is then fully described by only these parameters, it is a very compact way to store a PSoW.

III. Pseudo Circuit Model

The purpose of the pseudo circuit is to reconstruct the desired PSoW at the input of a standard cell. First, we look at the selection of the pseudo circuit topology and parameters. Then, we study processing of the simulation output and constructing a database such that PSoW's can be compared. Then, a methodology is proposed to estimate the pseudo circuit parameters given a PSoW.

A. The Pseudo Circuit

The design space of the pseudo circuit is large because we could choose any topology. Since the pseudo circuit is not a part of the real digital circuit, some non-realistic circuits could also be selected for the design. Five constraints are imposed on the pseudo circuit:

1) The output of the pseudo circuit should be similar to the output of a gate in the digital circuit.
2) The pseudo circuit should be small.
3) The output space of the pseudo circuit should cover the entire possible output range of gates.
4) The absolute transition time of the waveform should match.
5) The pseudo circuit should have PVT variations.

The output signal transition of a gate is basically the charging or discharging of the effective capacitive load at the output pin. Therefore, an RC circuit is one of the simplest possible pseudo circuits. However, the MOSFETs in a digital CMOS gate are quite nonlinear. Since accuracy in delay estimation is the primary objective, a digital gate is selected for the pseudo circuit design. To keep the simulation overhead as small as possible, we select the simplest digital gate: an inverter. To produce a realistic PSoW at the input of this inverter, we add two more inverters to form a three inverter chain, which is driven by a simple ramp signal. See Fig. 3.

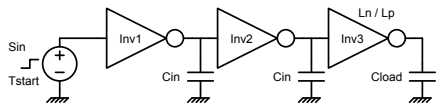


Fig. 3: The Pseudo Circuit Schematic

The pseudo circuit is used to represent any possible target PSoW which could be the output of any digital cell. Let us first consider only the nominal waveform (when all the PVT parameters are at their nominal values). It should be able to have all possible realistic slew values. We first add a ideal ramp voltage source with tunable input signal slew (S_{in}) and a tunable capacitive load (C_{load}). However, this is not enough. The output loads of Inv_1 and Inv_2 are still constant. Due to the electric gain, the sensitivity of the output signal slew with respect to the input signal slew is low for an inverter. The input signal slew of Inv_3 is not well controllable. Therefore, we add additional capacitors at the intermediate nodes, with the same value to reduce the design space by one dimension. For each pair of S_{in} and C_{load}, a value of C_{in} is selected such that the input signal slew of Inv_3 is exactly the same as the input slew of Inv_1.

We control the start time of the output transition by shifting the transition of the input ramp signal. This adds parameter T_{start}.

Realistic PVT variations have many parameters. To keep the number of parameters limited, we choose to only vary one PVT parameter in the psuedo circuit, the transistor length. We vary the PMOS (L_p) and the NMOS (L_n), with a correlation equal to one.

The final pseudo circuit has four independent parameters (S_{in}, C_{load}, σ_L, T_{start}) and one dependent parameter (C_{in}). The spread in the channel length (σ_L) directly controls the spread in the output waveform. Therefore, the channel length spread (σ_L) can attain various possible values to generate various possible target PSoW's. The FSME method [9] gives the flexibility to select the pdf of the parameters after the circuit simulation. Due to this feature, the pseudo circuit is simulated only once with the maximum possible parameter spread (σ_L) using the FSME method and the output is stored in a database. The actual spread of the channel length variation is used during waveform comparison.

The pseudo circuit is simulated for the sampled values of S_{in} and C_{load} from their respective range using the highest value of σ_L in the specified range. The output waveforms of each simulation along with their circuit configurations are stored in a database. This database is used during the SSTA flow to estimate the pseudo circuit parameters such that the target waveforms can be generated.

B. Database Processing and Quality Factors

The comparison of the PSoW's is in itself a challenging task due to the fact that a PSoW is a dataset with five dimensions (S_{in}, C_{load}, σ_L, $time$, $Voltage$). To reduce the complexity of the problem, only mean and SD curves of the waveforms are compared. Additionally, instead of comparing the entire mean and SD curve, only their "quality factors" are compared. Here, quality factors are specific parameters which can quantitatively measure the shape of waveforms. The proposed quality factors of the mean and SD curves are:

1) The slew of the mean curve (Q_{Slew})
2) The separation of mean and SD curves ($Q_{ShiftMean}$)
3) The peak height of the SD curve (Q_{Max})
4) The V_{DD} / 2 crossing time of the mean curve (Q_{Tmid})

The quality factors are demonstrated with the mean and SD curves in Fig. 4.

$\mathbf{Q_{Slew}}$ is the slew of the mean curve of the PSoW. It is basically independent of σ_L. Therefore, the Q_{Slew} is independent of the spread used in the pseudo circuit.

$\mathbf{Q_{ShiftMean}}$ is a measure of separation between the mean and SD curves. The position of the mean curve is defined by its 50% voltage crossing time. The position of the SD curve is defined by the weighted mean of time while considering the SD curve as a weight profile.

$\mathbf{Q_{Max}}$ is the maximum spread of the waveform. Since the spread in the output waveform depends on σ_L, Q_{Max} is a function of σ_L. During the experiments, it has been found that Q_{Max} is close to a linear function of σ_L. Therefore, Q_{Max} can be written as:

$$Q_{Max} = Q_{MaxM} \times \sigma_L + Q_{MaxC} \tag{1}$$

$\mathbf{Q_{Tmid}}$ is the 50% voltage crossing time of the mean curve. It is used to measure the absolute start time of the transition of the PSoW.

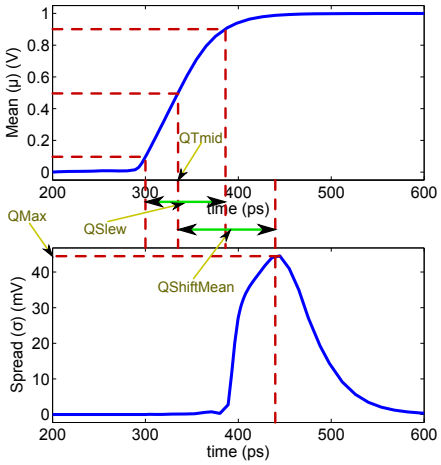


Fig. 4: Quality factors for the waveform comparison

In our method, we calculate and cache PSoWs and their quality factors for many values of input signal slew (S_{in}) and output capacitive load (C_{load}).

C. Waveform Comparison Methodology

We now need to choose the pseudo circuit parameters to generate a given PSoW. The quality factors of the target PSoW (T_{Slew}, $T_{ShiftMean}$, T_{Max} and T_{Tmid}) are calculated first.

The quality factor Q_{Slew} is a function of slew (S_{in}) and output capacitive load (C_{load}) as shown in Fig. 5a. A collection of S_{in}-C_{load} pairs can be estimated such that Q_{Slew} is equal to T_{Slew} as shown in Fig. 5b (the red points). The black line is a linear best fit curve of the interpolated points.

$Q_{ShiftMean}$ is also a function of C_{in} and C_{load}. Therefore, a similar collection of S_{in}-C_{load} pairs can be estimated such that $Q_{ShiftMean}$ is equal to $T_{ShiftMean}$.

The intersection of Q_{Slew} with T_{Slew} and $Q_{ShiftMean}$ with $T_{ShiftMean}$ gives two lines in the S_{in}-C_{load} plane which satisfy the individual quality factors. The intersection of these two lines will give a pair of S_{in}-C_{load} which will satisfy both of the quality factors simultaneously as shown in Fig. 5c. Let us call the intersection value of S_{in} and C_{load} MS_{in} and MC_{load} respectively. MS_{in} and MC_{load} are the two parameters of the pseudo circuit which satisfy the quality factors T_{Slew} and $T_{ShiftMean}$.

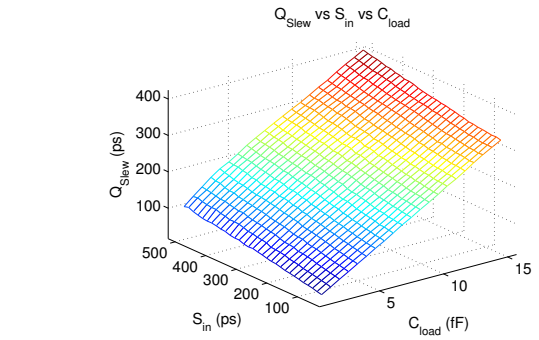
The datasets C_{in}, Q_{MaxM}, Q_{MaxC}, and Q_{Tmid} are a function of S_{in} and C_{load}. The values of C_{in}, Q_{MaxM}, Q_{MaxC}, and Q_{Tmid} for the corresponding model parameters MS_{in} and MC_{load} can be estimated using an interpolation function. Let us call these interpolated values MC_{in}, MQ_{MaxM}, MQ_{MaxC}, and MT_{mid}.

As we discussed earlier, Q_{MaxM} and Q_{MaxC} are the coefficients of the linear function of Q_{Max} vs σ_L as given in (1). The value of σ_L for the target T_{Max} ($M\sigma_L$) can be estimated using this equation.

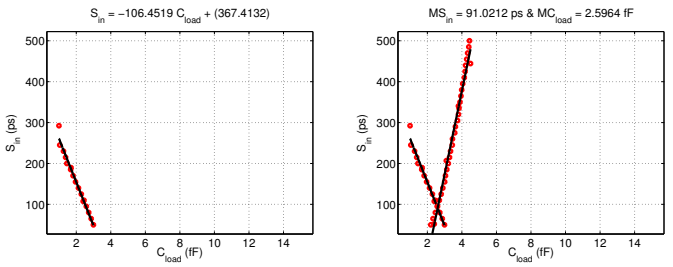
The 50% crossing time of the mean curve of the PSoW corresponding to the selected MS_{in} and MC_{load} is M_{Tmid}. The same for the target waveform is T_{Tmid}. The delay compensation, required for the synchronization of absolute time, is equal to the difference of the T_{Tmid} and M_{Tmid}.

IV. Results

To evaluate the accuracy of the proposed modelling scheme, Spectre circuit simulations are carried out on a realistic digital data path driving various standard cells. The data path is then replaced by



(a) Q_{Slew} vs S_{in} vs C_{load}



(b) Q_{Slew} & T_{Slew} intersection (c) Slew & ShiftMean intersection

Fig. 5: MS_{in} and MC_{load} estimation

our pseudo circuit model, and the results (in terms of distributions of delay and slew along with the mean and SD curve of input PSoW) are compared. In the experiments, 45nm PTM based Nangate cells [7], [8] have been used.

Two sets of simulations are carried out for each gate (DUT). The first simulation is with a real driver circuit to generate a reference PSoW ("Target PSoW"). Our method is then used to estimate the parameters of the pseudo circuit model which can generate the Target PSoW. Then, the real driver is replaced by the pseudo circuit model and simulated, generating the "Model PSoW". The target PSoW is compared with the model PSoW to analyze the accuracy of the model. Additionally, as we target delay calculation, we compare the mean and SD of the delay of the DUT and the output signal slew. The PVT variations in the pseudo circuit are calculated by our method. The PVT variations for the DUT are determined by the CMOS technology. We used a variation in L only, with 3σ equal to 30% of the nominal value.

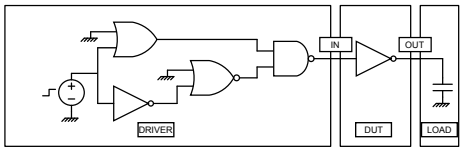
The circuit of the first simulation setup for an inverter (INV X1) is shown in Fig. 6a, and referred to as *target simulation setup*. Here an inverter is placed inside the DUT block and a capacitive load is added into the load block. A realistic driver circuit with multi input switching along with interconnect modelled with capacitance is used in the experiment. An ideal ramp is fed to the driver circuit. The inverter of the DUT block is replaced by other standard cells for the simulations. All experiments use single input switching for the DUT, unused inputs are tied to an appropriate constant. The signal slew of the ideal voltage signal generator and the output capacitive load is kept fixed for all different standard cells.

The circuit of the second simulation setup for the same inverter (INV X1) is given in Fig. 6b, and referred to as *model simulation setup*. The only difference between the target and the model simulation setup is in the driver circuit. The sizing of the inverters and internal capacitors in the pseudo circuit are decided while developing the pseudo circuit model. In this case, the sizing of the inverters in the pseudo circuit does not match with any of the standard cell inverters. Additionally, only the last inverter in the pseudo circuit has

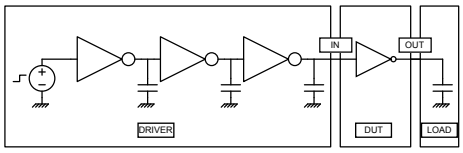
TABLE I: Error % comparison in mean and SD of delay and slew of the 45nm standard cells due to pseudo circuit model

		Delay Mean (ps) (μ)			Delay SD (ps) (σ)			Slew Mean (ps) (μ)			Slew SD (ps) (σ)		
Circuit	**Strength**	**Target**	**Model**	**Error**	**Target**	**Model**	**Error**	**Target**	**Model**	**Error**	**Target**	**Model**	**Error**
INV	X1	79.44	77.68	2.22	10.75	10.86	1.08	104.96	102.86	2.00	13.06	13.24	1.39
BUF	X1	67.60	67.69	0.12	8.76	8.75	0.07	70.54	70.42	0.17	6.62	6.66	0.58
NAND2	X1	81.40	79.48	2.36	11.07	11.18	1.00	107.00	105.08	1.79	13.38	13.66	2.13
NOR2	X1	96.29	94.23	2.13	13.37	13.45	0.58	139.44	137.98	1.05	18.81	19.00	1.01
AND2	X1	71.62	71.54	0.11	9.19	9.15	0.46	70.75	70.58	0.25	6.77	6.64	1.95
OR2	X1	74.40	74.39	0.01	9.85	9.82	0.28	71.71	71.63	0.11	6.92	6.84	1.26
XNOR2	X1	86.56	87.08	0.60	11.11	11.19	0.68	95.16	95.31	0.16	9.61	9.71	1.09
XOR2	X1	100.19	97.52	2.66	13.99	14.00	0.09	144.46	142.51	1.35	19.47	19.71	1.21
BUF	X2	58.12	57.97	0.26	8.25	8.25	0.10	37.77	37.63	0.36	3.46	3.39	1.92
NOR2	X2	65.14	63.43	2.62	8.78	8.82	0.49	83.89	81.73	2.57	9.51	9.86	3.59
AND2	X2	61.51	61.08	0.70	8.61	8.60	0.17	38.17	37.98	0.48	3.50	3.44	1.71
OR2	X2	65.61	65.27	0.52	9.55	9.50	0.47	40.13	39.93	0.51	3.91	3.86	1.51
XNOR2	X2	75.34	76.32	1.30	10.63	10.90	2.59	53.70	53.79	0.16	5.51	5.51	0.01
XOR2	X2	69.18	66.85	3.36	9.35	9.34	0.19	89.01	86.39	2.95	10.22	10.44	2.14

L variation whereas each MOSFET in the target simulation setup has PVT variations. The pseudo circuit parameters are selected such that the PSoWs at IN of both the simulation setups match.



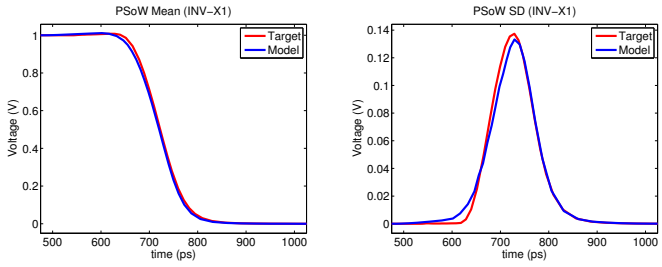
(a) Target simulation setup



(b) Model simulation setup

Fig. 6: Experimental Setup for INV X1

In this example (DUT = INV X1), the mean and SD curve of target and model PSoW are plotted in Fig. 6a and Fig. 6b. The error in the quality factors of these two set of PSoW's, Q_{Slew}, $Q_{ShiftMean}$, Q_{Max}, and Q_{Tmid} are 1.06%, 7.09%, 2.98% and 0.28% respectively. Additionally, the mean value of the delay of DUT in target and model simulation is 79.44ps and 77.68ps respectively with an error of 2.22%. Similarly, the SD of the delay in both setups is 10.75ps and 10.86ps respectively with an error of 1.08%. The mean value of the output signal slew of DUT in both models is 104.96ps and 102.86ps respectively with an error of only 2.00%. The SD of the slew is 13.06ps and 13.24ps with an error of only 1.39%. These data shows that the error in the delay and slew variation estimation for INV X1 is within 2.5%. Similar results due to various other standard cells are reported in Table I.



(a) Mean Comparison (b) SD Comparison

Fig. 7: Mean and SD Comparison for INV X1

The above results show that a compact implicit model with only five model parameters can effectively reproduce the target PSoW's. The error introduced by the substitution of the original driver circuit by the pseudo circuit model in the delay and slew mean and SD estimation is within 3.5%.

V. Conclusion

This paper proposes a very compact implicit model to represent a probabilistic set of waveforms (PSoW) using a pseudo circuit model. This pseudo circuit model is based on a reference circuit with five parameters. By tuning these parameters, various possible PSoW can be generated. Experiments have been carried out to estimate the error introduced by the substitution of the pseudo circuit model in comparison with the original PSoW on 45nm based Nangate standard cells. The experiments show that the error introduced by the pseudo circuit model on the mean and standard deviation of the delay and slew are within 3.5%. In the future, we will try to improve the model further to reduce the error in the variance estimation.

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