2D AND 3D INTEGRATION WITH ORGANIC AND SILICON ELECTRONICS

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Track A5. Energy Generation, Recovery and Management Systems

Abstract—**Organic electronics, such as OLEDs, OPVs, and polymer based power storage units (batteries and capacitors) are rapidly becoming low-cost viable alternatives to silicon-based devices. These organic devices however, are still reliant on the support functions of standard silicon components such as power and logic transistors. Integration of these organic devices with standard silicon electronics into a combined heterogeneous system requires specific design and fabrication considerations. Full-scale integration with conventional silicon based electronic components is challenging due to their incompatibility with common semiconductor fabrication process that can damage the active organic compounds. The printable/spray/spin nature of organic electronics fabrication makes 3D integration an attractive methodology. We propose to combine the organic and inorganic portions of a heterogeneous system by fabricating the modules separately (hence enabling parallel manufacturing) in a specific 2D layout scheme, and subsequently connecting the devices together in a post fabrication process. In this paper we discuss the 2D designs in detail and propose a 2D-3D hybrid design as well as a fully 3D stacked design for organic electronics with energy storage devices in a face-to-back configuration. The fabrication process of each device and the integration of OPVs and OLEDs with power storage devices are discussed. An overview of test procedure and fault tolerances for the proposed configuration is provided. Finally, a potential solution for a new test environment derived from a mixed configuration of different technologies and materials is proposed.**

Index Terms— **3D Integration, Organic Electronics, Interconnects, Photovoltaics, Polymer Battery, Capacitor, OLED.**

1 Introduction - Challenges in Organic Electronic Fabrication

Organic electronics have some unique characteristics such as being flexible, transparent and low cost, which makes them a promising candidate for many future electronic applications [1]. Nevertheless, their full-scale integration with other conventional electronic components is very challenging due to their incompatibility with the common semiconductor fabrication processes that can damage the active organic compounds. For this reason, using organic devices such as organic photovoltaics (OPVs) or organic light emitting diodes (OLEDs) with conventional energy storage devices remains highly challenging. OPVs and OLEDs are created using wet chemical processing fabrication methods. Our previous work on OPVs, and fabrication steps have been described in detail elsewhere [2].

The most attractive process for 3D devices is using monolithic fabrication, where the devices are fabricated successively on top of each other. Monolithic fabrication offers the lowest potential cost, with fewest potential steps. However since silicon based processing, such as chemical etching or high temperature annealing, can destroy the active organic layers, a fully monolithic fabrication process is not likely. For these aforementioned reasons, 2D configurations or other 3D approaches are considered and discussed.

2 Proposed 2D and 3D Organic-Silicon Configurations

2.1 2D integration of organic devices

As a way to incorporate both types of electronics, one can use a 2D layout where organic and silicon based devices are connected together. As an example, if solar cell units are to be integrated with power storage units in a functional way, these devices have to be fabricated separately and later connected side by

978-3-9810801-7-9/DATE11/©2011 EDAA

side as depicted in Figure 1. One potential drawback to the standard 2D layout is relatively long interconnects (ICs) between the organic devices and power storage units which may result in small but significant energy losses diminishing the use of the solar cell [3]. Furthermore, as OPVs suffer from relatively poor power conversion efficiencies (~1%) [4], in contrast to their silicon counterparts, relatively large surface areas are required to harvest enough energy to power up any electronic device. Consequently, effective use of the available surface area is vital.

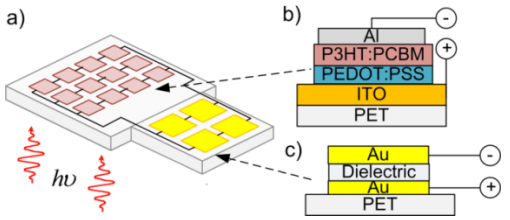

Figure 1: a) An example of a 2D electronic circuit made of organic photovoltaic arrays connected to an array of capacitors acting as an energy storage device. Schematics of b) an OPV and c) a polymer capacitor.

We propose 3D stacking of organic electronics such as OPVs and OLEDs with energy storage devices in a face-to-back configuration to overcome the potential drawbacks of the 2D configurations. The fabrication process of each device and the integration of OPVs with polymer capacitors are discussed in detail. We also show how this basic configuration and approach could be expanded to other organic devices such as OLEDs. Developing testing procedures for the proposed configurations is necessary and is detailed to include fault models.

2.2 Face-to-back 3D integration of organic devices

One method of addressing the 3D monolithic process problem is to adopt a face-to-back approach, where isolated devices are brought in contact with each other [5-7]. In contrast with the 2D technique, this approach has the advantage of allowing different fabrication processes to be used for making separate components on a single device. The IC lengths are also reduced and optimization of the available surface area can be achieved. Figure 2a displays the 3D approach where OPVs are stacked in a face-to-back way with a capacitor. The same approach can also be used to integrate OLEDs with capacitors as shown Figure 2b.

Figure 2a displays two OPVs mounted on top of a single capacitor, this 3D stacking can be expanded to arrays of capacitors and OPVs in series or parallel. Ideally, each single array of OPVs or OLEDs can be directly connected to an array of capacitors in an autonomous and selective way. Numerous ICs spanning across the whole sample are no longer needed, which consequently decrease device complexity and energy lost in the ICs. When the capacitor is fully charged the power may be converted to recharge a battery located elsewhere.

The 3D assembly proposed can also be imagined as a power harvesting and storage unit for low power autonomous electronic devices. Figure 3 illustrates this concept with OPVs and capacitors used to supply power for two OLEDs. Using Al vias through the base substrate allows testing of 3D integrated organic electronics, such as the one depicted in Figure 3, without altering the base. This prevents any alteration of the organic active layers and direct probing of device performance at each level for each component can be done in real time.

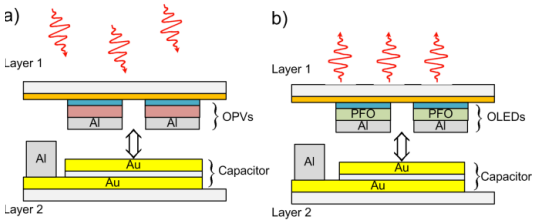

Figure 2: An example of a 3D integration of capacitors with a) OPVs, and b) OLEDs.

Nevertheless, the device displayed in Figure 3 is not yet fully functional. A controller is needed to allow smart management of the available energy as follows:

i) in the absence of solar radiation, the OLEDs are powered uniquely by the capacitors,

ii)when the OLEDs are not turned on, the OPVs are used to recharge the capacitors,

iii) For long usage period, all components operate at the same time allowing the OLEDs to be powered up by both the capacitors and the OPVs.

With the 3D approach as presented in this work, the power controller components can be added using conventional semi-conductor fabrication processes on layer 2 prior to 3D stacking.

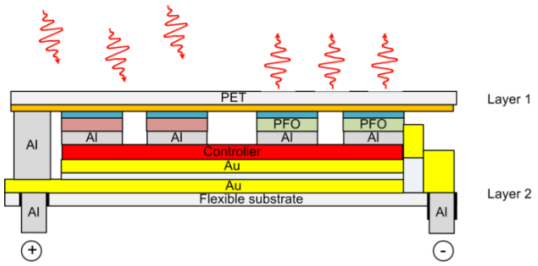

Figure 3: Schematic of the proposed 3D stacking of OLED/OPVs components with capacitors.

Measuring fault tolerance of individual components requires access to a large number of test points. While micro-probing on standard-sized test pads can be used for validation prior to packaging, and post-packaging testing can be accessed through device pin-outs, the accessibility of these test points are often costly and cumbersome due to the small dimensions of the devices. The flexible nature of the organic layers allows printed test connectors [8] to be applied replacing manual or even automated probing, for larger throughput testing. More precisely, a large number of test I/Os can be routed from the specific test points along the OPV/OLED arrays to a high-density bus, then subsequently fanned-out to individual connection tracks matching the pitch of the connector ports of a suitable external test interface (see Figure 4a). Testing of individual layers prior to assembly can be accomplished using a similar set of fault models developed in Table 2, while final testing and validation of the 3D stacked structure can also benefit from built-in test access point connectors. Upon verification of each individual layers the printed micro-connectors can be detached using cutting tools, and individual layers can be combined and assembled into the final 3-D stacked configuration (see Figure 4b). Designated test microconnectors can remain after stacked assembly post-integration tests and controller configurations.

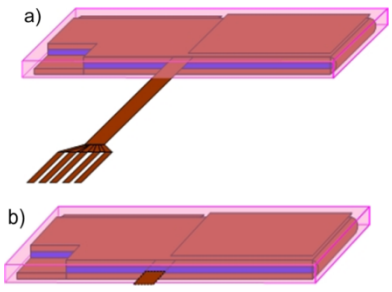

Figure 4: Example of printed microconnectors for built-in test point access: a) connector bus carrying test signal lines out to test interface; b) connector removed in preparation for 3-D stacked assembly.

3 Design and Characterization of IntegratedElectronics

Organic electronics give the designer more flexibility and the application constraints must be considered carefully. For example fabrication of an OPV on a polymer such as PET will yield a device with less power conversion efficiency then one a rigid glass substrate, but it will have added benefit of being very thin and flexible.

3.1 Organic component results

Our previous work on OPVs, and fabrication steps have been described in detail elsewhere [2], therefore only a brief description of the process will be giving here. Following a thorough cleaning in sodium hydroxide (NaOH), acetone, 2-propanol and deionized water, the indium tin oxide (ITO)-coated polyethylene terephthalate (PET) samples were subjected to poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (H. C. Starck, PEDOT:PSS,) spin coating at 2000 rpm. The substrates were then transferred onto a hotplate and dried at 110 ^{o}C in air for 15 min. The active polymer solution consisting of a blend of poly(3-hexylthiophene) (P3HT, Ricke-Metals) and phenyl-C61-butyric acid methyl ester (PCBM, Nano-C) in chlorobenze(anyhydrous, Sigma-Aldrich) was subsequently spin-casted at 700 rpm in air on top of the PEDOT:PSS layer. The samples were then covered with a petri-dish and allowed to dry for 20 min. Finally, the cathode contacts were made by either using small drops of eutectic Ga-In in air or by thermal evaporation of aluminum on top of the polymer active layer (see Figure 5). Fabricated OPVs with I-V results are shown in Figure 5. The maximum power conversion efficiency and device characteristics of the ITO-OPVs with no post-annealing on PET in air are reported in Table 1.

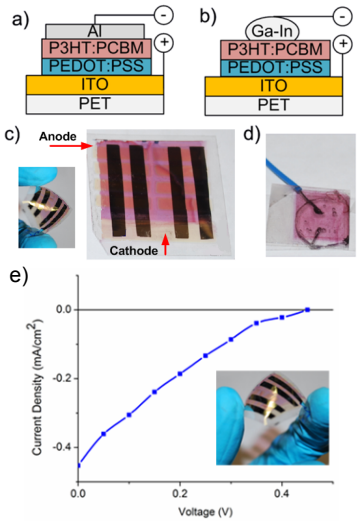

Figure 5: Schematic of the organic photovoltaic devices using a) aluminum and b) eutectic Ga-In cathodes. Photography of the OPVs with c) Al and d) Ga-In contacts. e) Optical image of an OPV made on PET (inset) with I-V curve at 1 SU.

Polymer-metal composite capacitors were fabricated from 30cmx30cm sheets of Nafion® N-115 membranes exhibiting levels of capacitance of 1 mF cm^{-2} or 40 mF/g (defined as the weight of active materials Nafion and Au). The Nafion® N-115 membranes have a mean nominal thickness of 127µm. The design and fabrication of these capacitors has been reportedly in detail elsewhere in the literature [10-11].

Table 1: Device performance summary for the ITO-OPVs

	V_{oc} (V)	J_{sc} (mA/ cm^2)	F.F. (%)	E_{ff} (%)
ITO-OPVs	0.45	0.45	29	0.59

3.2 2D configuration test results

Two-terminal current-voltage (*I-V*) measurements on OPVs fabricated on PET substrates were performed. The samples were first measured in the dark and thereafter exposed to 1 SU illumination. Several tests on the post fabricated OPVs show open-circuit voltages of V_{oc} = 0.46 V, short-circuit currents of I_{sc} =3.2 mA/cm2, and fill-factors of ~51%. Power conversion efficiencies up to 0.59% were achieved.

Testing of the integrated 2D system was initiated by connecting a capacitor to an OPV according to Figure 6a, and ambient light room of 0.4 W/ m^2 was used as power source for the OPV. Measurement of the charge and discharge of the capacitors was done by connecting aNational Instruments DAQ module with Labview to the setup allowing for real-time monitoring.

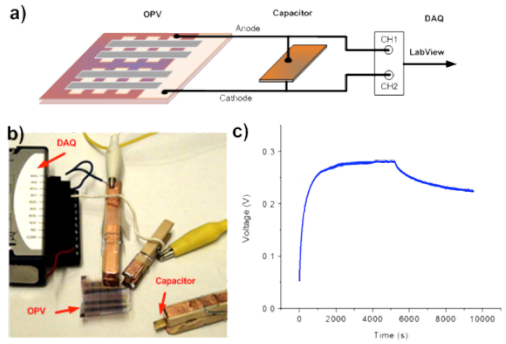

Figure 6: 2D system under test: a) diagram, and b) laboratory configuration of the test setup. c) charge/discharge curves of a IMPC capacitor.

3.3 Fault tolerance design and test

Due to the sensitivity of organic active layers to oxygen and humidity, defects are common causes of faulty devices and remain as one of the biggest challenges. Metals such as aluminum can oxidize upon contact with air creating a dielectric Al_2O_3 layer. Flexible substrates have a lower potential yield compared to that of substrates such as glass or silicon due to surface bumps and non-uniformity. PET for an example has a mean surface roughness of ~ 40 nm, which dramatically alters the uniformity of the PEDOT:PSS layer during the spin casting process. Without a uniform electron blocker layer carrier recombination can occur causing poor device performance or failure.

In solar cells, where serial connections of cells are common, a faulty cell will render the device useless. To overcome this issue bypass diodes are needed and are connected in parallel with each cell as shown in Figure 7a.

In such configuration, for a defect free OPV the internal resistance is much smaller than the intrinsic resistance of the diode, allowing the current to flow through the OPVs. In the event of a damaged or shaded OPV cell, the internal resistance of the solar cell becomes much larger than the diode, causing the current to deflect to the diode. In addition, any shaded part of the OPV modules should be considered as resistors where most of the power collected by the illuminated cells is deflected to the shaded cells. To prevent this behaviour blocking diodes may be installed between parallel modules as depicted in Figure 7a.

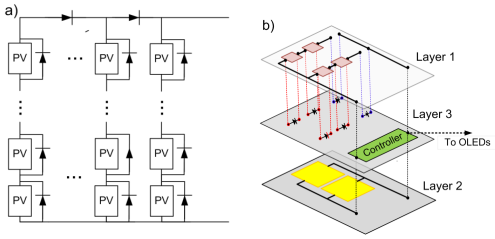

Figure 7: Schematic of a) OPV arrays with bypass and blocking diodes, and b) 3D stacking of OPVs/ capacitors with diodes and controller.

The 3D model presented here allows a straightforward integration of additional components such as diodes. These new modules can be incorporated with the controller as a third layer (layer 3) as depicted in Figure 3. In this way, external probing and monitoring of faulty OPVs can be achieved without altering any components in layer 1 and layer 2.

A list of common fault models must be determined for each organic electronic component. As an example fault models for OPVs are listed in Table 2.

Table 2: Fault model for organic solar cells.

Fault	Description	Diagnostic
Device failure	Device ceases to work due to component failure or organic layer degradation (for OPVs).	$V_{oc}\approx 0$, $I_{sc}\approx 0$ and high serial resistance. Efficiency is effectively zero.
Light source shading	The photoactive area is not uniformly/ completely illuminated.	High resistance in cell and lower efficiency than expected.
External electrical contacts	Contacts to the anode or cathode are defective.	I_{sc} sensitive to vibration and very low. Serial resistance high. V_{oc} normal.
Quality of intrinsic contacts (e.g. Al for OPVs)	Poor deposition of the metal cathode.	Very low serial resistance (< 200 Ω) and absence of the diode-like behavior.

4 Conclusions

Organic electronics, such as OLEDs, OPVs, and polymer based power storage units (batteries and capacitors) are rapidly becoming low-cost viable alternatives to silicon-based devices. These organic devices however must be integrated with standard silicon components such as transistors and interconnects. Integration of these organic devices with standard silicon electronics while capturing the benefits of these devices is not straightforward. 2D and 3D design configurations were presented along with basic fault models for organic components and 2D configuration device testing. The 2D layout was shown to required relatively long interconnects (ICs) between the organic devices and the power storage units resulting in excessive energy lost, significantly reducing the function. OPVs that suffer from low power conversion efficiencies (<10%) require larger surface area to harvest sufficient energy. Even small losses between interconnects may have a significant impact on device function. Effective use of the available surface area is vital which makes the 2D design approach unrealistic for real world devices. Future implementations of the 3D back-to-back configuration presented here may overcome the drawbacks of the simple 2D configuration.

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