An LOCV-based Static Timing Analysis Considering Spatial Correlations of Power Supply Variations

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***Abstract*—As the operating frequency of LSI becomes higher and the power supply voltage becomes lower, the on-chip power supply variation has become a dominant factor which influences the signal delay of the circuits. The static timing analysis (STA) considering on-chip power supply variations (IR-drop) is therefore one of the most crucial issues in the LSI designs nowadays. We propose an efficient STA method to consider on-chip power supply variations in the static timing analysis by utilizing the spatial correlations of IR-drop. The proposed method is based on the widely-used technique in STA considering OCV (on-chip variations), which is called LOCV (Location-based OCV) technique, and therefore our method is easy to be incorporated into the existing timing analysis flow. The proposed method is evaluated by using test data including H-tree clock structure with various on-chip IR-drop distributions. The experimental results show that the proposed method can reduce the design margin with respect to power supply variations by 6-85% (47% on the average) compared with the conventional practical approach with a constant OCV derating factor, while requiring no additional computation cost in the static timing analysis. Thus the proposed method can contribute to a fast timing closure considering on-chip power supply variations.**

Keywords-static timing analysis; power supply variation; OCV

I. INTRODUCTION

The static timing analysis (STA) considering on-chip power supply variations has become one of the most crucial issues in the LSI designs because of the higher operating frequency and the lower power supply voltage. There have been a lot of researches which address the issue of STA considering on-chip power supply variations. References [1, 2] propose methods to calculate the maximum path delay considering power supply variations. In [3], a delay calculation method, where the delay maximization problem is formulated as a non-linear optimization problem, is proposed. Reference [4] proposes a method to analyze critical path delay considering dependencies between temperature, power consumption, leakage current, and power supply variation. Reference [5] proposes an STA method where spatial and temporal power supply variations are handled statistically. Although these conventional methods are supposed to give a high accuracy in STA considering power supply variations, it has been difficult to adopt these approaches to full-chip STA in a very large scale design iteratively until timing closure because of the limited design period. Therefore, a fast static timing analysis considering power supply variations, which has very little additional cost to the existing timing analysis flow, is highly demanded. In response to this demand, a practical method which applies a constant derating factor based on the maximum IR-drop has been widely used. This approach, however, is very pessimistic because it assumes an extreme situation with respect to IR-Drop [3, 5].

In this paper, we propose an efficient STA method in which the spatial correlations of on-chip power supply variations are incorporated into the widely-used technique in STA considering OCV (on-chip variations), which is called LOCV (Location-based OCV, also known as AOCV or Advanced OCV) technique [6, 7]. The proposed method is described in Section II, and the experimental results using test data including H-tree clock structure are shown in Section III. Finally, conclusions are drawn in Section IV.

II. PROPOSED STA METHOD

We propose a new STA method, in which the spatial correlations of the on-chip power supply variations are incorporated into the conventional LOCV technique. The flow of our method is illustrated in Fig. 1.

First, the voltage-delay property, which is the relationship between IR-drop (voltage drop) and delay increasing rate is characterized by using Spice simulation. Next, the on-chip distribution of IR-drop is extracted by using an IR-drop analysis tool. Then, the correlation between IR-drop and distance is extracted from the on-chip distribution of IR-drop, and an equation relating IR-drop to distance is derived. Then, the equation relating *delay* to distance is derived and LOCV table is constructed. Finally, static timing analysis is performed by using the LOCV table. Note that the characterization is performed once for each technology, while the steps from IR-drop analysis to STA are performed for each design.

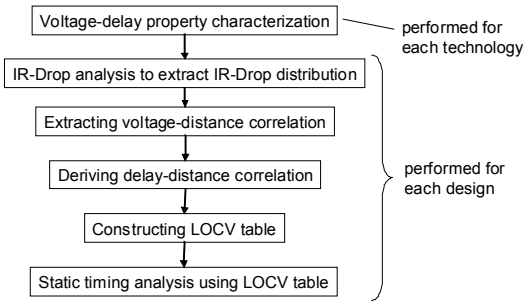

Figure 1. Flow of proposed method.

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A. Characterization of Voltage-Delay Property

The voltage-delay property, which represents the relationship between IR-drop and delay increasing rate, is characterized for a representative clock buffer in the target technology by using Spice simulations. The delay increasing rate per unit voltage drop is calculated as follows:

$$R_{vd} = \frac{d(V_{nom} - \Delta V_c) - d(V_{nom})}{d(V_{nom})\Delta V_c}, \quad (1)$$

where R_{vd} is the delay increasing rate per unit voltage drop, $d(V)$ is the delay of the buffer with power supply voltage V, V_{nom} is the nominal power supply voltage, and ΔV_c is the amount of voltage drop used in the characterization.

B. IR-drop Analysis

First, the IR-drop analysis is performed by using an IR-drop analysis tool. Next, sample instances (function blocks) are selected from the design, so that the selected sample instances are scattered all over the chip layout area. Then, the average IR-drop, which is the static IR-Drop or the temporal average of the dynamic voltage drop, is extracted for each sample instance. Note that, in [8], it is shown that the path delay increase mainly depends on the temporal average of the dynamic voltage drop and that the shape of the IR-drop waveform has little impact on the delay increase.

C. Extracting Correlation Between IR-drop and Distance

The correlation between IR-drop and distance is extracted by using the above IR-drop analysis results as follows: First, the locations of the sample instances are extracted from layout design data. Next, for each of the combinations of any two sample instances, the distance and IR-drop difference between these two instances are calculated. Then, the distance and IR-drop difference of each instance pair is plotted on a graph, and the equation relating IR-drop to distance is derived as shown in Fig. 2. An example of this equation is shown below.

$$\Delta V(L) = aL^2 + bL + c \quad (2)$$

Here, L is the Euclidean distance between two instances, $\Delta V(L)$ is the voltage difference with respect to distance L, and a, b, and c are the coefficients to be fitted.

D. Deriving Correlation Between Delay and Distance

The correlation between IR-drop and distance extracted in the previous step is then transformed into the correlation between delay and distance by using the voltage-delay property as follows:

$$D(L) = R_{vd}\Delta V(L). \quad (3)$$

Here, $D(L)$ is the delay increasing rate with respect to distance L.

E. Constructing LOCV Table

In the LOCV technique, the OCV derating factor is calculated based on the relationship between delay variation and distance, and the resultant derating factors are listed on a table, which is called *LOCV table* as shown in Fig. 3. As well as the process variations, the power supply variations also have a correlation with distance [5]. Therefore, we incorporate the relationship between distance and the delay variation caused by IR-drop into the LOCV table.

The OCV derating factors are calculated as follows: First, the OCV derating factors considering process variations are calculated by using the conventional methods [7]. Next, the OCV derating factors for capture paths in the hold analysis (or the launch paths in the setup analysis) are multiplied by (1+ $D(L)$). Note that the proposed method does not necessarily give the delay of each path under the IR-drop occurred at the corresponding path. The purpose of our method is to calculate the *relative* delay between capture and launch paths considering IR-drop.

F. Performing STA Considering On-Chip Variations

Once the LOCV table is constructed for the target design, the STA is performed in the same manner as the conventional LOCV technique. This makes our method very easy to be incorporated into the existing timing analysis flow, and no additional computation cost is required in STA compared with the conventional LOCV technique, which contributes to a fast timing closure considering IR-Drop.

III. Experimental Results

In order to evaluate our method, we made test data which include H-tree clock structure [9] for 40nm process technology as shown in Fig. 4. The X-Y coordinate system, where the unit

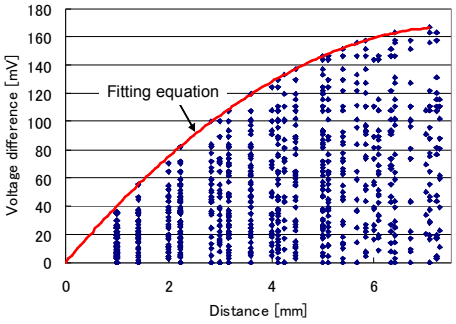
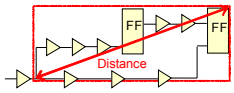


Figure 2. Correlation between voltage difference and distance.



Distance \ #Stages	0	1	2	3	4
0mm	1.15	1.16	1.17	1.18	1.19
1mm	1.14	1.15	1.16	1.17	1.18
2mm	1.13	1.14	1.15	1.16	1.17
3mm	1.12	1.13	1.14	1.15	1.16
4mm	1.11	1.12	1.13	1.14	1.15

Figure 3. Example of LOCV table.

of length is millimeter, is specified so that the left-bottom edge of the chip is the coordinate origin. The chip size is 8mm x 8mm, the nominal power supply voltage is 1.0V, and the clock frequency is 200MHz. The clock buffer size is 16 times as large as the minimum clock buffer size of the technology. In the experiments, HSPICE was employed for Spice simulations.

We used two pairs of launch and capture paths for hold analysis in which two flipflops in each pair are close to each other in order to evaluate the hold-critical cases. The first pair (referred to as *Path-pair 1*) includes the launch flipflop *FF1* and the capture flipflop *FF2*, while the second pair (referred to as *Path-pair 2*) includes the launch flipflop *FF3* and the capture flipflop *FF4*, as shown in Fig. 4. Here, each launch path includes the data path from the launch flipflop to the capture flipflop. In each of these path-pairs, the capture path is supposed to go through areas with larger voltage drops than the launch path, and thus the hold time tends to become critical by the IR-drop. The path distance is defined as the diagonal length of the minimum rectangular surrounding the corresponding path-pair, which is the same as the conventional LOCV technique. The path distances for Path-pair 1 and Path-pair 2 are 5.48mm and 1.25mm, respectively.

A. *IR-drop distribution*

We employed the triangular waveform for power supply voltage waveforms, where the noise width is equal to the clock cycle. The ground voltage was assumed to be constantly zero for simplicity. We used three types of on-chip power supply variations (IR-drop distributions). All the types have a hot spot at the coordinate (2, 2), where the IR-drop is maximized. The peak IR-drop (the peak voltage drop value of the voltage waveform) at the hot spot was set to 300mV, which is 30% of the nominal power supply voltage. (Usually, very large IR-drops are alleviated in the layout design phase. Therefore we think that the maximum IR-drop value of 300mV is an appropriate assumption.) Accordingly, the temporal average of voltage drop at the hot spot is 150mV.

The first IR-drop distribution (referred to as *Type 1*) is a linear distribution, in which the IR-drop is linearly decreased with the distance from the hot spot. The second and third IR-drop distributions (referred to as *Type 2* and *Type 3*, respectively) are exponential distributions, in which the IR-drop is exponentially decreased with the distance from the hot spot. These IR-drop distributions are expressed as follows:

$$\Delta V_l(x,y) = 150\left(1-\sqrt{(x-x_h)^2+(y-y_h)^2}\,/\left(6\sqrt{2}\right)\right)$$
$$\Delta V_e(x,y) = 150\exp\left(-\alpha\sqrt{(x-x_h)^2+(y-y_h)^2}\right) \quad (4)$$

Here, $\Delta V_l(x, y)$ and $\Delta V_e(x, y)$ are the IR-drops (the temporal average of voltage drop) at the location (x, y) in the linear distribution (Type 1) and the exponential distributions (Type 2, 3), respectively. (x_h, y_h) is the location of the hot spot. α is a coefficient which was set to 0.25 and 0.5 for the second (Type 2) and third (Type 3) distributions, respectively. In (4), the unit of voltage is millivolt and the unit of distance is millimeter. These IR-drop distributions are illustrated in Fig. 5.

B. *STA by proposed method*

First, the voltage-delay property was characterized by Spice simulations. The representative clock buffer is the same as the clock buffer used in the H-tree structure described above. The delay increasing rate per unit voltage (R_{vd}) was calculated by using (1), where ΔV_c was set to 50mV.

Next, the OCV derating factors for IR-drop distributions Type 1, 2, and 3 were calculated by using (3) and (4). The OCV derating factors are listed on Table I. Note that, if the conventional practical approach which uses a constant OCV derating factor based on the maximum IR-drop is applied, the OCV derating factor (with respect to IR-drop) is 1.216. (The maximum IR-drop in this case is 150mV, which is the temporal average of the dynamic IR-drop at the hot spot.)

In the experiments, the nominal path delay, which is the path delay with the nominal power supply voltage, was calculated by Spice simulation, thus excluding the calculation error of the STA tool. Then, the nominal delay of the capture path was multiplied with the corresponding OCV derating factor (with respect to IR-drop) listed on Table I to obtain the path delay with on-chip power supply variations. Note that process variations were omitted in this experiment for

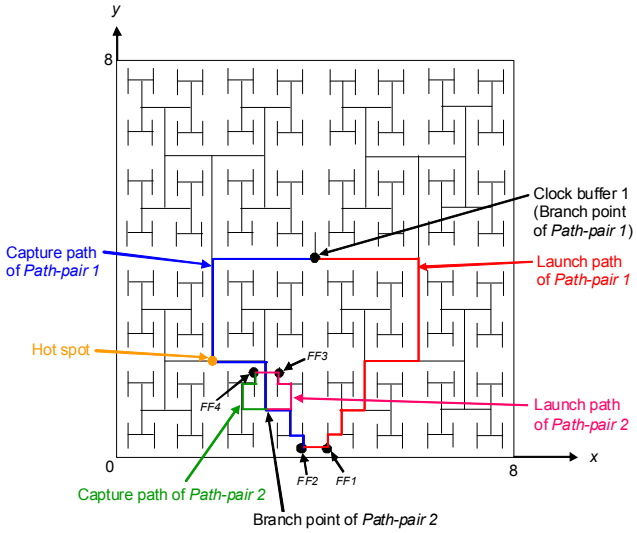


Figure 4. H-tree clock structure.

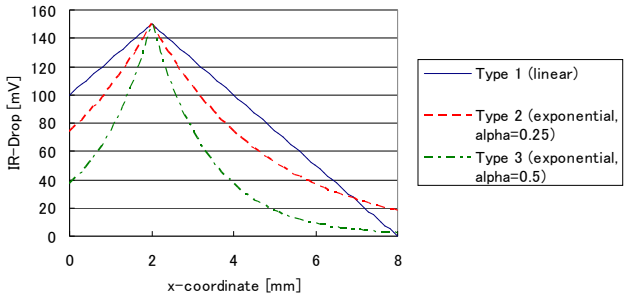


Figure 5. Three types of IR-drop distributions on chip.

simplicity. Also, we calculated the reference path delays under the dynamic voltage drop by Spice simulations.

As the purpose of our method is to calculate the relative delay between capture and launch paths, we specified the ratio of capture and launch path delays as the criterion to evaluate the accuracy of the proposed method. The criterion is the ratio of the capture path delay divided by the launch path delay, which we call the *path delay ratio*. If the path delay ratio is larger than one, the capture path delay is larger than the launch path delay, which means that the hold time constraint is violated. Also, if the path delay ratio given by the proposed method is smaller than that by Spice simulation (reference), the proposed method is too optimistic.

The path delay ratios by the proposed method were compared with those by Spice simulations (references) and those by the conventional practical method in which a constant OCV derating factor assuming the maximum IR-drop (150mV) is employed. The results are shown in Fig. 6 and Fig. 7. In all the cases, the path delay ratio by the proposed method is larger than the reference and smaller than that given by the conventional practical method with a constant OCV derating factor, which means that the proposed method reduces the extra design margin (pessimism) of the conventional method and still it is not too optimistic. The proposed method reduced the design margin, which is defined as the difference between OCV derating factor and one, by 6-85% (47% on the average). Also, the proposed method achieved a 23-98% (69% on the average) improvement on the accuracy of calculating the path delay ratio compared with the conventional practical approach while requiring no additional computation cost in STA.

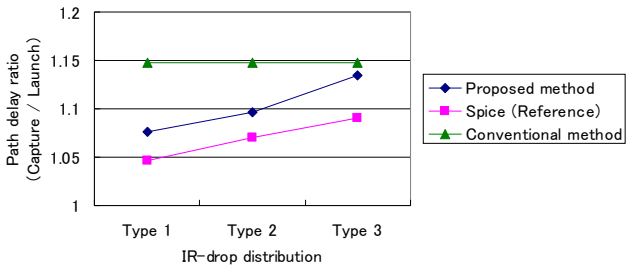


Figure 6. Path delay ratio of Path-pair 1.

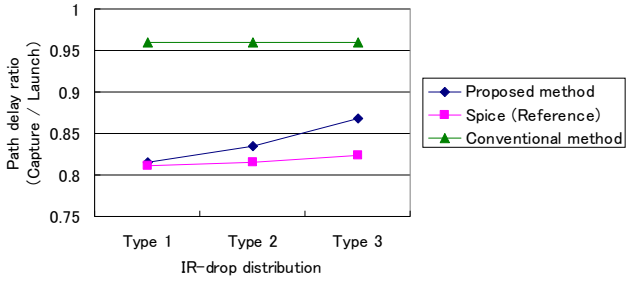


Figure 7. Path delay ratio of Path-pair 2.

TABLE I. OCV DERATING FACTORS

IR-drop distribution	Path-pair 1 (L=5.48mm)	Path-pair 2 (L=1.25mm)	Conventional method
Type 1	1.139	1.032	1.216
Type 2	1.161	1.058	
Type 3	1.202	1.100	

IV. CONCLUSIONS

We have proposed an efficient method to consider on-chip power supply variations (IR-drop) in the static timing analysis. Our method incorporates the delay variation caused by IR-drop into the LOCV technique by utilizing the spatial correlations of on-chip power supply variations. The proposed method was evaluated by using test data including H-tree clock structure. The experimental results show that the proposed method can reduce design margin with respect to power supply variations by 6-85% (47% on the average) compared with the conventional practical approach with a constant OCV derating factor, while requiring no additional computation cost in STA.

Future works will be directed toward the validation of the proposed method by using actual design data.

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