Strategies for Initial Sizing and Operating Point Analysis of Analog Circuits

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***Abstract*—This work presents novel analog sizing flows based on analytical techniques. A graph-based operating point driven sizing approach provides operating point voltages and a rough sizing with respect to constraints. A voltage-range analysis method using linearized operating-point models obtains information about feasible voltage ranges. A direct-sizing method solves nonlinear algebraic circuit equations directly to obtain design parameters from specifications. All three methods require no or only minimum simulation effort and can provide quick insight into circuit design space and constraints in an early design stage. They allow flexible inclusion into state-of-the-art simulation-based optimization flows, where they lead to improved results with less optimization effort and prevent unnecessary simulation effort on unfeasible circuit topologies. The sizing flows are enhanced by a commercial optimization tool in order to obtain reliable circuits.**

I. INTRODUCTION

Reuse of analog circuit blocks is increasingly important to meet the demand for continuous improvement of design efficiency, for example by shortening the time for the migration from one semiconductor technology to another one or by redefinition of the circuit specification. The reused blocks have to be resized, as a one-to-one transfer is hardly possible. Moreover, the fulfillment of constraints (e.g. saturation of MOS transistors) and feasibility checking of supply voltage ranges or signal swings are crucial to achieve robust circuit implementations. The sizing can take different levels of automation, starting with manual sizing by the designer associated with tedious hand calculations of many equations, up to commercial tools. State-of-the-art methods rely on simulation-based calculation of design parameters (e.g. widths and lengths of transistors) and simulation-based evaluation of constraints for devices or circuit blocks within an iterative optimization loop, e.g. [1] – [6] . These simulator-in-the-loop approaches require multiple simulation runs, causing sophisticated performance estimation techniques that map design variables to performances to obtain fast optimizations [7] – [9]. However, it can not be determined in advance whether there exists a solution. For unfeasible circuit topologies effort in terms of tool-setup time and simulation runtime would be wasted. In addition, the quality of the solution is crucially dependent on the starting conditions. Thus, this work presents sizing strategies consisting of additional tool steps, which effectively analyze the feasibility of a given topology to give the designer additional insight into the circuit with minimum simulation effort. The different strategies provide a good initial sizing as starting point for subsequent simulation-based optimization steps.

The following section provides a brief description of the novel sizing strategies and the analytical methods that constitute them.

II. NOVEL SIZING FLOWS

A. Analytical Sizing Methods

First, an operating point (OP) driven sizing [10] is employed to rapidly find a feasible operating point of the circuit using a graph-based approach [11] for calculation of the node voltages so that the devices fulfill the saturation constraints. The subsequent sizing is based on technology parameters and estimated device currents. If no valid node voltages can be found, the circuit is not feasible for the given supply voltages. The calculations are straightforward, i.e. without iterations as in simulator-in-the-loop approaches. Short computation times are achieved and no complex modeling is required.

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Second, a linearized operating point model (LOP) [12] of MOS devices in saturation is used to formulate a set of linear inequalities, which describe feasible ranges of all circuit node voltages including free nodes (e.g. supply, input) with respect to device constraints. Based on this LOP all voltage ranges can be determined quickly from a single given DC operating point, i.e. information about feasible voltage ranges of free terminal nodes is required to check feasibility of the given structure at specified operating conditions (e.g. supply voltage ranges, input voltage range). Additionally, this approach provides information about circuit elements that limit the targeted specifications.

Finally, direct-sizing is based on setting up nonlinear algebraic DC equations of the circuit and inverting them to obtain design equations. Any transistor length and width to be determined adds a degree of freedom that has to be bound in terms of additional constraints formulated as an equation (e.g. from OP driven sizing derived voltage assignments). Specification parameters (e.g. small-signal gain and bandwidth) are taken into account by inserting them as such constraints while calculating the values for design parameters. Hence, compared to an optimization-based approach direct sizing allows a very fast calculation of element values, and it may be efficiently used to determine the design space of a circuit. Therefore, the strengths of direct-sizing are quick turn-around time and detection of contradictory specifications.

The OP-driven sizing and the direct sizing methods are completely free of external simulations, while the LOP analysis requires a single DCOP simulation. These sizing and analysis methods can be combined to design flows, which give the designer additional insight into the circuit compared to conventional simulation-in-the-loop optimization flows. The proposed methods are integrated in a software infrastructure where technology parameters are provided to the tools in lookup tables (LUTs) [13]. The LUTs contain all relevant parameters required by the algorithms and allow being independent from circuit simulators and PDK device models, which might be of different types (e.g. BSIM3, BSIM4, EKV). In addition, they reduce the number of equations to be solved thus being an ideal substitution for the equation-based transistor models. Two example flows are explained in the following.

B. *Fast Feasibility Flow*

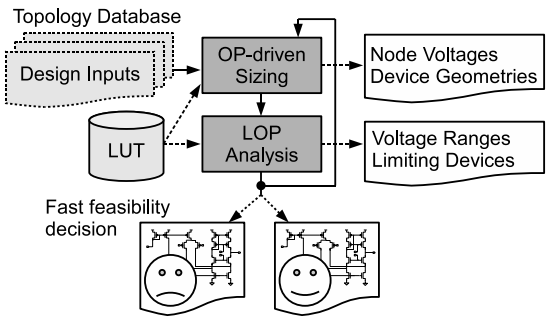

Figure 1. Fast circuit topology feasibility flow

We propose a fast feasibility flow consisting of the OP-driven sizing and the LOP analysis as depicted in Fig. 1. It assists the designer in the decision whether a given circuit topology is feasible with respect to constraints (e.g. saturation of transistors) in a target technology. This is an important issue for analog IP migration to a new technology node. Based on the circuit topology an initial OP driven sizing is performed resulting in defined node voltages and device geometries, whereas free node voltages (e.g. input signals) are estimated in a first step. A subsequent LOP analysis can quickly provide the feasible voltage ranges and feedback for the OP driven sizing by redefinition of the previously defined free node voltages. This gives the designer insight into the voltage range based constraints of the circuit. For example, the feasible input or output voltage ranges can be reported quickly. Reporting the minimum supply voltage leads to a quick feasibility decision of the given topology in the targeted technology. Additionally, the LOP analysis can indicate topology modifications by determining those devices, which limit the targeted voltage ranges. Typical examples are cascoded MOS structures that prevent operation at low supply voltages.

Compared to simulator-in-the-loop approaches the fast feasibility flow avoids simulations and optimization effort for infeasible topologies, thus enabling to explore a large number of circuit topologies from a topology database in a short period of time. In addition to the advice whether a topology is feasible, designer receives information for topology modification in order to meet all voltage ranges, if applicable.

C. *Entire SyEnA-Sizing Flow**

We propose an entire sizing flow that allows determining an initial sizing close to the given specification that may be used as starting point for a subsequent simulation-based optimization. This is a crucial issue since the starting condition has a major influence on the solution of most optimizations. Given a (new) circuit topology the graph-based voltage calculation is performed to obtain values for the node voltages. Subsequently, the direct sizing is applied, whereat the node voltages are used as constraints. After entering all required constraints – i.e. assignments for known voltages, currents and matching information as well as given small-signal specifications – the circuit designer will be able to quickly verify whether the specifications are in the design space of the circuit topology and whether they are consistent. This allows a much better understanding of the circuit. For example, the designer will be able to determine whether the desired gain and bandwidth of an amplifier can be realized for a given current consumption. If not, he receives advices about which parameters are responsible for this. In addition, the LOP analysis can be used to provide feasible voltage ranges. Furthermore, it can be checked whether the sizing operates within the required voltage ranges for inputs, outputs and supply voltages.

However, as analytical initial sizing cannot take into account all performances and full complexity of the devices subsequent sizing and yield optimization may be necessary, here by MunEDA's optimization tool WiCkeD [5]. WiCkeD provides a huge functionality to improve circuit performances and yield, e.g. by Worst-Case-Diagnosis, Monte-Carlo-

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Analysis, stochastic and yield optimization based on global and local process parameter variations.

Using the proposed direct-sizing flow, a quick adaption to new specifications and technologies can be achieved. Prior to the optimization, the analytical methods provide information on which devices and parameters limit the performances and are responsible, that the circuit does not meet the specification. If necessary, the designer can modify the topology instead of a time-consuming optimization step. Moreover, an initial sizing near to the specification avoids optimization effort, thus facilitating WiCkeD to find a good solution.

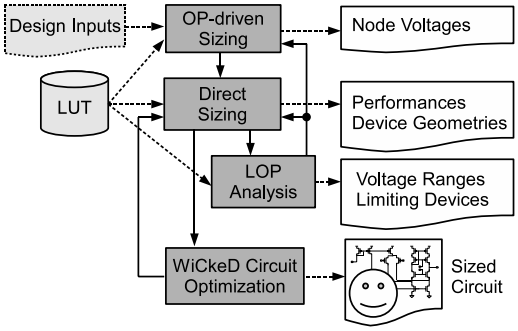

Figure 2. Entire SyEnA-sizing flow with WiCkeD circuit optimization

III. CONCLUSION

Two novel sizing strategies for analog circuits have been presented. They are composed of novel analytical and state-of-the art methods for circuit analysis and sizing. The advantage of the combination of analytical and simulation-based methods consists of using the strengths of the respective approaches. Our methods

- offer fast calculation of feasible operating point without a circuit simulation,
- determine feasible voltage ranges of all circuit nodes from a single given DC operating point,
- reports devices, constraints and parameters that limit the performance or fail the specification,
- offer a near to specification initial sizing as an improved starting point for the optimization,
- avoid simulations, optimization effort and complex modeling, compared to simulator-in-the-loop approaches.

For example, if an amplifier has to be developed in a new technology or adapted for a revised specification the methods support the designer by providing information about necessary topology modifications, i.e. which devices or device parameters are responsible. Furthermore, in contrast to simulator-in-the-loop approaches, the short analysis times enable a rapid investigation which topology from a database would be suitable to solve the task. Nevertheless, simulation-based approaches, such as WiCkeD, provide a huge functionality to further improve circuit performances and yield, which is why they should not be waived. The analytical methods avoid optimization effort by providing a good starting point. Therefore, the presented flows supply a powerful tool for analysis and sizing of analog circuits. They present intermediate results from the research project SyEnA and are currently tested within the scope of the project on industry-relevant circuits.

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