Mathematical approach based on a "Design of Experiment" to simulate process variations

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***Abstract*— this paper describes a Design Of Experiments (DOE) based method used in computer-aided design to simulate the impact of process variations on circuit performances. The method is based on a DOE approach using simple first and second order polynomial models with multiple experiment maps. It is a technology & circuit-independent method which allows circuit designers to perform statistical analysis with a dramatically reduced number of simulations compared to traditional methods, and hence to estimate more realistic worst cases, resulting in a reduced design cycle time. Moreover, the simple polynomial models enable direct linking of performance sensitivity to process parameters. The method is demonstrated on a set of circuits. It showed very accurate results in linking linearity, gain and noise performances to process parameters, for both RF and analog circuit.**

I. INTRODUCTION

Technological advancements in microlithography have fueled the shrinking of minimum device sizes in integrated circuits and particularly in CMOS ICs. In parallel, the weight of process variability tends to increase [1], [2] thus making circuit performance more sensitive to uncontrollable process variations. These variations are random and lead to a spread in the circuit performance. The wider the spread is, the narrower the margin designers will have on their nominal specifications. Circuit designers usually verify the functionality of their circuits under extreme own-minded chosen process conditions which may actually not occur. This method is known as the Worst-case corners analysis. As design specifications and system constraints are becoming tighter in today's RF and analog circuits, in addition of being unrealistic, the Worst-case corners analysis becomes effort and time consuming. Thus, it is obvious that a realistic approach for modeling process variation and mapping it directly to circuit level is becoming mandatory to achieve acceptable yield under reasonable design effort [2]. In this work, we demonstrate a technology-independent DOE-based CAD tool with polynomial modeling which links circuit performance metrics to the process parameters. This method is used by circuit designers during the first step of a design phase to simulate in an early stage the impact of process variations on circuit performance.

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The paper is organized as follows. Section 2 describes the process variations device modeling methodology on top of which the DOE flow is built. Section 3 gives a detailed description of the DOE flow itself. In section 4 we describe the circuits on which the method is applied. Section 5 and section 6 review the obtained simulation results on these circuits and their interpretation.

II. PROCESS VARIATIONS MODELING METHODOLOGY

A design of experiment applied to computer-aided design is a mathematical method which allows, in a limited number of electrical simulations to analyze the response of any circuit performances with respect to a certain number of process parameters.
The modeling methodology supports the parameterization of the process variation by applying to any process parameter a deviation with respect to its mean value. This deviation is expressed in term of *number of sigma*, where *sigma* is the standard deviation of the statistical distribution of the parameter.
This capability is applicable to the Global Variations through a specific so-called User-Defined Corner (UDC). It is also applicable to the Local Variations (mismatch effects) through dedicated device instance parameters.
Of course the traditional Pre-Defined Corners (PDC) are still available together with the Statistical models.

The modelling structure (see Figure 1) that has been chosen ensures that

- all types of variation are expressed as a deviation reflecting a shift with respect to the typical value. For the i^{th} parameter P_i let's call D_i the deviation, T_i the typical value, μ_i the mean value and σ_i the standard deviation.
- the Pre-Defined Corners are partially correlated: subsets of device families are correlated together (the main example is the MOSFET families). The deviation D_i is an integer and the Process Parameter value is expressed as

$$P_i = T_i + D_i \times \sigma_i$$

- the Statistical Models are totally correlated (active-passive correlations). The deviation is randomly defined following a statistical distribution, the Process Parameter value is expressed as

$$P_i = \text{distribution}(\mu_i, \sigma_i)$$

- the User-Defined Corners are also totally correlated which means the DOE techniques will lead to an accurate modelling similar to the Statistical Models. The deviation D_i is here a relative floating number as defined by the user or as set by the DOE flow (see next section)

$$P_i = T_i \pm D_i \times \sigma_i$$

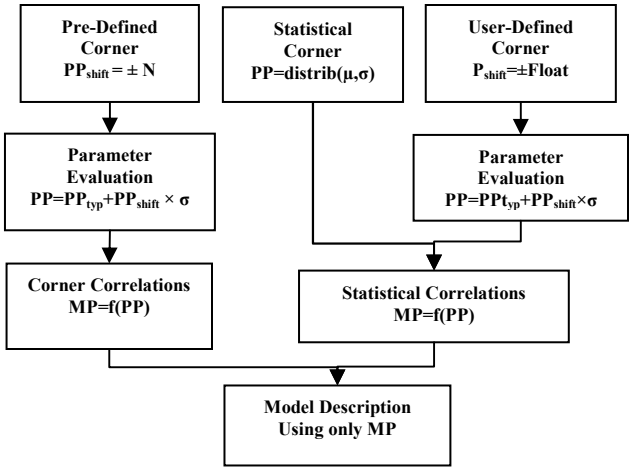

Figure 1. The Modelling Structure

III. DOE FLOW DESCRIPTION

The DOE flow described in this paper integrates several methods which offer the users the best trade-off between speed and accuracy of their analysis. For example, in the full factorial method, 10 process parameters will lead to 2^{10}=1024 simulations whereas more speed-efficient DOE would reduce dramatically the number of simulations by a factor of 100 [3].

The DOE flow proposed here extracts one polynomial model per circuit performance versus the process parameters. The extraction is based on the results of a reduced set of simulations corresponding to a relevant DOE. The polynomial model may be linear or quadratic with or without interactions between process parameters as shown in equation 1:

$$Y=a_0+a_1X_1+\ldots+a_iX_i+\ldots+a_{11}X_1^2+\ldots+a_{ii}X_{ii}^2+\ldots+a_{12}X_1X_2+\ldots+a_{ij}X_iX_j+\ldots \quad (1)$$

where X_i is related to one process parameter and Y represents a circuit performance.

Depending on the number of Process Parameters impacting the circuit and the polynomial order to be extracted, the flow selects the most pertinent type of DOE in term of speed-accuracy trade-off among the Full-Factorial [4], the Plackett-Burman [5], the Doehlert [6]or Latin Hypercube [7].

The DOE analysis flow is summarized in Figure 2:

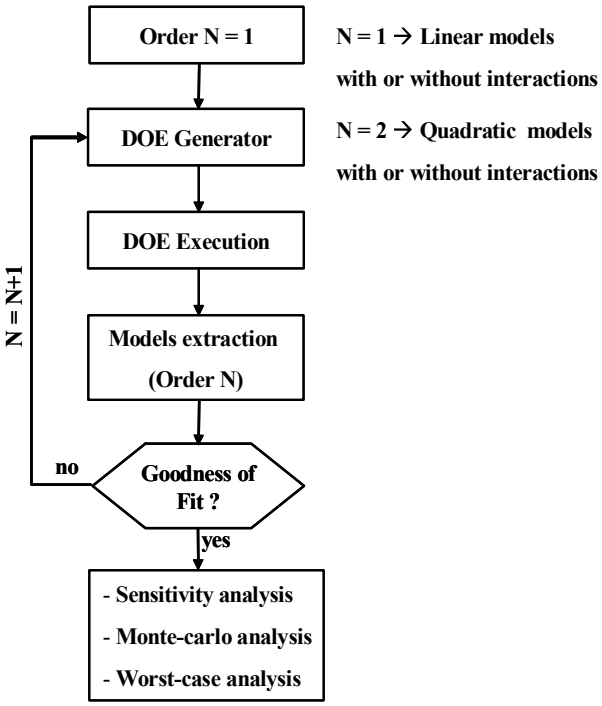

Figure 2. DOE Flow chart

A control loop is built to validate the reliability of the extracted polynomial models. Indicators, provided in the flow, should satisfy a set of criteria to reach an acceptable fit of models. If this last condition is verified, three advanced analysis are then accessible: a sensitivity analysis which evaluates the impact of each process parameter on each circuit performance; a monte-carlo analysis, where the full circuit compact models are replaced by the polynomial models evaluations, which dramatically speeds-up the traditional statistical simulations; a worst-case analysis which extracts the set of process parameters values leading to the maximum and the minimum of circuit performances.

IV. CASES STUDY

The proposed DOE flow has been applied to the design of a 2GHz transconductance low-noise amplifier (LNTA) and an operational amplifier in a voltage follower configuration for baseband applications. A wide variety of analog performance metrics covering gain, noise and linearity were simulated on both circuits. Figure 3 gives an overview of the LNTA which is composed of two stages. First, a transconductor stage amplifies and converts the RF input voltage into current. Then a cascode stage increases the output impedance for better current driving capabilities. The LNTA is designed using mainly MOS transistors, MOM capacitors and P+/poly-silicon resistors. It is used as an RF low-noise amplifier in wireless receivers.

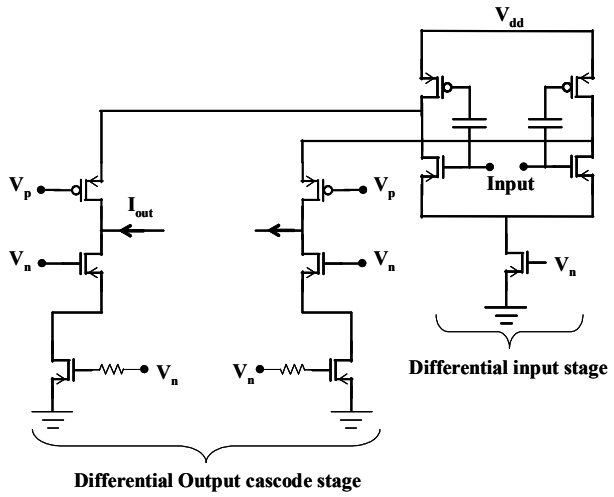

Figure 3. Circuit of the LNTA

The most important RF design specifications on the LNTA are the transconductance gain G_m, the noise figure NF, and the third order input-referred intercept point IIP_3. From an RF design perspective, it is mandatory to estimate the variation of these metrics and to verify that the circuit meets the specifications, even under extreme process variations. For example, a one σ-spread on the value of the IIP_3 leads to a 2σ-spread on the noise generated by the third-order non-linearity. Therefore, the IIP_3 variation cannot be neglected in a design point of view. In addition, the G_m impacts the whole receiver path following the LNTA. Typically, less gain would relax the linearity specification of the following blocks whereas more gain could help by relaxing the noise figures. In other words, in RF and analog, the specifications on an RF low-noise amplifier impact the following stages and therefore, a random process variation should be considered accurately during the design phase. In this context of severe constraints, the DOE flow proposed in this work is the best suited CAD tool to simulate the performances of this RF block under random process variations. Figure 4 shows the simulation bench used in the DOE analysis of the LNTA. This bench should be chosen carefully in order to preserve the same input and load conditions.

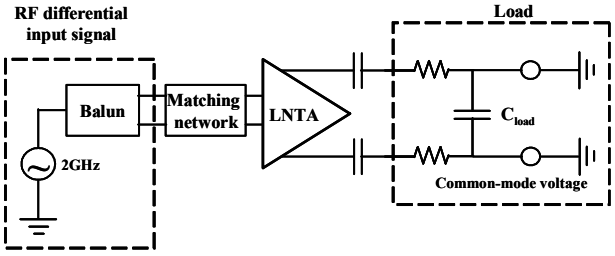

Figure 4. LNTA simulation bench

Figure 5 gives an overview of the operational amplifier design used in the voltage follower testcase. The first stage is a folded-cascode implementation with PMOS differential transistors. The second stage comprises a voltage gain made of a common-source amplifier and a common-drain voltage buffer. The output of the common-drain stage is feedback at the input to achieve an overall unity gain. An RC network is connected at the output stage to compensate the pole created by the common-source stage. The design of this baseband voltage follower involves mainly MOS transistors, MOM capacitors and P+/poly-silicon resistors.

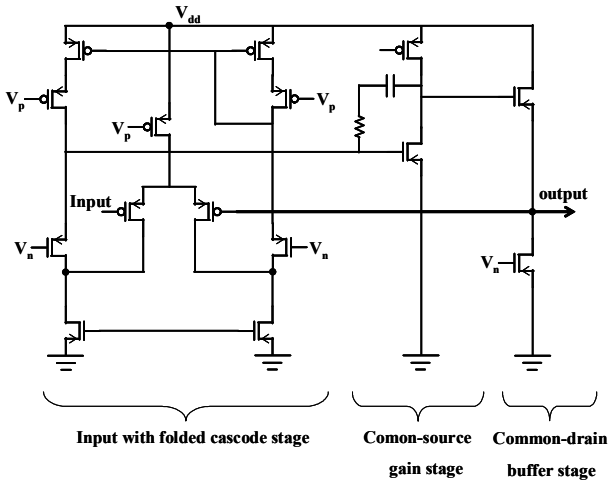

Figure 5. Circuit of the voltage follower

At baseband low-frequency applications, the analog specifications are certainly less stringent than those of the RF parts. However, in the frame of the intended application, this analog voltage follower should satisfy severe specifications among which noise and non-linearity are to be considered with precaution. Figure 6 shows the simulation bench used in the DOE analysis of the voltage follower. This bench is chosen carefully to preserve the same input signal and load conditions.

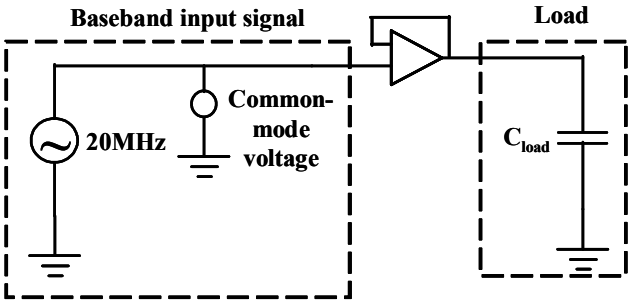

Figure 6. Voltage follower simulation bench

V. SIMULATION RESULTS

The LNTA simulation bench of figure 4 is used to extract the following RF performances: G_m, NF and IIP_3. The DOE analysis applied to this bench has lead to three distinct polynomial equations (table 1). At this stage, it is important for the circuit designer to realize the flexibility of the DOE flow which offers several types of models in order to choose the best model for each extraction of a performance metric. For example, the NF is most likely modeled with first-order polynomial equation, whereas for the G_m and IIP_3, it is very difficult to achieve reliable results without using interactions and/or quadratic effects. Therefore, the user can choose the type of model which better matches his targeted performance extraction. We have applied the linear Plackett-Burman method with no interactions in an AC simulation to determine the noise figure of the LNTA.

TABLE I. DOE RESULTS FOR THE LNTA

	DOE polynomial model
NF dB	1.71 - 0.0254nsvt - 0.0236dtox – 0.012psvt - 0.007poly_cd - 0.006drsh + 0.003active_cd
IIP_3 dB_m	-10.88 - 0.1psvt - 0.04dtox + 0.04nsvt - 0.03poly_cd - 0.022drsh - 0.015dtox*nsvt – psvt*nsvt
G_m mS	79.6 + 1.63nsvt + 1.36dtox + 1.18poly_cd – 0.15dtox*nsvt + 0.14poly_cd*nsvt + 0.12poly_cd*dtox + 0.1psvt^2 – 0.07nsvt^2 – 0.06dtox^2

For the gain extraction (AC simulation), a quadratic Plackett-Burman method including interactions between process parameters was necessary to achieve the reliable results shown in table 1. For the IIP3, a more accurate simulation bench was needed, involving a transient analysis followed by a Fast Fourier Transform (FFT).

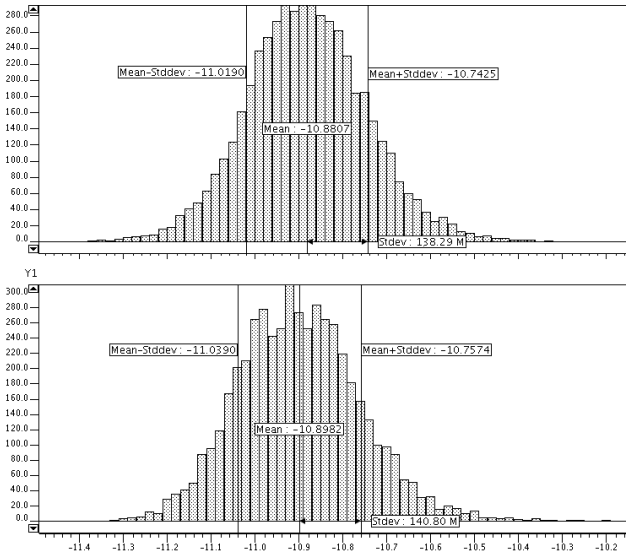

Figure 7. DOE and electrical model comparison

A first-order polynomial equation including interactions between process parameters was used to model the input-referred third order intercept point as shown in Table 1. To validate the accuracy of the extracted IIP_3 model, a comparison between the DOE model and the actual electrical model was performed using Monte-Carlo analysis. Figure 7 shows the good matching we obtained with almost the same σ-spread of both histograms.

VI. RESULTS ANALYSIS

In all three analyses on the LNTA design, the reliability criteria indicated by the flow were satisfied. We applied the sensitivity analysis on the polynomial models obtained for each performance to better evaluate the weight of the involved process parameters. Following DOE analysis, it is important for a circuit designer to draw conclusions that will give him reliable information on his design under random process variations. Because the LNTA is mainly biased by NMOS devices at the input and the output stages, we note from table 1 that the nsvt process parameter is the most influent on the gain G_m. In the same way, regarding the noise figure, one can see from polynomial equation of table 1 that the process parameters affecting the gain are also affecting the noise figure. When looking at the monte-carlo analysis performed on the corresponding polynomial model, one can see a very low σ-spread of the NF (Figure 8). This result proves the robustness of the noise figure performance with respect to process variations.

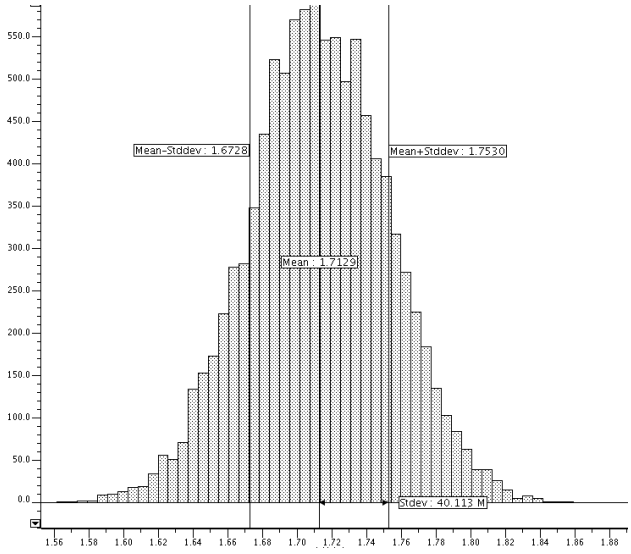

Figure 8. DOE NF model Monte-carlo analysis

Equations in Table 1 show that the PMOS devices of the cascode output stage have an important weight in the IPP3 model. Indeed, the non-linearity in RF design is mainly related to the circuit load characteristics and to the dynamic range of the output signal.

The same advanced analysis offered by the flow were applied to the results of the baseband operational amplifier. Here, the overall noise of this block, comprised of the thermal (high-frequency) and the 1/f (low-frequency) components, is of particular interest to the circuit designer. Therefore, the designer can apply the DOE flow to analyze independently both noise components by specifying two different noise metrics: N_{TH} and noise corner frequency F_{corner}. From Table 2, one can see that for N_{TH} (respectively F_{corner}), the psvt (respectively dtox) has the biggest weight among all other parameters. At this point, several conclusions could be drawn. First, the output stage formed by NMOS transistors is not a major contributor to the overall noise. From this angle, the DOE flow is capable of identifying the optimization zone in a design. To reduce efficiently the overall noise performance, a better understanding of what impacts both components is necessary.

TABLE II. DOE RESULTS OF THE VOLTAGE FOLLOWER

	DOE polynomial model
N_{TH} nV	$5.5 - 10^{-3}(80.9psvt + 80.8dtox - 24.0nlvt + 11.2nsvt + 10.2drsh + 5.32\ poly\_cd)$
F_{corner} kHz	$1095 - 18.43dtox - 12.22psvt - 7.1nlvt - 6.3poly\_cd - 4.94nsvt - 2.85drsh + 1.43active\_cd - 0.4cdpolyn$
IIP_3 dBV	$8.7 + 10^{-3}(457.3dtox + 299.4psvt + 181.1nlvt - 166.7nsvt - 74.5plvt + 26.7active\_cd + 24.2poly\_cd*plvt + 23.6dtox*plvt - 22.5dtox*nlvt + 21.9nsvt*nlvt - 21poly\_cd + 15.6psvt*plvt)$

In summary, whether N_{TH}, F_{corner} or the overall noise performance need to be optimized, the designer will angle his work differently taking advantage of the DOE flow. Secondly, by tracking the process parameter which mostly impacts the desired performance, the designers can better predict its evolution from one technology node to another. As a concrete example, the oxide thickness is certainly getting thinner from one technology to the other, resulting in a more important spread during processing and fabrication. By analyzing the weight of the oxide thickness in the models given by the DOE flow analysis, the circuit designer will certainly predict qualitatively the evolution of his block in the case of a direct design porting.

VII. CONCLUSIONS

The circuits presented here are completely characterized under process variation by simple polynomial equations thanks to the proposed DOE flow. Compared to traditional analysis such as monte-carlo, it offers a good trade-off between speed and accuracy by reducing dramatically the number of simulations. Advanced analysis are also offered to help circuit designers to see what will make their design deviate from the nominal value and also to better angle their optimization work in the good direction.

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