Analog Circuit Reliability in Sub-32 Nanometer CMOS: Analysis and Mitigation

Georges Gielen, Elie Maricau and Pieter De Wit
ESAT-MICAS, K.U.Leuven, Belgium

***Abstract*—The paper discusses reliability threats and opportunities for analog circuit design in high-k sub-32 nanometer technologies. Compared to older SiO_2 or SiON based technologies, transistor reliability is found to be worse in high-k nodes due to larger oxide electric fields, the severely aggravated PBTI effect and increased time-dependent variability. Conventional reliability margins, based on accelerated stress measurements on individual transistors, are no longer sufficient nor adequate for analog circuit design. As a means to find more accurate, circuit-dependent reliability margins, advanced degradation effect models are reviewed and an efficient method for stochastic circuit reliability simulation is discussed. Also, an example 6-bit 32nm current-steering digital-to-analog convertor is studied. Experiments demonstrate how the proposed simulation tool, combined with novel design techniques, can provide an up to 89% better area-power product of the analog part of the circuit under study, while still guaranteeing a 99.7% yield over a lifetime of 5 years.**

***Index Terms*—NBTI, PBTI, Hot Carriers, TDDB, SBD, HBD, Failure-Resilience, Aging, Design for Reliability, High-k CMOS.**

I. Introduction

Today, people in the semiconductor device community are looking at transistor reliability as one of the major technology concerns for current and future CMOS nodes at 32nm and below [1]. Failure mechanisms such as Hot Carrier Injection (HCI) [2]–[4], Negative and Positive Bias Temperature Instability (N/PBTI) [4]–[7] and Temperature Dependent Dielectric Breakdown (TDDB) [4], [8]–[10] can have a big impact on the lifetime of an individual transistor and can therefore also threat the lifetime of an entire circuit. The design community, on the other hand, does not seem to consider reliability their responsibility. This clear gap between the device and the design community raises the question: is transistor reliability really a problem? An answer to this question can be found when looking into the history of transistor reliability assessment [11]. In the seventies and the eighties device scientists were the first to discover transistor failure mechanisms such as HCI, NBTI and TDDB. At that time, research effort was mainly focused towards understanding these phenomena, rather than trying to solve actual circuit reliability problems. In the nineties, the attention started to shift towards the impact of failure mechanisms on circuit behavior. Measurements on individual transistors at high temperatures and elevated voltage stresses were used to determine circuit design margins. For example, the maximum circuit operating voltage was chosen such that the maximum V_{TH} shift of a transistor was 50mV after 5 years of operation. At this point, the design community did not have to worry too much about reliability since it was taken care of by the technologists at the device level and only limited effort was done to analyze the impact of transistor aging at circuit level [12]. After the turn of the century, device scientists started to introduce new materials to further scale CMOS technologies. Unfortunately, these new materials introduced additional failure mechanisms and made existing aging effects more severe. Especially for sub-1nm EOT (Effective Oxide Thickness) devices, classic reliability assessment techniques now result in very narrow reliability margins [11]. As a result, the design community now also has to look at transistor reliability and an advanced design for reliability workflow is needed in order to gain sufficient design margins. This paper demonstrates how accurate transistor aging models, combined with efficient circuit reliability simulation tools and novel design techniques, can result in better performing and guaranteed reliable products.

The paper is organized as follows. Section II discusses transistor reliability in high-k CMOS technologies. It is shown how increasing oxide electric fields significantly reduce overall transistor behavior, how the introduction of new materials aggravates existing reliability effects and how decreasing device dimensions results in time-dependent transistor mismatch. Section III overviews models for the most important failure mechanisms in high-k CMOS nodes and discusses a technique to analyze the impact of stochastic transistor aging at circuit level. Section IV then studies the design of a failure-resilient current-steering digital-to-analog convertor in a 32nm high-k technology. It is shown that advanced transistor models and adequate tools can increase circuit design margins. For the circuit under study, a 89% reduction of the power-area product of the analog part of the circuit is achieved while still guaranteeing product reliability over 5 years of operation. Finally, conclusions are presented in section V.

II. Transistor Reliability in High-k CMOS

The exponential increase in the gate leakage current, when scaling the gate oxide thickness of CMOS transistors, forced device engineers to introduce gate materials with a higher dielectric constant compared to traditional SiO_2 or SiON gate dielectrics. This allows further increase of the gate oxide capacitance while keeping the physical gate thickness sufficiently large [13]. Unfortunately, the introduction of high-k materials,

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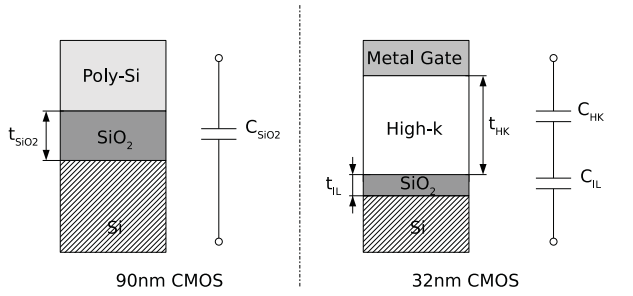

Fig. 1. Schematical representation of a traditional 90nm CMOS SiO_2-based stack (on the left) and a 32nm CMOS high-k metal-gate HfO-based stack (on the right).

combined with the further reduction of the lateral transistor dimensions, reduces circuit reliability.

A. Reduction of the Effective Oxide Thickness

In the search for suitable high-k dielectrics, most research currently focusses on HfO-based or TiN-based materials. Unfortunately none of these dielectrics is compatible with Si. This incompatibility is solved by maintaining a very thin SiO_2 or SiON interfacial layer (IL) between the silicon substrate and the high-k material. Fig. 1 depicts a schematical representation of a traditional 90nm CMOS stack and a modern 32nm high-k metal-gate (HKMG) stack. For a transistor in inversion, the electric field $E_{\mathrm{SiO_2}}$ over the SiO_2 layer in each stack can be written as:

$$E_{\mathrm{SiO_2}} = \frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{\mathrm{EOT}} \tag{1}$$

with V_{TH} the threshold voltage and EOT the effective oxide thickness:

$$\mathrm{EOT}_{\mathrm{90nm}} = t_{\mathrm{SiO_2}} \tag{2}$$

$$\mathrm{EOT}_{\mathrm{32nm}} = t_{\mathrm{IL}} + \frac{\varepsilon_{\mathrm{SiO_2}}}{\varepsilon_{\mathrm{HK}}} t_{\mathrm{HK}} \tag{3}$$

with $t_{\mathrm{SiO_2}}$ the thickness of the SiO_2-oxide in a 90nm technology (typically $t_{\mathrm{SiO_2}} = 2.0 - 2.4$nm), t_{IL} the thickness of the SiO_2 interfacial layer in the 32nm technology (typically $t_{\mathrm{IL}} = 0.5 - 1$nm) and t_{HK} the thickness of the high-k layer in the 32nm technology (typically $t_{\mathrm{HK}} = 2 - 4$nm). $\varepsilon_{\mathrm{SiO_2}}$ and $\varepsilon_{\mathrm{HK}}$ are the dielectric constants for SiO_2 ($\varepsilon_{\mathrm{SiO_2}} \approx 3.9$) and the high-K-dielectric respectively ($\varepsilon_{\mathrm{HK}} \approx 30$). As a result, $\mathrm{EOT}_{\mathrm{32nm}}$ is typically smaller than $\mathrm{EOT}_{\mathrm{90nm}}$, resulting in a larger electric field over the SiO_2-interfacial layer of a HKMG technology compared to the electric field over the SiO_2-oxide in a traditional CMOS technology (i.e. $E_{\mathrm{SiO_2,32nm}} > E_{\mathrm{SiO_2,90nm}}$). Since most transistor degradation effects depend exponentially on this electric field, the introduction of high-k materials further reduces the maximum operating voltage to guarantee reliable circuit operation [13].

B. Introduction of New Materials

Negative Bias Temperature Instability (NBTI), Temperature Dependent Breakdown (TDDB) and Hot Carrier Injection (HCI) were, in older SiO_2 or SiON based technologies (i.e. $\geq$65nm), considered as the most important aging effects [14]. Both the NBTI and HCI effect generates traps at the substrate/dielectric interface. These traps affect transistor parameters such as the threshold voltage V_{TH} [2], [5]. With the introduction of high-k materials, a thin SiO_2 or SiON interfacial layer has been maintained (see Fig. 1). Consequently, the substrate/dielectric interface does not change and NBTI and HCI remain a problem in HKMG technologies [13]. Further, research indicated the interfacial layer to be the major factor controlling breakdown in HKMG technologies [9]. Therefore, models and principles previously developed to characterise breakdown in older technologies still apply in high-k technologies. Finally, the PBTI effect, which is negligible in SiO_2 or SiON based technologies, is found to become a lot worse in high-k technologies [6]. Existing transistor failure mechanisms thus remain and even become worse with the introduction of high-k dielectrics in advanced nanometer CMOS nodes.

C. Atomic Scale Transistor Dimensions

BTI and HCI effects in large micrometer-sized transistors are typically considered deterministic [2], [5]. The application of a given stress on matched transistors therefore results in an identical shift of the transistor parameters. Scaling transistors down to nanometer dimensions, however, gradually changed these deterministic effects into stochastically distributed failure mechanisms [7]. At device level this results in a time-dependent shift of the transistor parameters (i.e. $\Delta V_{\mathrm{TH}} = \mathrm{f}(t)$) augmented with a time-dependent increase of the standard deviation on these parameters (i.e. $\sigma(V_{\mathrm{TH}}) = \mathrm{g}(t)$). Initially matched transistors, processed in ultra-scaled nanometer CMOS technologies, can therefore cause circuit failure resulting from increased time-dependent transistor mismatch.

III. Circuit Simulation and Analysis

Section II has discussed the reliability of transistors processed in a high-k metal-gate technology. This knowledge is now applied at circuit level. Degradation effect models, suitable for circuit simulation, are reviewed and an efficient simulation method for stochastic circuit reliability analysis is discussed.

A. Degradation Effect Modeling

Temperature Dependent Breakdown (TDDB), Hot Carrier Injection (HCI) and Bias Temperature Instability (BTI) are considered to be the most important aging effects in high-k CMOS technologies [8], [13]. Models for each of these effects are now reviewed.

TDDB is an extremely local phenomenon, for which an extra current flows through a small region of the gate oxide. During a breakdown degradation process, different BD modes can be distinguished. Hard-BD (HBD) is the most harmful mode and provokes a complete loss of the oxide dielectric properties with gate currents in the mA range. However, HBD is in nanometer CMOS technologies only a significant reliability threat at elevated operating voltages (i.e. $\mathrm{V_{str,HBD}@5year} \approx 1.2 - 1.4$V for EOT$=$ 0.9nm) [8], [10], [13]. For devices with an oxide thickness smaller than 5nm (CMOS nodes $<$ 180nm), HBD

can be preceeded by Soft-BD (SBD). SBD can be observed as a partial loss of the dielectric properties, resulting in an increase of the magnitude and the noise of the gate current. The probability to have n SBD defects at time χ can be described with a Poisson distribution [15], [16]:

$$P_n(t) = \frac{\chi^n}{n!}\exp(-\chi) \quad \text{with} \quad \chi = \left(\frac{t}{t_{\text{SBD}}}\right)^{\beta}$$
$$t_{\text{SBD}} = t_{63}\left(\frac{WL}{A_{\text{ref}}}\right)^{1/\beta}\left(\frac{E_{\text{ox}}}{E_{\text{ref}}}\right)^{\gamma}$$

where t_{63} is the time to breakdown at the 63rd percentile for a reference transistor with area A_{ref} stressed at E_{ref}. β and γ are process-dependent parameters.

HCI first became a problem in the eighties due to the continuous scaling of transistor dimensions without accompanying supply voltage reduction [17], [18]. Recent measurements on high-k CMOS transistors, however, revealed how high-k stacks are more resilient to HC stress than SiO_2 stacks [3]. Therefore, HCI appears to be much less a problem in high-k nodes, compared to TDDB and BTI effects. During HC stress, which consists of a large electric field near the drain end of a transistor in saturation, hot carriers are produced. The latter introduce both interface and oxide traps (near the drain) and a substrate current [17]. An increase in the number of interface and oxide traps changes transistor characteristics such as the threshold voltage V_{TH}, the carrier mobility β and the output conductance g_o [2]. As holes are much 'cooler' (i.e. heavier) than electrons, hot carrier effects in nMOS devices are more significant than in pMOS devices [17]. HC degradation is typically modeled with a power law dependence on the stress time t [17], [19]. The trapping probability of the carriers increases exponentially with increasing oxide electric field E_{ox}. Besides E_{ox} and the maximum lateral electric field E_m, HC dependence on temperature T and transistor length L is also reported [2], [17]:

$$\Delta V_{\text{TH}} \sim C_{\text{HC}}\frac{1}{\sqrt{L}}\exp(\alpha_1 E_{\text{ox}})\exp(\alpha_2 V_{\text{DS}})t^{n_{\text{HC}}} \qquad (4)$$

with ΔV_{TH} the transistor threshold voltage shift. n_{HC} is the time exponent and is typically around 0.5. C_{HC}, α_1 and α_2 are technology-dependent parameters and V_{DS} is the drain-source voltage.

BTI recently gained a lot of attention due to its increasingly adverse impact on circuits processed in nanometer CMOS technologies [20]. In older technologies (>65nm CMOS), BTI mainly affects pMOS transistors (i.e. Negative BTI or NBTI) [21]. In high-k CMOS technologies, however, a similar wear-out behavior has been observed in nMOS devices (i.e. Positive BTI or PBTI) [6]. BTI degradation is typically represented as following a power law of stress time and is accelerated by the electric field in the MOS's gate dielectric E_{ox} and by the temperature T [21]:

$$\Delta V_{\text{TH}} \sim \exp(\alpha_3 E_{\text{ox}})\exp(\frac{-E_{\text{a}}}{kT})t^{n_{\text{BTI}}} \qquad (5)$$

with ΔV_{TH} the transistor threshold voltage shift and α_3 and E_{a} process-dependent constants, n_{BTI} is the time exponent (typically around 0.16) and k is the Boltzmann constant. Formula (5), however, only models the result of a DC voltage stress, while AC stress reveals a peculiar additional property of the BTI mechanism: the so-called relaxation or recovery of the degradation immediately after the stress voltage has been reduced [22]. This phenomenon greatly complicates the evaluation of BTI, its modeling, and the extrapolation of its impact on circuitry. In [5] the authors have proposed a complete and analytical NBTI model, suited for circuit simulation. Additionally, in very small nanometer-size transistors, BTI has been observed as a stochastic phenomenon with a ΔV_{TH} distribution due to individual charging and discharging events. The CDF F_N of the ΔV_{TH} distribution can be described analytically by [7]:

$$F_N(\Delta V_{\text{TH}}, \eta) = \sum_{n=1}^{\infty}\frac{e^{-N}N^n}{n!}\left(1 - \frac{\Gamma(n, \Delta V_{\text{TH}}/\eta)}{(n-1)!}\right) \qquad (6)$$

with N the mean number of defects in the gate oxide. $N = \langle\Delta V_{\text{TH}}\rangle/\eta$ and $\langle\Delta V_{\text{TH}}\rangle$ represents the average overall threshold voltage shift calculated from formula (5) or using the model proposed in [5]. η is inversely proportional to the transistor area and is the average V_{TH} shift caused by a single carrier discharge (e.g. $\eta \approx 4.75$mV for a 0.8nm EOT pMOS with W= 90nm and L= 35nm [7]). Finally, n is the number of defects and $\Gamma(a, x)$ represents the upper incomplete gamma function.

B. Efficient Reliability Circuit Simulation

To quantify the impact of transistor aging effects at circuit level, a circuit reliability simulator is required. Such a simulator can be used at design time, to help a designer evaluating the reliability of his or her circuit and to pinpoint circuit reliability weak spots.

In this work an advanced stochastic reliability simulator, capable of analyzing the effect of HC degradation, NBTI, PBTI and SBD on the behavior of a circuit, is used [16]. In addition to transistor wear-out effects, the simulator also calculates the impact of parametric process variability on the circuit degradation. To quantify the impact of statistical effects, such as process variability and stochastic aging effects, on the behavior of a circuit, the simulator uses Design of Experiments (DoEs). These information gathering techniques allow to extract a maximum amount of information with a minimum set of experiments (or simulations) and thus limit simulation time [23]. Each DoE consists of a well-chosen set of circuit samples that are all evaluated with a core reliability simulator. The latter is SPICE-based and uses an automatic step-size control to optimize simulation speed and accuracy. Based on the results of the DoE-analysis, a circuit Response Surface Model (RSM) is derived. The RSM can then be used for further circuit reliability analysis such as circuit weak spot detection and yield calculation as a function of circuit lifetime. More details on the implementation of the simulator can be found in [16] and [24].

Fig. 2 illustrates the operation of the reliability simulator on a example LC-VCO circuit. Fig. 2(b) depicts the results of

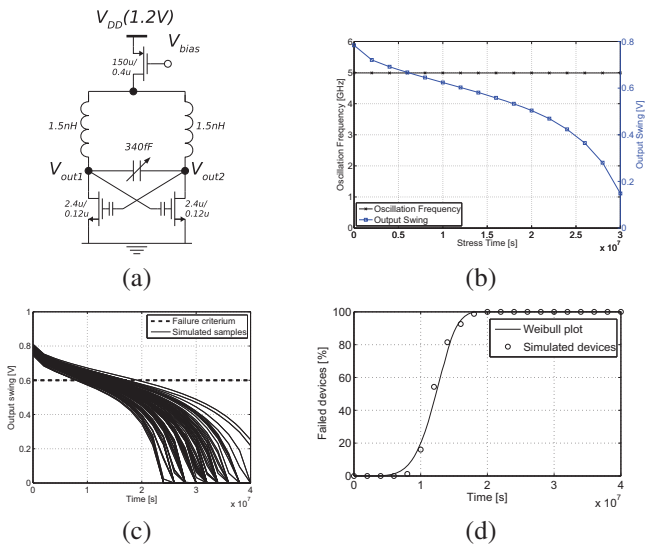

Fig. 2. Reliability simulation of an LC-VCO. LC-VCO (a). Nominal reliability simulation monitoring the oscillation frequency and the output swing (b). Dispersion of the output swing for 300 samples (c). CDF of the failure-time with a failure criterion set to an output swing less than 0.6V (d).

a nominal reliability simulation (i.e. not including the effect of process varations). The oscillation frequency is mainly a function of the inductor and capacitor value of the LC-tank and does therefore not vary over time. The output swing, on the other hand, reduces due to hot carrier degradation in the cross-coupled transistor pair. A variability-aware simulation on 300 samples (i.e. using the DoE-based simulation method, described above) indicates how some samples age very fast, while others are much more resilient to degradation (see Fig. 2(c)). When integrated in a real application - implying strict circuit specifications - this therefore results in a dispersion of the failure time (i.e. not all circuits fail at the same time). For this example, 20% of the samples already fail after 4 months, while another 20% functions correctly during a stress time of 6 months and more (see Fig. 2(d)). The example above illustrates how accurate wear-out effect models, combined with an efficient reliability simulator, can provide a lot of information about the aging behavior of the circuit. This information can help a designer to make his or her circuit more reliable or to increase design margins (also see section IV).

IV. Design Study: A Failure-Resilient IDAC

To illustrate the potential of the models and simulation techniques presented in section III, the design of a failure-resilient current-steering digital-to-analog convertor, implemented in a high-k 32nm CMOS technology, is studied.

A. Technology Details

A predictive 32nm high-k CMOS technology with 1.1nm EOT and a $V_{\text{TH}} = 0.38\text{V}$ is used. Simulation models for each failure mechanism (see section III-A) are calibrated with measurements from literature [6], [7], [16] and an $A_{\text{VTH}} = 2.5\text{mV}\mu\text{m}$ is used to estimate the effect of mismatch variations [4]. The nominal reliable supply voltage $V_{\text{DD,nom}}$

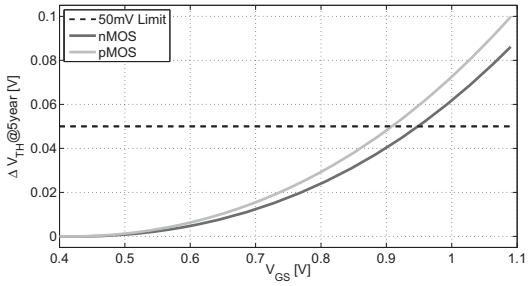

Fig. 3. Simulation of the threshold voltage shift after 5 years as a function of stress voltage for an nMOS and pMOS transistor in a predictive 32nm CMOS technology with $V_{\text{TH}} = 0.38V$. For a reliability margin of $\Delta V_{\text{TH}} \leq 50\text{mV@5year}$ the maximum supply voltage is only 0.91V and is limited by NBTI.

is calculated, based on accelerated stress measurements on individual devices. $V_{\text{DD,nom}}$ is defined as the stress voltage for which the threshold voltage shift does not exceed a reliability margin of 50mV after 5 years. Only PBTI, NBTI and SBD aging mechanisms are included in the simulations, since these are considered to be the major failure mechanisms in high-k technologies (see section II). Extrapolation from accelerated stress measurements results in a $V_{\text{DD,nom}}$ of only 0.91V (see Fig. 3). With $V_{\text{TH}} = 0.38\text{V}$, this is very little headroom to work with, especially when designing an analog circuit where stacked transistors are typically used to achieve a sufficiently large small-signal output resistance. Nevertheless, this is how reliability margins are typically determined in older technologies [11]. Additionally, this technique (i.e. reliability assessment based on accelerated stress tests on individual transistors) does not guarantee a reliable circuit:

- The reliability margin is chosen arbitrarily - in this example $\Delta V_{\text{TH}} \leq 50\text{mV}$ - and the sensitivity of the circuit to individual transistor V_{TH} variations is not considered.
- Aging-induced threshold voltage variations due to atomic-scale transistor effects are not considered (see section II).

More optimal designs using higher supply voltages can be realized if the actual impact of degradation mechanisms on a circuit is evaluated. In the next sections, this technique is evaluated for an example analog circuit: a current-steering digital-to-analog converter (IDAC). The DAC is designed and compared according to the following three design strategies: (1) conventional design, (2) degradation-aware design at higher supply voltage to increase analog performance, and (3) degradation-aware design using circuit techniques relaxing the analog circuit requirements.

B. Conventional Circuit Design

The example 6-bit current-steering digital-to-analog converter (IDAC) is depicted in Fig. 4. Because of the unary implementation, this IDAC mainly consists of 63 matched unary current-source transistors M_{cs}. Using the switch transistors M_{sw}, the individual currents are routed to one of the output nodes $V_{\text{out}+}, V_{\text{out}-}$, both connected to a fixed load resistor R_{load}. In case of sufficient voltage headroom, cascode transistors M_{cas} are added to increase the output impedance. A

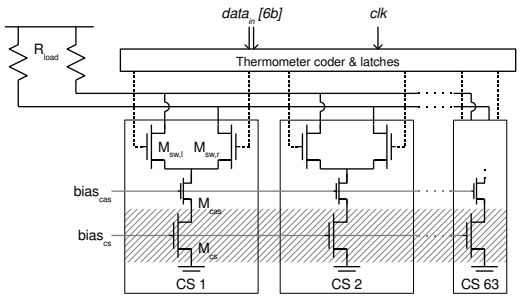

Fig. 4. Schematic of a 6-bit current-steering digital-to-analog converter. Reliability simulation is performed on the current-source transistors M_{cs}, shaded in gray, which are the accuracy-limiting transistors of the circuit.

digital thermometer decoder and clocked latches generate the switch transistor driving signals, based on the IDAC digital input word $data_{\text{in}}$.

From a static performance point of view, the yield of this circuit is limited by the Integral Non Linearity (INL). The INL, defined as the largest difference between the ideal and the actual output value of the DAC, should be limited to 0.5LSB and is caused by mismatch on the current-source transistors M_{cs}. Monte-Carlo simulations [25] are used to determine the maximum allowable current deviation $\sigma(\Delta I_{\text{LSB}})/I_{\text{LSB}}$, for a certain DAC configuration. Using the Pelgrom mismatch equations [26] and the IDAC specifications, the sizes of the current-source transistors can be calculated:

$$\frac{W}{L} = \frac{I_{\text{LSB}}}{\beta\left(V_{\text{GS}}-V_{\text{TH}}\right)^2} \tag{7}$$

$$WL_{\text{min}} \approx \frac{A_{\text{VTH}}^2}{\left[\frac{\sigma(\Delta I_{\text{LSB}})}{I_{\text{LSB}}}\frac{(V_{\text{GS}}-V_{\text{TH}})}{2}\right]^2} \tag{8}$$

According to (8), minimal chip area and associated chip cost, requires a maximal V_{GS} voltage. On the other hand, preserving the transistor operation in the saturation region limits the usable V_{GS} range: $V_{\text{GS}} \leq V_{\text{DS}} + V_{\text{TH}} \leq V_{\text{DD}} - V_{\text{out,sw,diff}} - V_{\text{DS,cas}} - V_{\text{DS,sw}} - V_{\text{TH}}$. A design value of $V_{\text{GS}} = 0.6V_{\text{DD}}$ yields a good compromise.

In case of high-resolution DACs the area of the unary current source (8), and the corresponding current-source matrix area, will dominate the area of the analog part of the digital-to-analog converter. As such, this area will be used in the area-power product later on. The digital part of the DAC (i.e. the thermometer coder and the latches) is more robust to compoment variations and aging effects, compared to the analog part, and is therefore not studied here. The latter part takes about half of the total chip area.

Reliability simulations on conventional current-source transistors, designed for a yield (defined as INL $\leq$ 0.5 LSB and DR$\geq$ $0.2V_{\text{DD}}$) of 99.7% (3σ design), result in a yield reduction to 99.08% (2.6σ) after 5 years, even though the supply voltage does not exceed the 'safe' $0.91V$ limit (section IV-A). Reliability assessment based on accelerated stress tests on individual transistors is therefore not a sufficient, nor an appropriate technique for circuit design in advanced high-k technologies.

C. Elevated V_{DD} to Improve Circuit Performance

To improve circuit performance in the second design, the supply voltage is increased above the 0.91V limit (see section IV-A). Although higher V_{dd} and associated increased degradation effects, circuit reliability is guaranteed through circuit simulation with the circuit reliability simulation method reviewed in section III.

Because of the statistical nature of the degradation effects (see section III-A), the spread on the individual current sources will increase. Therefore formula (8), which determines the minimum area of the LSB current source, is extended to:

$$WL_{\text{min,deg}} \approx \frac{A_{\text{VTH}}^2}{\left[\frac{\sigma(\Delta I_{\text{LSB}})}{I_{\text{LSB}}}\frac{(V_{\text{GS}}-V_{\text{TH}}-\Delta V_{\text{TH}})}{2} - \sigma_{\text{BTI}}(V_{\text{TH}})\right]^2} \tag{9}$$

with ΔV_{TH} and $\sigma_{\text{BTI}}(V_{\text{TH}}) \sim \frac{1}{WL}$ the BTI-induced absolute threshold voltage shift and the BTI-induced standard deviation on the threshold voltage respectively. ΔV_{TH} and $\sigma_{\text{BTI}}(V_{\text{TH}})$ increase with time (see section III-A). The effects of increased V_{dd} are clearly shown in (9):

- If V_{DD} is increased, σ_{BTI} and ΔV_{TH} will increase, requiring a *larger* unit transistor area: $WL_{\text{min,deg}} > WL_{\text{min}}$ since the latter only takes initial process variations into account (see formula (8)).
- If V_{DD} is increased, V_{GS} becomes larger, resulting in *smaller* area realizing the same current accuracy. Furthermore, WL_{min} becomes less sensitive to $\sigma_{\text{BTI}}(V_{TH})$ and ΔV_{TH} variations.

Fig. 5 depicts the required area-power product for a supply voltage ranging from 0.8V to 1.8V with a yield target of 99.7% and a circuit lifetime of 5 years (i.e. the black solid line). The square marker in Fig. 5 represents the conventional design from the previous subsection IV-B, meeting yield specifications at design time but not after 5 years of operation. The circuit designs, operating at low supply voltages, are performance limited by process variations. At higher supply voltages, the circuit performance is limited by PBTI aging effects. Supply voltages higher than 1.4V strongly increase the probability for hard breakdown events in the transistors (see section III-A), therefore a 0.2V backoff is introduced. Eventually, this results in an optimum $V_{\text{DD}} = 1.2$V, where the area-power product of the analog part of the IDAC is improved by 53% when compared to the design at the nominal supply voltage, while a 99.7% yield is still guaranteed over a lifetime of 5 years. As can be seen, other performance metrics might yield different optimum supply voltages. System level designers should thus determine the most appropriate performance characteristic.

D. Design Techniques to Relax Analog Circuit Requirements

The availability of area-efficient, low-power digital circuits in CMOS, allows the implementation of digitally-assisted analog systems. In this way, the effect of performance-limiting analog imperfections can be reduced greatly, leading to designs with a significantly reduced area-power product. In the third IDAC design, digital calibration is used to eliminate different

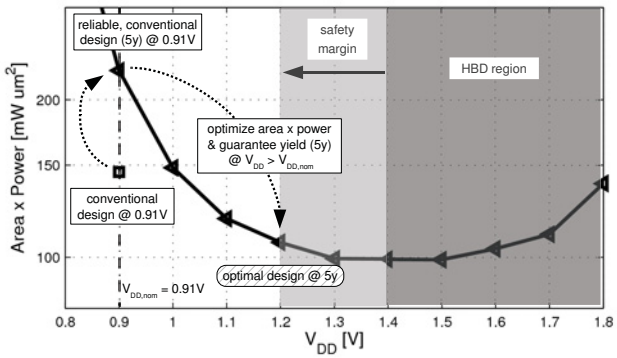

Fig. 5. Area-power product of the analog part of a 6-bit DAC versus supply voltage. Each design guarantees a 99.7% yield after 5 years. An optimum supply voltage can be found, making optimal use of the technology ($V_{\mathrm{DD}} > V_{\mathrm{DD,nom}}$) and taking the expected degradation into account.

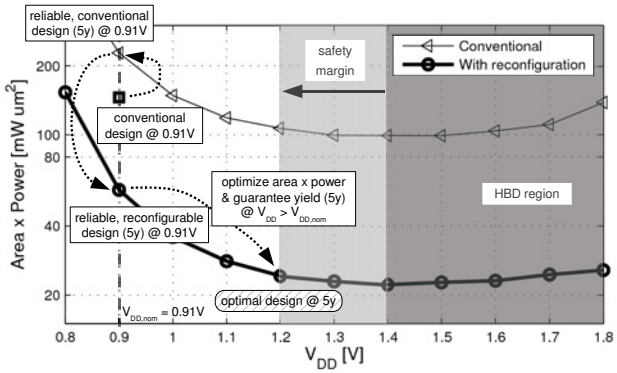

Fig. 6. Area-power product of the analog part of a standard and reconfigurable 6-bit DAC versus supply voltage. Optimal supply voltages can be found for both implementations. The reconfigurable design outperforms the conventional design both at the nominal supply voltage as well as at the optimized supply voltage.

error sources: gradient errors (spatial reliability), gain and offset errors (deterministic reliability), random mismatch induced errors (stochastic reliability). In this section, the example IDAC will be optimized using the Switching Sequence Post Ajustment (SSPA) technique [25]. This algorithm optimizes the order in which the individual current sources are addressed, thereby reducing the INL. In Fig. 6, the SSPA algorithm is combined with the supply voltage increase technique discussed in the previous section. Application of the SSPA technique strongly improves the performance of the DAC. At the nominal supply voltage ($0.91V$), the area-power product decreases by 74% using the SSPA technique. When also optimizing the operating voltage, based on information from reliability simulations, this results in a supply voltage of $1.2V$ and an extra 15% area-power product decrease. The combination of design techniques (i.e. SSPA) and circuit reliability simulations (i.e. operating voltage optimization) thus yields an area-power product improvement of 89% when compared to the design at the nominal supply voltage.

V. Conclusions

Transistor reliability is a major concern for analog circuit design in deeply scaled nanometer CMOS technologies. With the introduction of high-k materials existing aging effects remain or even become worse. The paper clearly has shown the potential of advanced circuit reliability simulation tools and novel design techniques to improve circuit reliability and performance in deeply-scaled CMOS technologies. This has been demonstrated on a 6-bit 32nm CMOS current-steering DAC where the area-power product of the analog part of the circuit was reduced with 89% when compared to a conventional design.

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References

[1] "International Technology Roadmap for Semiconductors (ITRS)," http://www.itrs.net/Links/2009ITRS/Home2009.htm, 2009.
[2] E. Maricau *et al*, "An analytical model for hot carrier degradation in nanoscale CMOS suitable for the simulation of degradation in analog IC applications," *Microelectronics Reliability*, 2008.
[3] E. Amat *et al*, "Channel Hot-Carrier degradation in short channel devices with high-k/metal gate stacks," *CDE*, pp. 238–241, 2009.
[4] L. Lewyn *et al*, "Analog Circuit Design in Nanoscale CMOS Technologies," *Proceedings of the IEEE*, 2009.
[5] E. Maricau *et al*, "NBTI Model for Analog IC Reliability Simulation," *EL*.
[6] M. Cho *et al*, "Positive and negative bias temperature instability on sub-nanometer EOT high-K MOSFETs," *IRPS*, pp. 1095–1098, 2010.
[7] B. Kaczer *et al*, "Statistics of Multiple Trapped Charges in the Gate Oxide of Deeply Scaled MOSFET Devices, Application to NBTI," *EDL*, 2010.
[8] S. Pae *et al*, "Reliability characterization of 32nm high-K and Metal-Gate logic transistor technology," *IRPS*, pp. 287–292, 2010.
[9] G. Bersuker *et al*, "Mechanism of high-k dielectric-induced breakdown of the interfacial SiO2 layer," *IRPS*, pp. 373–378, 2010.
[10] M. Alam *et al*, "A study of soft and hard breakdown-Part II: Principles of Area, Thickness and Voltage Scaling," *TED*, 2002.
[11] G. Groeseneken *et al*, "Trends and perspectives for electrical characterization and reliability assessment in advanced CMOS technologies," *ESSDERC*, pp. 64–72, 2010.
[12] R. Tu *et al*, "Berkeley reliability tools-BERT," *TCAD*, 1993.
[13] R. Degraeve *et al*, "Review of reliability issues in high-k/metal gate stacks," *IPFA*, pp. 1–6, 2008.
[14] G. Gielen *et al*, "Emerging yield and reliability challenges in nanometer CMOS technologies," in *DATE*, 2008.
[15] E. Wu *et al*, "Power-law voltage acceleration: A key element for ultra-thin gate oxide reliability," *Microelectronics Reliability*, 2005.
[16] E. Maricau and G. Gielen, "Stochastic circuit reliability analysis," *DATE*, 2011.
[17] P. Ko *et al*, "Hot-electron-induced MOSFET degradation-model, monitor, and improvement," *TED*.
[18] S. Tam *et al*, "Lucky-electron model of channel hot-electron injection in MOSFET'S," *TED*, 1984.
[19] H. Kufluoglu and M. Alam, "A geometrical unification of the theories of NBTI and HCI time-exponents and its implications for ultra-scaled planar and surround-gate MOSFETs," *IEDM*.
[20] D. Schroder *et al*, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing," *JAP*, 2003.
[21] J. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: A review," *Microelectronics Reliability*, 2006.
[22] B. Kaczer *et al*, "Ubiquitous relaxation in BTI stressing? New evaluation and insights," *IRPS*, 2008.
[23] D. Montgomery, "Design and analysis of experiments," 2009.
[24] E. Maricau and G. Gielen, "Efficient variability-aware nbti and hot carrier circuit reliability analysis," *TCAD*, 2010.
[25] T. Chen and G. Gielen, "A 14-bit 200-MHz Current-Steering DAC With Switching-Sequence Post-Adjustment Calibration," *JSSC*, 2007.
[26] M. Pelgrom *et al*, "Matching properties of MOS transistors," *JSSC*, 1989.