Stochastic Circuit Reliability Analysis

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***Abstract*—Stochastic circuit reliability analysis, as decribed in this work, matches the statistical attributes of underlying device fabrics and transistor aging to the spatial and temporal reliability of an entire circuit. For the first time, spatial and temporal stochastic and deterministic reliability effects are handled toghether in an efficient framework. The paper first introduces an equivalent transistor SPICE model, comprising the currently most important aging effects (i.e NBTI, hot carriers and soft breakdown). A simulation framework then uses this SPICE model to minimize the number of circuit factors and to build a circuit model. The latter allows for example very fast circuit yield analysis. Using experimental design techniques the proposed method is very efficient and also proves to be very flexible. The simulation technique is demonstrated on an example 6-bit current-steering DAC, where the creation of soft breakdown spots can result in circuit failure due to increasing time-dependent transistor mismatch.**

***Index Terms*—NBTI, Hot Carrier Degradation, TDDB, SBD, HBD, Failure-Resilience, Aging, Design for Reliability.**

I. Introduction

Integrated circuits processed in ultra-scaled CMOS processes are more than ever subject to various statistical reliability effects such as process variations, noise, breakdown effects, etc [1]. Fig. 1 illustrates how spatial stochastic reliability effects (i.e. parametric process variations) affect the yield of a circuit, right after production. At this point, a circuit is considered unreliable if the yield is too small. Once in use, temporal (i.e. time-dependent) wear-out effects also affect the reliability of a circuit (see Fig. 1 and Fig. 2). Temporal deterministic reliability effects such as Negative Bias Temperature Instability (NBTI) and Hot Carrier degradation (HC) cause a shift in transistor parameters (e.g. threshold voltage), possibly resulting in circuit malfunction. Additionally, temporal stochastic reliability effects such as soft breakdown also become increasingly important in sub 90nm processes. The latter cause a shift of transistor parameters (e.g. gate conductance) as well, but, since they are stochastic in nature, they can also cause circuit failure resulting from increasing time-dependent transistor mismatch. The combined effect of deterministic and stochastic reliability effects can significantly reduce the yield of a circuit within its lifetime [1], [2]. In this work an example 6-bit binary-weighted current-steering DAC is studied. The DAC requires a $\frac{\sigma(I_{\text{LSB}})}{I_{\text{LSB}}} \leq 0.13$ to achieve an initial yield of 99.9% and temporal reliability effects will increase the relative error on each current source, causing a yield reduction of just under 2% over an operational lifetime of 5 year.

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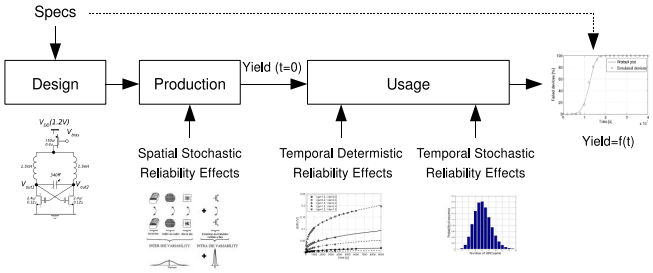

Fig. 1. Spatial and temporal deterministic and stochastic reliability effects can have a large impact on the yield of a circuit as a function of its lifetime.

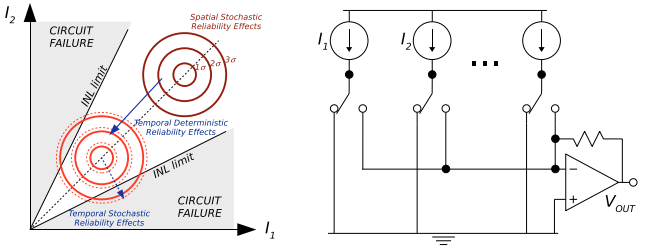

Fig. 2. The integral nonlinearity (INL) of a current-steering digital-to-analog converter is observed. Spatial stochastic reliability effects introduce an initial relative error $\sigma(I)/I$ on each current source. Temporal reliability effects can increase this initial until finally the circuit fails (i.e. INL≤ 0.5LSB).

The reliability issues described above i) force designers to use large design margins, ultimately limiting circuit performance, and ii) increase uncertainty on the lifetime of a circuit. Traditional design tools using deterministic device compact models combined with standard SPICE simulators are therefore no longer sufficient to design a reliable circuit. Unfortunately, emulating the impact of stochastic effects on a circuit or a system generaly demands a lot of computing power. In previous work, the authors demonstrated how the usage of design of experiments can be very efficient for analyzing the interaction between parametric process variations and deterministic aging effects [3]. This work presented here builds upon this method and adds temporal stochastic reliability effects, resulting in an efficient technique for stochastic circuit reliability analysis. The proposed methodology is therefore the first to combine:

1) Spatial stochastic reliability effects (i.e. parametric process variations)
2) Temporal deterministic reliability effects (i.e. NBTI and Hot Carrier degradation)
3) Temporal stochastic reliability effects (i.e. Soft Breakdown)

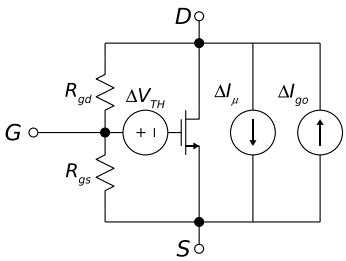

Fig. 3. An equivalent transistor SPICE model emulates the cumulative effect of all transistor wear-out mechanisms. ΔV_{TH}, ΔI_{μ} and ΔI_{go} result from NBTI and HC degradation [7], [8]. R_{gs} and R_{gd} model the SBD induced increase of the gate current.

The paper is organized as follows. Section II describes relevant previous work in the area of circuit reliability analysis. Section III discusses an comprehensive transistor model for wear-out effects in nanometer CMOS technologies. The simulation framework is explained in detail in section IV and demonstrated on a current-steering DAC in section V. Finally conclusions are drawn in section VI.

II. Relevant Work

Over the last two decades, various software solutions to analyze the effect of transistor aging on analog and digital circuits have been reported [3]–[5] and commercial tools such as the ELDO reliability simulator and RelXpert have been developed. Most tools do however not consider temporal stochastic reliability effects or only treat it as a deterministic effect (e.g. only estimating the impact of a first breakdown using the time to first breakdown for the 63rd percentile) [4]. Sasse [6] proposed a Monte-Carlo-based method to emulate the impact of multiple breakdowns on the operation of a circuit. In his work, he demonstrated how such a simulator can either relax circuit specifications or reveal very specific reliability issues. But, although accurate, Sasse's method is very computationally intensive and therefore in practice only suited for very small circuits (i.e. 10 transistors or less). Although each of the papers reviewed above provided valuable contributions and new ideas to find a more efficient and/or more accurate method to estimate the reliability of a circuit, none of them properly combined all of these effects in one solution. The intent of this work is to do just that and to provide a first approach to efficiently implement stochastic circuit reliability analysis for use on larger mixed-signal circuits.

III. Transistor Wear-out Effect Modeling

HC degradation (HC), NBTI and Soft Breakdown (SBD) are considered to be the most important transistor wear-out effects in current CMOS technologies. HC and NBTI result in an increase of the threshold voltage, a decrease of the carrier mobility and an increase of the output conductance, modelled as ΔV_{TH}, ΔI_{μ} and ΔI_{go} respectively (see Fig. 3). Compact models for both effects are presented in [7] and [8]. Breakdown (BD) results from oxide damage due to strong electric fields in nanometer CMOS technologies and gives rise to an increase of the transistor gate current. For oxide thicknesses below 5nm, Hard BD (HBD) can be preceeded by SBD [1]. SBD can be observed as partial loss of the dielectric properties, resulting in a smaller increase of the gate current when compared to HBD. However, Alam [9] showed that the occurance of HBD is very unlikely in a nanometer CMOS technology. HBD is therefore not considered here. The probability to have n SBD defects at time χ can be described with a Poisson distribution [10]:

$$P_n(t) = \frac{\chi^n}{n!}\exp(-\chi) \tag{1}$$
$$\chi = \left(\frac{t}{t_{SBD}}\right)^{\beta}$$
$$t_{SBD} = t_{63}\left(\frac{WL}{A_{ref}}\right)^{1/\beta}\left(\frac{E_{ox}}{E_{ref}}\right)^{\gamma}$$

where t_{63} is the time to breakdown at the 63rd percentile for a reference transistor with area A_{ref} stressed at E_{ref}. β and γ are process-dependent parameters. Formula (1) is only valid for fixed stress voltages. And, while a circuit is aging, the transistor stress voltages might change due to aging-induced transistor parameters shifts. A dynamic SBD model, including support for changing operating points, is therefore required. To find such a model, the probability to have n SBD spots at time t_2, $P_{n'}(t_1)$, has to be looked at as the sum of probabilities to achieve n' SBDs at time t_1, followed by the probability to create an extra $n - n'$ breakdown spots between t_1 and t_2:

$$P_n(t_2) = \sum_{n'=0}^{\infty}\left[P_{n'}(t_1)\frac{\Delta\chi^{n-n'}}{(n-n')!}\exp(-\Delta\chi)\right] \tag{2}$$
$$\Delta\chi = \left(\frac{t_2 - t_1}{t_{SBD}|_{E_{ox}=E_{ox,2}}}\right)^{\beta}$$

where $n \geq n'$, $E_{ox,1}$ the stress at t_1, $E_{ox,2}$ the stress at t_2 and $E_{ox,1}$ and $E_{ox,2}$ not necessarily the same. Model parameters where extracted from measurements published in [10] and [11]. The creation of a SBD spot manifests itself as an increase in the gate current and is modelled with a resistor from gate to drain and a resistor from gate to source (i.e. R_{gd} and R_{gs} in Fig. 3). Each resistor is modelled using formula (2), with E_{ox} being the gate-source stress for R_{gs} and the gate-drain stress for R_{gd} and L being half of the actual transistor length.

IV. Stochastic Reliability Analysis

A. Concept

Spatial stochastic reliability effects such as parametric process variations have a significant impact on the performance of a circuit right after production. The pool of potentially fabricated circuits resulting from these variations, can be described by an n_s-dimensional circuit factor space $\mathcal{F}$, where every dimension or factor $f_{s,i};\ i = \{1, \ldots, n_s\}$ represents a fixed design parameter or a technology parameter with a process-dependent statistical spread. Every factor $f_{s,i}$ is characterised by a mean and a standard deviation. Data for each factor can come from test structures on wafers or from

SPICE simulations on models that have been characterized by the foundry. Examples of these factors are resistor values, transistor width and length and gate-oxide thickness. In addition to spatial stochastic reliability effects, temporal stochastic reliability effects, such as soft breakdown, also have an impact on the distribution of sample circuits. $\mathcal{F}$ is therefore augmented with n_t time-dependent factors $f_{t,j}$; $j = \{1, \ldots, n_t\}$. In contradiction to the spatially related factors $f_{s,i}$, the distribution of these factors $f_{t,j}$ changes as a function of time. Two examples of such a time-dependent factor are the values of R_{gd} and R_{gs} to model SBD (see section III). The total number of factors in $\mathcal{F}$ is now $n = n_s + n_t$. The upper left graph on Fig. 4 depicts an example of a two-dimensional factor space, where $f_{t,1}$ represents a temporal stochastic reliability parameter and $f_{s,1}$ represents a spatial stochastic reliability parameter. Every circuit in $\mathcal{F}$ has a behavior defined by m circuit performance parameters (e.g. DC gain, bandwidth, etc), corresponding to a point in an m-dimensional circuit performance space $\mathcal{P}$. At time $t_0 = 0$ [sec], every circuit sample $\mathbf{f} = [f_{s,1}, \ldots, f_{s,n_s}, f_{t,1}, \ldots, f_{t,n_t}]$ in $\mathcal{F}$, can therefore be mapped on a point $\mathbf{P}^0 = [P_1^0 \ldots P_m^0]$ in $\mathcal{P}$ (see Fig. 4 upper right). However, when the circuit ages, the behavior of the circuit can change. This will result in a new point $\mathbf{P}^i$, for every sample $\mathbf{f}$, at every time point t_i. The time-dependent shift of a point in $\mathcal{P}$ originates from temporal deterministic and stochastic reliability effects. The time-dependent statistical spread on a set of points $\mathbf{P}^i$ at time point i, on the other hand, results from spatial and temporal *stochastic* reliability effects. The link between $\mathcal{F}$ and $\mathcal{P}$ is defined as ϑ:

$$\mathbf{P}^i = \vartheta(\mathbf{f}, t_i) \text{ with } \mathbf{f} \in \mathcal{F} \text{ and } \mathbf{P}^i \in \mathcal{P} \tag{3}$$

The circuit also has to meet application-dependent circuit specifications (i.e. $\mathbf{P}_{min}$ and $\mathbf{P}_{max}$). Every circuit violating these specifications will result in yield loss and, since every circuit ages over time, the yield Y will be time-dependent (see Fig. 4 bottom):

$$Y_i = \phi(t_i, \mathbf{P}_{min}, \mathbf{P}_{max}) \tag{4}$$

with Y_i the yield at time t_i. A stochastic reliability analysis tool, as discussed in this paper, efficiently quantifies the reliability of a circuit via ϑ and ϕ

As an example, Fig. 5 illustrates the effect of spatial and temporal stochastic reliability effects on a simple current mirror. The circuit was designed to achieve an initial relative error $\sigma(I)/I \leq 0.07$ on each output current. The circuit was then simulated over a stress time of 10 years and evaluated after 0, 5 and 10 years. Temporal deterministic reliability effects, in this case NBTI, decrease the overall output current because the threshold voltage increases and the carrier mobility decreases. But, since the operating temperature and the stress voltages are fairly low, this effect is negligible here. Temporal stochastic reliability effects under the form of SBD, on the other hand, have a large effect on i) the overall current (i.e. I increases from $4.8\mu A$ to $5.9\mu A$ over 10 year) and ii) on the relative output current error (i.e. $\sigma(I)/I$ increases from 0.07 to 0.13 over 10 year). As a result, some of the circuits even fail the

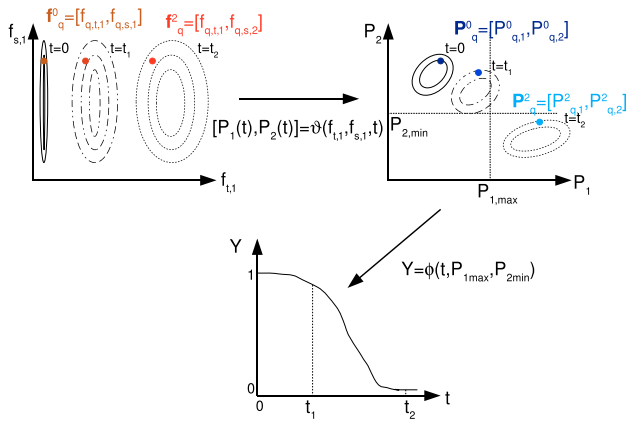

Fig. 4. Example representation of a 2-dimensional factor space $\mathcal{F}$ (upper left), resulting in a 2-dimensional performance space $\mathcal{P}$ (upper right). Every point in $\mathcal{F}$ maps on a set of points in $\mathcal{P}$. Each set shifts as a function of time, due to temporal deterministic and stochastic reliability effects, while the statistical spread on each set changes due to spatial and temporal stochastic reliability effects. Adding circuit specifications ($P_{1,max}$ and $P_{2,min}$) results in a time-dependent yield Y (bottom).

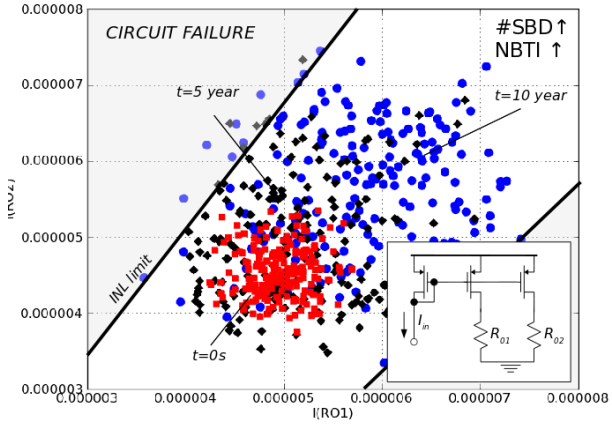

Fig. 5. Soft breakdown simulation of a current mirror, evaluated after a circuit lifetime of 0 (red squared markers), 5 (black diamond markers) and 10 (blue round markers) year.

INL limit (i.e. the maximum current error to achieve an overall INL≤ 0.5LSB when the circuit would be integrated in a 6-bit IDAC) at the 5 or 10 year time point (see Fig. 5).

B. Factor Minimization

Temporal stochastic reliability effects manifest themselves as a set of time-dependent factors in $\mathcal{F}$. When including soft breakdown in the circuit analysis flow, for example, two extra factors are needed per transistor (i.e. R_{gs} and R_{gd}, see section III). Including temporal stochastic reliability effects therefore drastically increases the number of factors per circuit. Fortunately, in a real circuit, only a very limited number of transistors will age in such a way that they have a significant effect on the performance of the circuit. For example, the creation of soft breakdown spots in a transistor will only affect circuit performance if (see section III):

- a large gate-source or gate-drain voltage stress is applied (i.e. $\geq 0.5V$)
- the transistor has a large area
- the transistor is driving a small current (i.e. increase in the gate current due to SBD has a large effect)

To reduce the overall simulation time, the number of time-dependent factors is therefore minimized, based on the results of a circuit sensitivity analysis (see Algorithm 1). The input

Algorithm 1 FACTOR MINIMIZATION ALGORITHM

1: INPUT: $\mathbf{f} = \{f_{s,q}, f_{t,r}\};\ q = 1, \ldots, n_s;\ r = 1, \ldots, n_t$
2: Create nominal netlist:
$\mathbf{f} = [0, 0, \ldots, 0]$
3: Evaluate netlist over time T_{str}:
$\mathbf{P}^k = \vartheta(\mathbf{f}, k = [0, \ldots, T_{str}])$
4: Perform sensitivity analysis:
5: **for** $f_{t,i}$ in circuit **do**
6: Evaluate netlist without $f_{t,i}$:
$\mathbf{f}_{\bar{i}} = \{f_{s,q}, f_{t,r}\};\ r \neq i$
$\mathbf{P}^k_{\bar{i}} = \vartheta(\mathbf{f}_{\bar{i}}, k = [0, \ldots, T_{str}])$
7: Calculate netlist sensitivity to $f_{t,i}$:
$S^{\mathbf{P}}_{\bar{i}} = \frac{\mathbf{P}^{T_{str}}_{\bar{i}} - \mathbf{P}^{T_{str}}}{\mathbf{P}^0 - \mathbf{P}^{T_{str}}}$
8: **end for**
9: Minimize the number of factors:
f' $= \{f_{s,q}, f_{t,r'}\}$;
$q = 1, \ldots, n_s;\ r' = \{i\}$ with $S^{\mathbf{P}}_{\bar{i}} > 0.05\text{max}(S^{\mathbf{P}})$
10: OUTPUT: **f'**

to the algorithm is a collection of all the circuit factors, both spatial and temporal. First, a nominal version of the circuit is evaluated over stress time T_{str} [3]. In a second step, the circuit performance sensitivity $S^{\mathbf{P}}_{\bar{i}}$ to each time-dependent factor $f_{t,i}$ is calculated:

$$S^{\mathbf{P}}_{\bar{i}} = \frac{\mathbf{P}^{T_{str}}_{\bar{i}} - \mathbf{P}^{T_{str}}}{\mathbf{P}^0 - \mathbf{P}^{T_{str}}} \tag{5}$$

where $\mathbf{P}^{T_{str}}$ represents the circuit performance at time T_{str}, $\mathbf{P}^{T_{str}}_{\bar{i}}$ is $\mathbf{P}^{T_{str}}$ but with factor $f_{t,i}$ set to its initial value and $\mathbf{P}^0$ is the circuit performance at time $t = 0$. Finally, factors with very little impact on the overall circuit behavior, over the entire stress time, are removed from the factor space $\mathcal{F}$ and not considered for further circuit analysis. The output of Algorithm 1 is a reduced set of circuit factors that serves as an input for the further circuit analysis with design of experiments (as described in section IV-C).

Fig. 6 illustrates the result of Algorithm 1 on an advanced current mirror. The circuit contains 8 transistors resulting in a factor space with 40 dimensions (i.e. $n_s = 24$ and $n_t = 16$). Even an analysis with only two levels per factor, to screen out unimportant factors and assuming each factor is independent, would take at least 80 reliability simulations evaluated over the entire stress time T_{str}. The simulation method, as presented

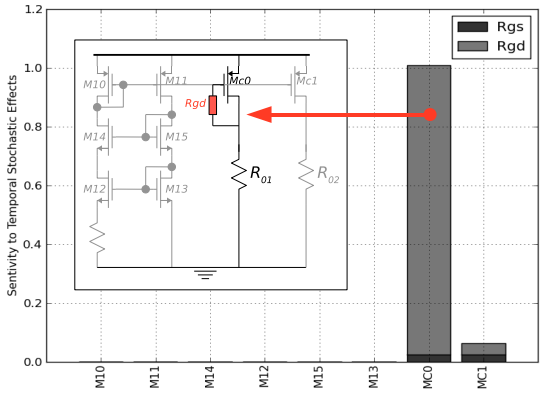

Fig. 6. Sensitivity of the output current of an advanced current mirror to temporal stochastic reliability effects.

here, reduces the number of factors based on only 1 reliability simulation. In this example I_{o1} (i.e. the current through M_{c0}) was opserved as output of the circuit (i.e. $\mathbf{P}$). The result of the analysis is depicted in Fig. 6 and indicates how I_{o1} is only sensitive to breakdowns generated between the gate and drain of transistor M_{c0}. The number of time-dependent circuit factors is thus reduced from 16 to 1, and the overall circuit analysis time also decreases significantly.

C. Stochastic Circuit Analysis with Design of Experiments

Once the number of circuit factors is reduced, further circuit analysis to quantify the link between the factor space $\mathcal{F}$ and the circuit performance space $\mathcal{P}$ is needed. In [3], the authors introduced an efficient technique to analyze the impact of process variability on circuit aging. The latter does however only includes spatial stochastic and temporal deterministic reliability effects, while the flow presented here does also include temporal stochastic reliability effects. The simulator generates a Response Surface Model (RSM) $\hat{\vartheta}$ to approximate ϑ (see section IV-A). This RSM can be evaluated in a very short time frame and therefore allows very fast yield calculation. To find a sufficiently accurate RSM, a design of experiments (DoE) technique is used. These well-known information gathering techniques allow to extract a maximum amount of information, with a minimum set of experiments (or simulations) [12]. Each DoE consists of a well-chosen set of points in $\mathcal{F}$, which are all evaluated with a nominal reliability simulator to find values in $\mathcal{P}$. The purpose of the latter is to evaluate a specific circuit sample over its entire lifetime [3]. The experiments and the corresponding simulation results can then be used to create $\hat{\vartheta}$. Fig. 7 depicts a schematic representation of the proposed simulation flow. The input to the simulator is a fresh (i.e. unstressed) netlist and a testbench. In a first step, spatial and temporal circuit factors are extracted from the input netlist (see 'Circuit Factor EXTRACTION' on Fig. 7). In a second step, the number of temporal factors is reduced with a sensitivity analysis (see section IV-B). Next, a set of Design of Experiments (DoE) (see [3]) is used to explore

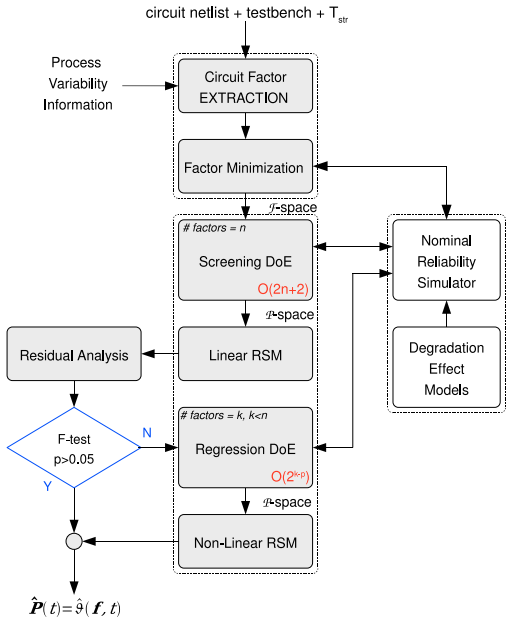

Fig. 7. The stochastic reliability simulation flow.

the behavior of the test circuit, as a function of every circuit factor. Every experiment is evaluated by a nominal reliability simulator to calculate the aged version of that sample circuit [3]. Then, a response surface model $\hat{\vartheta}$ is generated based on the output of the DoEs. And finally, $\hat{\vartheta}$ can be evaluated by a designer to calculate, for example, the time-dependent yield.

V. Experimental Results

The proposed framework is demonstrated on a 6 bit binary-weighted current-steering Digital-to-Analog Converter (IDAC) (see Fig. 8). The overall simulation accuracy of the proposed method depends on:

1) the correctness of the transistor wear-out effect model.
2) the accuracy of the RSM $\hat{\vartheta}'$, emulating the link between the factor space and the performance space.

The former is discussed in section III and were validated through single-transistor measurements [8], [10], [11], [13]. The latter depends on the choice of design of experiments and the type of RSM and was validated in [3] (also see section IV). The circuit under study is designed in a 90nm CMOS technology. The experiments have been executed on a dual-quad core 2.8GHz Intel Xeon processor with 8GB of RAM.

A. The Current Sources

The current sources generating the binary-weighted output currents are crucial elements in the DAC (see Fig. 8). Each current source is designed to generate a specific output current. Therefore a change or variation of this current can cause an erroneous value at the output of the DAC. To minimize process variation induced mismatches large gate-source voltages (i.e. 0.5V) and larger than minimum-sized transistor lengths are used. This guarantees an initial yield of 99.9% (i.e. INL$\leq$ 0.5LSB). Unfortunately, both the usage of large transistors and large V_{GS} voltages worsen deterministic (i.e. NBTI) and stochastic (i.e. SBD) aging effects (see also Fig. 5):

- NBTI increases the absolute value of the threshold voltage and output conductance and decreases the carrier mobility. As a result the output current and output resistance of each current source reduces over time.
- The formation of SBD spots increases gate leakage. And, being a stochastic phenomenon, SBD will also induce an time-dependent mismatch.

B. The Transimpedance Amplifier

The transimpedance amplifier comprises an OTA and a resistive feedback element R_{OTA} (see Fig. 8). The circuit converts an input current to an output voltage. The transfer function of this circuit is mainly determined by the size of the resistor:

$$\frac{V_{\text{OUT}}}{I_{\text{IN}}} = R_{\text{OTA}} \frac{A_{\text{OTA}}}{1 + A_{\text{OTA}}} \approx R_{\text{OTA}} \tag{6}$$

with A_{OTA} the OTA open loop gain. R_{OTA} is not affected by aging phenomena. The performance of the transimpedance amplifier will therefore remain fairly constant over its entire lifetime (i.e. provided that the gain of the OTA remains large enough, which is true in this example).

C. The Current-steering DAC

The entire IDAC circuit was analyzed over a lifetime of 10 years. The simulation took 25 minutes. The circuit contains 31 transistors, resulting in 96 spatial factors (i.e. $n_s = 96$) and 62 temporal factors (i.e. $n_t = 62$). Fig. 9 depicts the result of the sensitivity analysis to reduce the number of factors prior to the stochastic analysis with design of experiments: from the 62 temporal factors only 4 remained. Fig. 10 depicts the result of the nominal reliability simulation (i.e. no statistical effects) showing the absolute value of the aging-induced threshold voltage shift ΔV_{TH} for each transistor in the circuit. Altough for each transistor, ΔV_{TH} is fairly small (i.e. maximum 64mV for M14), it can cause a minor shift of the overall circuit performance and contributes to the increase in performance spread. Finally, Fig. 11 shows the result of the stochastic circuit reliability analysis and plots the integral nonlinearity (INL) at time $t = 0$ and after 5 years of operation. The initial circuit performance distribution, resulting from parametric process variations, clearly increases over time due to temporal reliability effects. Right after production, the yield is 100%, while the yield is reduced to 98.3% after a lifetime of 5 years. Although just under 2% is not much, for circuits in mass production with a long life expectancy (e.g. in automotive or biomedical applications), this yield loss might result in a major reliability problem with large consequences.

VI. Conclusions

The paper has discussed how spatial reliability effects combined with temporal stochastic and deterministic reliability effects can impact the operation of an ultra-scaled CMOS circuit over its lifetime. The authors have proposed an efficient method consisting of i) a statistical transistor aging model,

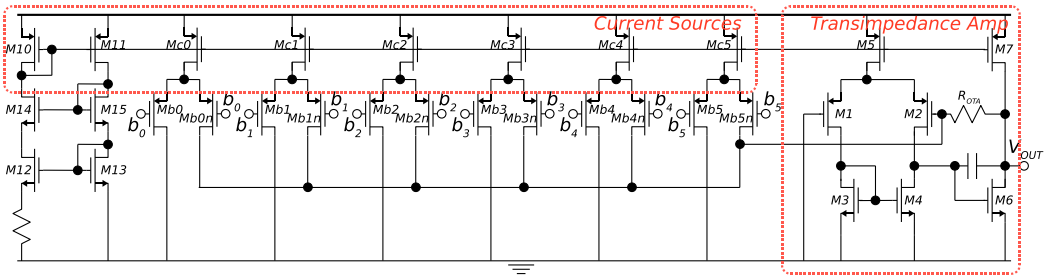

Fig. 8. The 6-bit current-steering digital-to-analog converter.

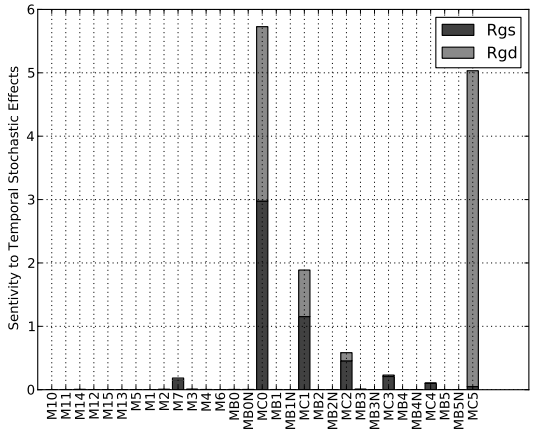

Fig. 9. Sensitivity of the IDAC INL to temporal stochastic reliability effects.

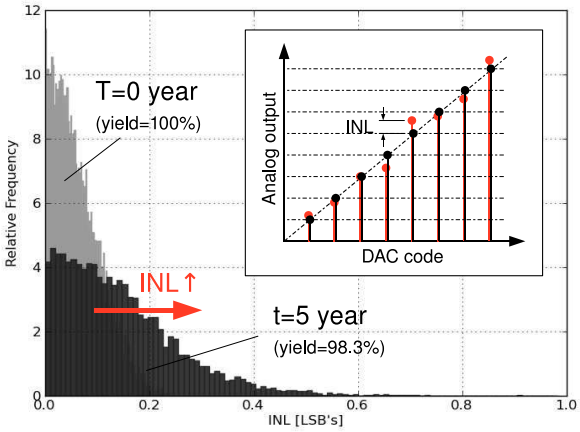

Fig. 11. IDAC performance shift over 5 years of operation.

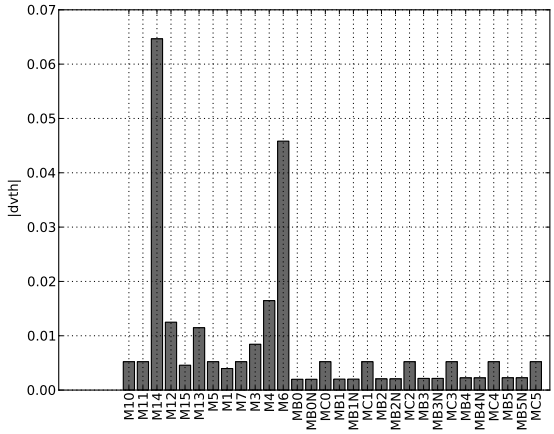

Fig. 10. Threshold voltage shift for each transistor after 10 year.

ii) a screening analysis to reduce simulation time and iii) an efficient stochastic circuit reliability analyzer based on design of experiment techniques. The method has been demonstrated on a 6-bit current-steering DAC and indicated how temporal stochastic reliability effects such as soft breakdown can reduce circuit yield over time. Tools such as the one described in this work are needed in nanometer CMOS technologies to predict and anticipate possible circuit performance shift and to guarantee a 100% yield over the entire lifetime of the product.

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