Case Study: Alleviating Hotspots and Improving Chip Reliability via Carbon Nanotube Thermal Interface

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***Abstract*—The increasing power consumption of integrated circuits (ICs) enabled by technology scaling requires more efficient heat dissipation solutions to improve overall chip reliability and reduce hotspots. Thermal interface materials (TIMs) are widely employed to improve the thermal conductivity between the chip and the cooling facilities. In recent years, carbon nanotubes (CNTs) have been proposed as a promising TIM due to their superior thermal conductivity. Some CNT-based thermal structures for improving chip heat dissipation have been proposed, and they have demonstrated significant temperature reduction. In this paper, we present an improved CNT TIM design which includes a CNT grid and thermal vias to dissipate heat more efficiently to obtain a more uniform chip thermal profile. We present simulation-based experimental results that indicate a 32% / 25% peak temperature reduction and 48% / 22% improvement in chip reliability for two industrial processor benchmarks, showing the effectiveness of our proposed thermal structure.**

I. Introduction

While process scaling has enabled increasing device integration, it has also resulted in higher power density and thermal effects in ICs. Higher power consumption and temperature affect circuit performance (*e.g.*, reduced threshold voltage V_{th}, increased wire resistance), reliability (*e.g.*, negative-bias temperature instability (NBTI), electromigration, dielectric breakdown), and IC packaging. The International Technology Roadmap for Semiconductors predicts that the power dissipation levels of "cost-performance" and "high-performance" ICs will reach 1.73 W/mm^2 and 0.43 W/mm^2, respectively, by 2022 [1].

Cooling solutions such as air fans or liquid-based techniques (*e.g.*, heat pipes) can dissipate in excess of 100W. However, significant thermal contact resistance at multiple interfaces from the die through the heat spreader to the heat sink remains a challenging problem. Limited cooling capabilities of the package give rise to localized heating spots, known as hotspots, at highly active regions of a chip. While IC design methods (*e.g.*, dual V_{th}, runtime thermal management) can help alleviate some of the aforementioned problems, novel TIMs and structures need to be explored that can continue to meet the ever-increasing packaging demands of future ICs. TIMs fill the gaps between thermal transfer surfaces. Because TIMs possess higher thermal conductivity than air, the thermal contact resistance is reduced, thereby lowering the temperature at the junction.

CNTs exhibit extraordinary structural, electrical, and thermal characteristics. Due to their high thermal conductivity and small thermal contact resistance than traditional TIMs, CNTs have been investigated for their use as a TIM between the die and the heat spreader. The thermal conductivity k of single multi-walled CNT (MWCNT) and single-walled CNT (SWCNT) is reported to be 3,000 and 5,000–8,000 W/m·K, respectively [2]. For CNT bundles, k is in the range of 1,750–5,800 W/m·K [3]. This is significantly higher than copper where k is 400 W/m·K. Furthermore, the thermal contact resistance of CNT arrays with a copper interface is reported to be only about 10 mm^{2}K/W [4]. Thus, CNTs are exhibiting very promising results for usage as a TIM.

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Simple and efficient methods for growing highly aligned and densely packed CNTs on silicon surfaces were demonstrated in [4]. Horizontal and vertical aligned CNTs were presented in [5]. Furthermore, researchers have also shown how different CNT junction patterns can be created [6]. These methods will enable many CNT-based structures to be feasible as a TIM. The authors in [7] simulated the use of CNTs as thermal interconnects for on-die heat transfer between hot and cool (areas of lower activity) regions in silicon-on-insulator (SOI) based ICs. The authors in [8] proposed a via-based grid where thermal through silicon vias (TTSVs) are allocated to specific regions on the chip for thermal management of 3D ICs.

In this case study, we present a novel CNT-based 3D grid structure as the TIM layer. In our structure, CNT thermal vias improve the heat dissipation between the silicon substrate and the heat spreader. The horizontal CNT mesh balances the temperature across the chip, and reduces peak temperature which is critical for improving chip reliability. By routing the heat from hotspots to the entire die, the heat dissipation area is no longer constrained by the hotspot area. Consequently, more heat can be dissipated from the heat spreader. The relation between via density and temperature distribution is also studied. Therefore, the advantages of both CNT TIM and CNT thermal vias are leveraged to improve heat dissipation in both horizontal and vertical directions. The peak temperature improvement of two industrial processors are investigated under two scenarios: (a) assuming ideal thermal conductivity, and (b) using practical thermal conductivity for CNT arrays. The results demonstrate excellent thermal profile improvement in both cases.

ISAC2 [9], which has the ability to perform space- and time-adaptive chip-package thermal analysis, was used to simulate the Alpha 21364 and OpenSparc T1 [10] processor benchmarks. The power profiles of the benchmarks in our experiments were obtained from the architectural simulator McPAT [11]. Finally, since the operating temperature has a significant impact on circuit aging (*i.e.*, NBTI), the effect of the proposed structures on circuit reliability improvement was also analyzed.

The contributions of this work are as follows:

- This is the first case study to investigate a CNT-based grid structure TIM and thermal vias for IC thermal management;
- We present simulation results on two industrial designs, and show the beneficial impacts of using proposed scheme to improve the chip thermal profile and circuit reliability issues such as NBTI; and
- Both theoretical and practical scenarios with corresponding parameters are demonstrated.

The rest of this paper is organized as follows. Section II provides background material that will be helpful in understanding the ideas presented in this work. Section III describes our proposed CNT-based thermal management structure in detail. To justify such a structure, we also comment on the possible manufacturing scheme

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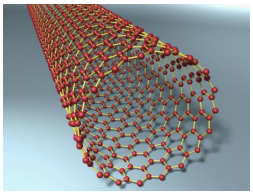
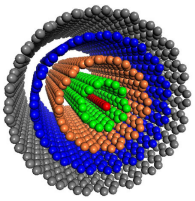


(a) Single-walled [12].



(b) Multi-walled [13].

Fig. 1. Types of CNT structure.

given the current state of CNT fabrication. The simulation setup and experimental results are presented in Section IV. We conclude this paper in Section V.

II. Preliminaries

In this section, we present some background material that will be helpful in understanding the remainder of this paper.

A. Carbon Nanotubes

CNTs are one-dimensional conductors which may be visualized as a rolled-up mono-layer (Fig. 1(a)) or multi-layers (Fig. 1(b)) of graphite with diameters and lengths in the nanometer and millimeter range, respectively [14]. Furthermore, depending upon their chirality (*i.e.*, "twist"), they can be either semiconducting or metallic. CNTs have many remarkable electronic and mechanical characteristics, such as high thermal conductivity and ballistic current transport. CNTs have attracted immense attention within the research community for their potential usage in a wide range of applications. As mentioned earlier, because their thermal conductivity is around 8-15 times higher than that of copper, CNTs are an attractive candidate to replace copper for on-die heat transfer.

B. Thermal Management Structure

Fig. 2 shows the typical thermal management configuration of an IC. Solder bumps are deposited on the IC pads during the final wafer processing. The chip is then flipped and bonded with the packaging to interface with the external world. A heat spreader is used to dissipate or "spread" out excess heat from the IC (heat source) to the secondary heat exchanger (*i.e.*, heat sink). The heat spreader, typically a copper plate, works most efficiently when the heat is uniformly distributed over the entire IC substrate [7]. Fins are commonly added to the heat sink to increase the surface area to achieve higher heat removal efficiency. A cooling mechanism such as air fans is integrated with the heat sink to dissipate the heat into external environment. A TIM, typically commercial silicone "grease", is added between the die and the heat spreader to improve thermal conductivity.

Recently, TTSVs have been proposed for insertion into a chip for better heat conduction from the device layer to the heat sink. This is shown in Fig. 3. The implementation of TTSVs has been realized by various approaches. The most common method is to fill the vias with metal (*e.g.*, copper, tungsten), and then, wrap the vias with an insulation layer. Studies have reported temperature reductions of up to 50% using silicon "dummy thermal vias" [15].

C. IC Thermal Analysis

Heat transfer modeling is typically performed by partitioning the chip and cooling package into discrete three-dimensional thermal elements. Compact heat transfer equations are then derived and solved using numerical techniques to characterize the thermal profile of the

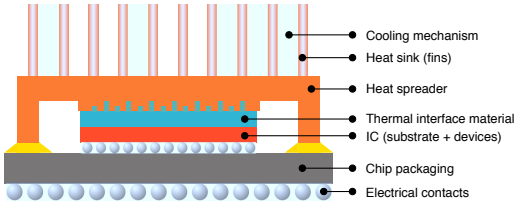


Fig. 2. Typical IC thermal management scheme.

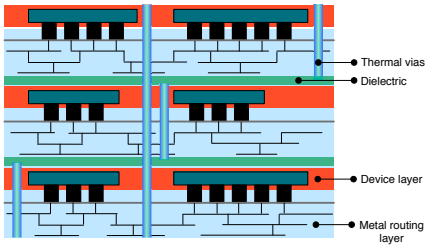


Fig. 3. Using TTSVs to improve heat conduction from die to heat sink [15].

IC. Virtually all methods are based on the steady-state Fourier heat flow model given by the following equation:

$$\nabla \cdot \left(k \nabla T\right) + q_{vol} = 0, \tag{1}$$

where k is the material's thermal conductivity, ∇T is the temperature gradient, and q_{vol} is the volumetric heat source. The Fourier model can efficiently and accurately model the thermal effects at feature length scales much longer than the mean free path of phonons (*i.e.*, 200-300 nm in silicon). In the nanometer regime, where the mean free path of phonons approaches device feature scale, ballistic phonon transport is the primary mechanism of heat transfer. Since the Fourier model cannot model this phenomenon accurately, other techniques such as the Gray phonon Boltzmann transport equation (BTE) under the relaxation time approximation can be used to model the nanometer device regions.

ISAC2 [9] combines the best features of the aforementioned models to accurately perform full-chip thermal analysis of billion transistor ICs. It uses a hybrid algorithm with lookup tables (to reduce computation time) and hierarchical spatial partitioning (to reduce memory usage). It can efficiently model heat transport across different scales, from nanoscale on-chip devices, through millimeter-scale silicon chip and centimeter-scale cooling package, to the ambient environment. We utilized this tool extensively in this work, and will describe its setup in Section IV.

D. Modeling Thermal Effects on Circuit Aging

NBTI is a key reliability issue for pMOS devices that is of immediate concern at the 45 nm node and below. NBTI manifests itself as an increase in V_{th} which results in a decrease in drain current and transconductance. At 32 nm, where high-k metal gate stacks and new materials like hafnium oxide are utilized to improve gate current density, the NBTI problem persists. Therefore, IC performance deteriorates over time (*i.e.*, circuit aging), and can lead to critical failure. Since V_{th} has a very strong correlation with operating temperature, the NBTI effect can be greatly reduced if the IC thermal profile can be improved.

A detailed model to predict the long term V_{th} degradation due to NBTI has been presented in [16]. A tight upper bound on ΔV_{th} can be calculated as follows:

$$\Delta V_{th} = \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1 - \beta_t^{\frac{1}{2n}}} \right)^{2n}, \tag{2}$$

TABLE I
NBTI PREDICTIVE MODEL & PARAMETERS

$$B_t = 1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C_k (1-\alpha) T_{clk}}}{2t_{ox} + \sqrt{C_k t}}$$

$$K_v = \left(\frac{q t_{ox}}{\epsilon_{ox}}\right)^3 K^2 C_{ox}(V_{gs} - V_{th})\sqrt{C_k} \exp^{\frac{2E_{ox}}{E_0}}$$

$$E_{ox} = \frac{V_{gs} - V_{th}}{t_{ox}} \qquad C_k = \frac{\exp^{\frac{-E_a}{k_B T}}}{T_0}$$

ξ_1	0.9	ξ_2	0.5
T_0 (s/nm^2)	10^{-8}	K (s$^{-0.25}$C$^{-0.5}$nm^{-2})	8×10^4
E_a (eV)	0.49	E_0 (V/nm)	0.335

where α and T_{clk} are the duty cycle and clock period, respectively, and $n = \frac{1}{6}$ for a H_2 diffusion based model [16]. K_v and B_t are determined by the equations and parameters shown in Table I. In these equations, q is the electron charge, k_B is the Boltzmann constant, t_{ox} and e_{ox} are the oxide thickness and permittivity, respectively, C_{ox} is the oxide capacitance per unit area, V_{gs} is the transistor gate to source voltage, T is the temperature, and t is the stress time.

Given a specific process technology, Eq. (2) can be simplified as a power law:

$$\Delta V_{th} = a\alpha^n t^n. \tag{3}$$

Now, the propagation gate delay degradation ΔD_{pgd} can be approximated as follows:

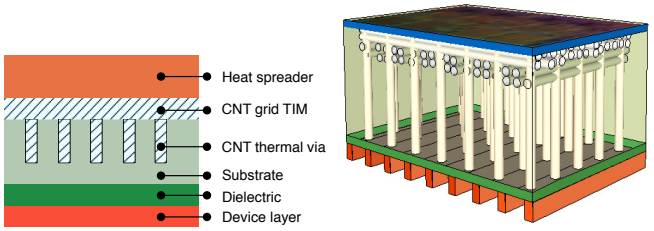
$$\Delta D_{pgd} = b\alpha^n t^n, \tag{4}$$

where a and b are constant parameters dependent upon technology and the gate type. It can be extracted using circuit simulation for a given gate subject to various operating conditions. The above model is used in this work to analyze the impact of temperature on aging.

III. PROPOSED CNT-BASED GRID THERMAL STRUCTURE

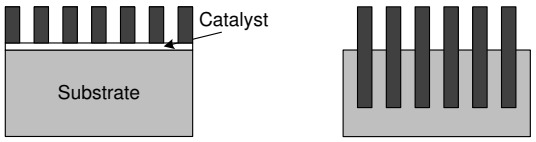
Fig. 4(a) shows the cross-sectional view of our proposed CNT-based grid thermal management structure. Fig. 4(b) illustrates the CNT grid layer in detail. It can be seen that our structure comprise of two parts. First, the thermal vias filled with CNT bundles transfer the heat from the silicon substrate to the CNT grid based TIM. Thermal vias are commonplace in 3D and printed-circuit board designs. Due to the increasingly severe requirement of heat dissipation in nanoscale SOI and CMOS circuits, we also employ the benefits of such vias in 2D design. The space in the unused substrate can be effectively utilized for planting the CNT thermal vias. The second part is the CNT grid layer which contains a mesh structure of CNT bundles (running horizontally and vertically). Heat can be conducted to the heat spreader through vertical CNT arrays, as well as flow from hotspots to the cooler regions through the horizontal CNT arrays. In this way, temperature is normalized across the chip, thereby reducing peak temperature. Furthermore, since the heat can now flow through the entire chip before being dissipated from the heat spreader, it implicitly increases the heat dissipation area and improves the dissipation efficiency. As will be demonstrated in Section IV, the proposed structure can effectively help dissipate the heat from the device layer and enhance overall chip reliability. It should be noted that most of the heat generated in the device layer is transferred to the substrate because the thermal conductivity from the device layer to the substrate is hundreds of times larger than the upper layer [17].

The feasibility of the proposed structure is enabled by the current state of CNT fabrication techniques. Our structure requires three key components: (a) CNT arrays running in the vertical and horizontal directions (Fig. 5(a)), (b) thermal vias filled with CNT bundles (Fig. 5(b)), and (c) the ability to interconnect the vertical and horizontal CNT arrays to form a mesh (Fig. 5(c)). The authors in [4]

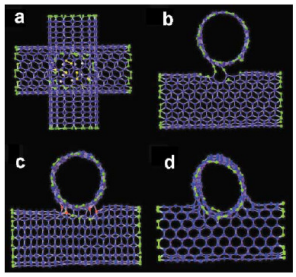


(a) Cross-sectional view. (b) 3D view of the CNT grid layer.

Fig. 4. Our proposed CNT-based thermal management structure containing the CNT grid layer and CNT thermal vias.



(a) Growing CNTs arrays on substrate. (b) Growing CNTs on bottom of vias.

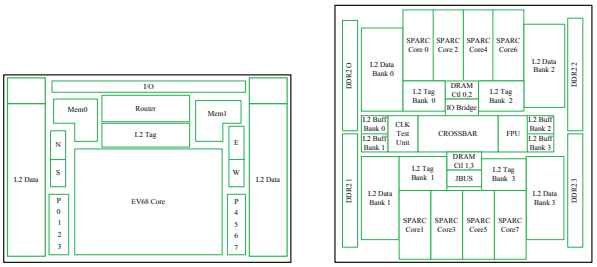


(c) Different patterns of molecular CNT junctions [6].

Fig. 5. Fabrication techniques for CNT arrays, vias, and pattern junctions.

have synthesized 15 μm thick CNT arrays with reported optimized thermal contact resistance as low as 7 mm^{2}K/W. In [18], a 13 μm thick CNT array on the surface of a free mating substrate exhibiting thermal contact resistance around 15-17 mm^{2}K/W was demonstrated. TSVs filled with CNT bundles were fabricated in [19] where a deep reactive ion etching (DRIE) process was used to etch deep vias in silicon. CNTs were then grown on a layer of catalyst at the bottom of the vias by thermal chemical vapor deposition (TCVD) as shown in Fig. 5(c). Hence, the CNT vertical arrays can be formed by the CNTs in the vias and the ones grown on the silicon. However, the horizontal CNT grid cannot be synthesized directly. We employ the approach of first growing CNT bundles, and then, deploying them on the surface to connect them together in a controlled manner. The junctions between the horizontal and horizontal/vertical bundles can be formed by the method presented in [6]. CNT junctions between two crossing CNTs can be formed by exposing them to an electron beam. This enables us to form molecular CNT junctions of different patters as shown in Fig. 5(c). With the method described above, our proposed thermal management structure can be built by first growing CNT vias and vertical CNT arrays, then horizontal CNT arrays, and then building the junctions between the vertical and horizontal arrays to create the entire CNT grid.

The structure presented in [7] uses CNTs only to transfer heat between hotspots and the cool regions of a chip. Our proposed structure is different because it specifically employs using CNTs as thermal vias and TIM *throughout* an IC. Furthermore, it is highly



(a) Alpha 21634. (b) OpenSparc T1.

Fig. 6. Floorplan of industrial processor benchmarks.

regular in design which facilities ease of fabrication. Furthermore, as we will see in the next section, it considerably improves the heat dissipation efficiency of the device layer, thereby reducing peak operating temperature and improving overall chip reliability.

IV. Simulation Results and Analysis

In order to investigate the benefits of our proposed CNT-based thermal management structure, we simulated the thermal profile of two industrial processors using ISAC2. The Alpha 21364 and OpenSparc T1 are single and eight core machines, respectively. Their floorplans are shown in Fig. 6. We studied the effect of using different TIM materials and structure on the thermal profile of these designs.

In order to simulate the designs in ISAC2, we created a power profile, floorplan and device descriptions, and a chip structure for the processors. The power profile contains the average power consumption under a typical workload. This was generated using McPAT. The floorplan file contains the coordinates and sizes of the main blocks shown in Fig. 6. The device file describes the MOS transistor characteristics. Finally, the chip file describes the material layers contained in the chip and IC packaging. For example, silicon for the device layer, and copper for the heat spreader. Our proposed thermal management structure was described in the chip file. Since the CNT grid structure enables the heat to flow in all directions along the CNTs, the grid can be described as a CNT layer between the device layer and the heat spreader. The CNT thermal vias were inserted in the silicon layer. Hence the original silicon layer is separated into two layers: the lower part is still silicon, while the upper part is a heterogeneous layer with CNT bundles distributed in silicon.

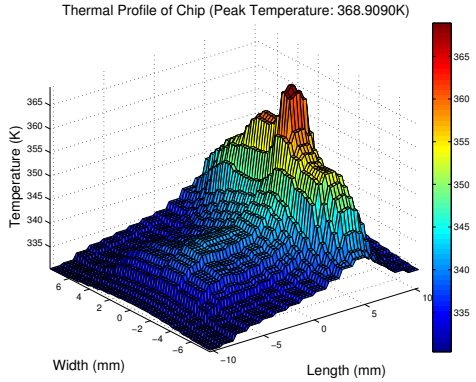
A. Reduction of Chip Peak Temperature

We evaluated the peak temperature reduction by applying our proposed thermal management structure. The baseline design to compare was assumed to be the case of using a silicone TIM between the substrate and the heat spreader (current practice). The thermal conductivity of silicone TIM is approximately 4 W/m·K [20]. The parameters for the CNT arrays in the grid in simulation were as shown in Table II. We note that the thermal conductivity of CNTs is set to that of MWCNTs, and is relatively conservative. The height of the CNT grid is assumed around 50 μm. Although the long synthesized CNTs can be several hundred micrometers in length [21], such long CNTs are prone to bend due to gravity. Finally, the heat capacity was computed based on the specific heat capacity reported in [22].

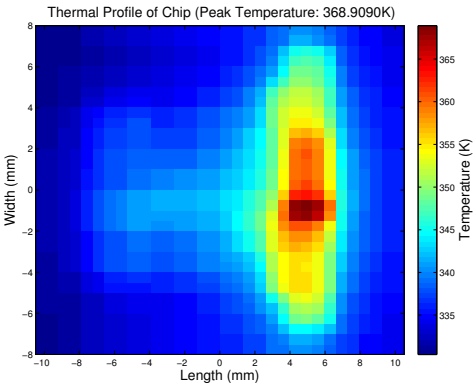
The peak operating temperature for the baseline design was found to be 415K (142°C) and 368K (95°C) for the Alpha 21634 and OpenSparc T1, respectively. We see that the peak temperature of OpenSparc T1 is significant lower than that of Alpha 21634. This is due to the effectiveness of migrating tasks from one core to multiple cores, and lowering the working frequency for the same

TABLE II
CNT Simulation Parameters

Parameter	Value
Height	50 μm
Thermal conductivity	3,000 W/m·K
Specific heat capacity	6 J/mol·K
Thermal via size	10 μm × 10 μm
Via pitch	50 μm



(a) 3D.



(b) 2D.

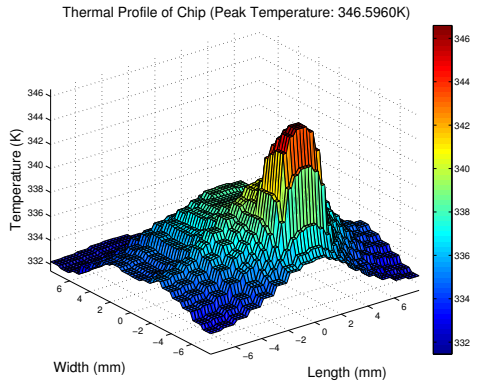
Fig. 7. Thermal profile of the Alpha 21364 using the CNT-based thermal management structure.

workload, which in turn, results in less power consumption and less heat dissipation. With the utilization of our proposed CNT-based thermal management structure, the peak temperature of both processors are significantly reduced. Their thermal profiles are are shown in Fig. 7 and Fig. 8, with the chip peak temperatures now being 369K (96°C) and 347K (73°C), respectively. This represents 32% and 23% reduction in the peak temperatures for the Alpha 21634 and OpenSparc T1, respectively. The hotspots appear in the floating point and clock tree units for the Alpha 21634 and OpenSparc T1, respectively. For IC packaging designers, this is a significant reduction in temperature. Thus, the effectiveness of our proposed structure is apparent due mainly to the CNTs' superior thermal conductivity.

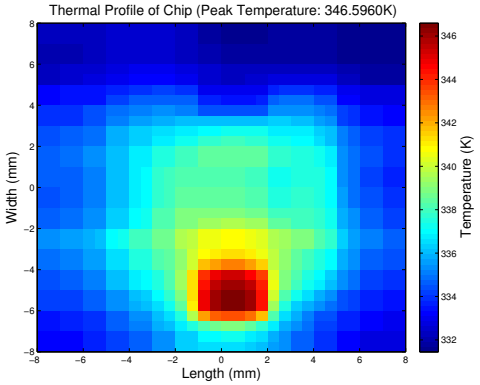
B. Effects of Parameter Variations

In this subsection, we further analyze the impact of parameter variations in the CNT grid and thermal vias on peak temperature reduction.

When only the CNT grid is employed, there is a high likelihood that the thermal conductivity of CNTs can be affected by mixed bundles comprising of both SWCNTs and MWCNTs. This is mainly

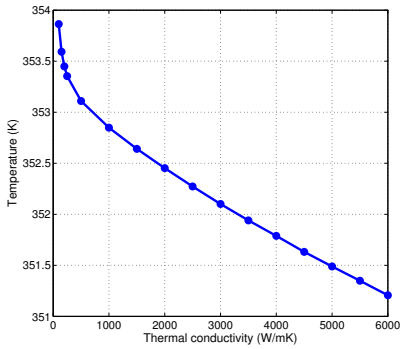


(a) 3D.

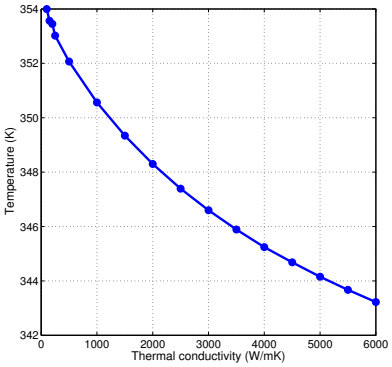


(b) 2D.

Fig. 8. Thermal profile of the OpenSparc T1 using the CNT-based thermal management structure.



(a) Without thermal vias.



(b) With thermal vias.

Fig. 9. Plots for chip peak temperature as a function of CNT thermal conductivity.

due to the current state of CNT fabrication. Consequently, we evaluated how such a change will affect chip peak temperature reduction. Fig. 9 presents the trend of peak temperature as a function of CNT thermal conductivity (varying from 100 to 6,000 W/m·K). It can be seen that the peak temperature initially drops exponentially, then decreases almost linearly. Furthermore, it drops only 1K as the thermal conductivity increases from 3,000 to 6,000 W/m·K illustrated in Fig. 9(a). This is because the heat transfer capacity of the CNT grid has reached a saturation point due to the high CNT thermal conductivity. This can be confirmed by Fig. 10 which shows the heat flow in the CNT grid. Furthermore, thermal vias have not been utilized. In Fig. 9(b), where thermal vias are used, we can see steady decrease in peak temperature (approximately 4K as the thermal conductivity increases to 6,000 W/m·K) as there are direct paths from the device layer to the heat spreader to remove excess heat.

Next, we investigated the impact of the optimal thermal via pitch on the chip thermal profile. It is fairly obvious that as the number of thermal vias increase, the chip peak temperature will decrease. However, the penalty will be a rapid increase in via area overhead as these structures have to be drilled through the substrate. Fig. 11 shows the impact of thermal via pitch on peak temperature and area overhead. We observe that when the pitch exceeds 200 μm, the thermal vias will be too sparse to be effective. Designers may choose an acceptable overhead to obtain the desired temperature reduction based on these results. Note that we are assuming that thermal vias are inserted uniformly across the substrate.

We also investigated non-uniform via planning. In such a scenario,

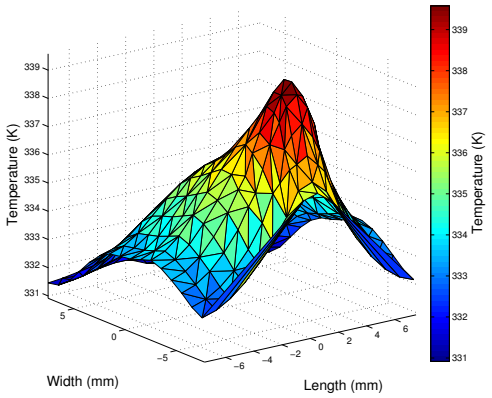


Fig. 10. Thermal profile of the CNT grid layer.

more vias are placed in the hotspots. However, we found that the results were relatively worse than using uniform planning. This is because even though more heat can be conducted out of a hotspot due to a large number of thermal vias, more vias are also needed to transfer the heat to the cooler regions. If the thermal via number is insufficient in the cooler regions, heat will still be congested in the CNT grid localized around the hotspot. Through simulation, it was also found that the thermal via size greatly affects the temperature reduction. Naturally, the larger the via size, the higher the temperature reduction. CNT bundles with diameters ranging from 20-50 μm

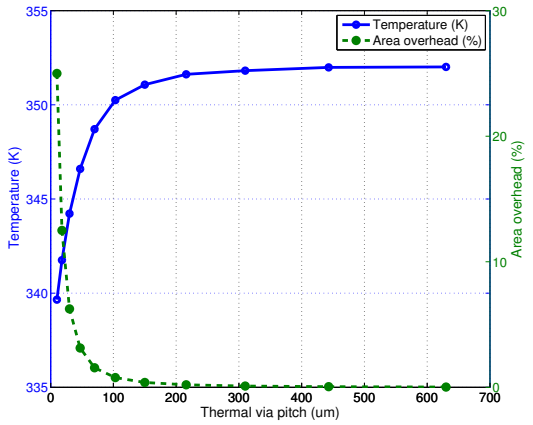


Fig. 11. The impact of thermal via pitch on peak temperature and area overhead.

have been reported in [19]. Here, we used a 10 μm diameter foreseeing advancements in fabrication techniques and reducing the area overhead.

It should be mentioned that in the above discussion, we used the ideal thermal conductivity of CNT bundles. However, due to non-ideal contacts between CNTs, and CNT/substrate, the thermal conductivity of CNT can only be in the range of hundreds W/m·K. For example, the thermal conductivity of a MWCNT array is reported to be 250 W/m·K [2]. Hence, here we also consider the non-ideal case of using real practical parameters for experiments. We repeated the simulations using this parameter value, and found that even with this, the peak temperature of the OpenSparc T1 was reduced by 15K (15°C) to around 353K. This represents a 16% temperature reduction. Similar results were obtained for the Alpha 21634. Thus, we can see that the effectiveness of the proposed structure remains given even the current CNT fabrication status.

C. NBTI Improvement

It is well known that temperature plays an important role in the NBTI effect. A processor module with peak temperature needs attention since its circuitry can degrade more rapidly than other components. It is almost always the critical component for reliability failure. In order to calculate the impact of peak temperature reduction on the processor reliability improvement, a temperature-aware NBTI timing analysis algorithm was used [23]. The foundation of this algorithm is based on Table I. It takes circuit netlist, a set of input vectors, signal probability, *etc* as inputs. Then, it evaluates the delay degradation of each gate/blocks, and propagates the delay information to the next stage. Finally the delay degradation of the critical path is accumulated and calculated under a given process technology and NBTI stress time parameters

In this work, we assumed a 10 year working life. The process technology (65 nm) and working parameters for the Alpha 21364 and the OpenSparc T1 were taken from [11]. As temperature has a big impact on circuit delay degradation, it was expected that the delay degradation will be reduced as the chip peak is reduced. Running the algorithm on both processors revealed that the delay degradation for the hottest units was reduced by 48% and 22% for the Alpha 21364 and the OpenSparc T1, respectively. This reduction can possibly help in achieving NBTI-aware timing closure more quickly and easily in IC design.

V. Conclusions

In this paper, we have presented an efficient thermal management structure using a CNT-based grid and CNT thermal vias. In the proposed method, heat can be efficiently conducted out of the silicon substrate, and dissipated through the heat spreader as well as directed to the cooler areas of the chip. Simulation results on two industrial processor benchmarks showed significant temperature reduction using the proposed structure, which in turn, results in improvement on circuit aging (reliability).

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