Power Management Trends in Portable Consumer Applications

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***Abstract*—Mobile consumer electronics continue to converge, in terms of functionality and feature sets, bringing many challenges to the circuits required to power these applications. This paper outlines some of the technology available to address these challenges.**

I. Introduction

Mobile consumer electronics continue to converge in terms of functionality. For example, mobile phones no longer just provide the user with the ability to make a phone call: the devices are now capable of providing high-speed internet access, high-definition video and advanced gaming applications. This brings many challenges to the circuits required to power these consumer devices. Size restrictions, power limitations and thermal constraints mean that the power management devices have to become smarter to ensure that devices are useable from a consumer perspective. This paper outlines the basics of power management and shows how the next generation of power management integrated circuits with emerging technology is addressing these challenges.

II. OVERVIEW

In the past, it was fairly easy to categorize consumer electronics: a handset was used to make phone calls; a music player to listen to music; a DVD player to watch films; and a computer to access the Internet. However, consumer electronics have progressed and it is no longer expected to have separate consumer gadgets to access different applications. Each device has to service multiple applications and include differentiating functionality. Each consumer market segment, and its associated technology, is also converging and will continue to do so.

There will of course be exceptions as new technology is introduced, but consumer expectation is that handsets must now connect to the internet, play advanced games, make video calls and play music. As well as integrating more applications, consumers also expect faster response times, longer battery life, brighter displays with high definition (HD), smarter devices enabling multi-tasking, increased HD content such as 3D videos and 3D displays, social networking and the ability to handle future applications that develop over the next few years.

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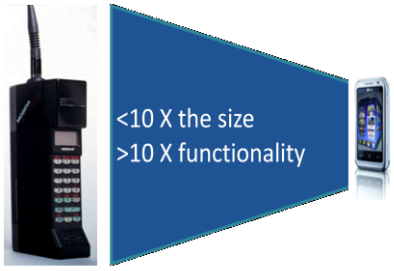

Figure 1. In two decades the mobile phone has transcended several application areas, whilst reducing form factor.

These consumer requirements drive two main areas of development; firstly the need for increased processing capabilities for these consumer devices; and secondly, a reduction in the size of the components that go into these consumer devices.

III. Powering Mobile Consumer Electronics

With the increased functionality in mobile electronics comes the requirement for more power and more power rails. There is an increase in power consumption, since there are more circuits (sub-systems) operating resulting in an increase in the requirement of the number of voltage regulators.

The battery voltage has to be converted to a level which is usable by each of the sub-systems, and each sub-system typically requires a specific voltage. There are effectively two ways of converting the battery voltage to the require voltage: Low-Drop-Out (LDO) regulators or DC-DC converters. Each has its own advantages and disadvantages and these are explained in the next sections.

IV. Low Drop-Out (LDO) Regulators

LDOs are Low Drop-Out regulators which provide a low cost regulated output. The major component of an LDO is a MOSFET which is used as a variable resistor to “drop” the voltage across it in order to provide the required output voltage. The main disadvantage with LDOs is that the power loss will be high, and thus efficiency is low if the difference between the input and output voltage is large.

Therefore, when using an LDO it is desirable to keep the input voltage as close to the output voltage as possible, to minimise power loss. The power dissipation in a typical LDO is shown in Figure 2 and Equation (1).

Figure 2. Typical LDO

$$P_{loss}=(V_{in}-V_{out})\times I_{out} \quad (1)$$

V. Switch Mode Power Supplies (SMPS)

The most common form of SMPS or DC-DC converters are buck (step-down) and boost (step-up) regulators. It should be noted that there are other types of converters, such as buck-boost and charge pump regulators but their analysis is outside the scope of this paper.

A. Buck (step-down) converters

The buck (or step down) converter, shown in Figure 3, is used to convert a positive DC voltage to a lower positive DC voltage. It can be a bi-directional converter, but for simplicity we only consider the power flow from the higher voltage to the lower voltage.

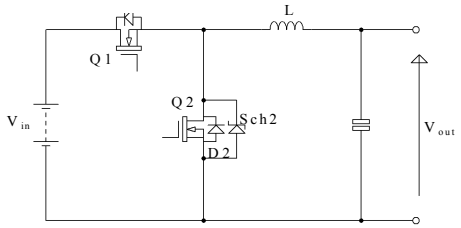

Figure 3. Basic circuit schematic for a buck converter. (Q2 is the MOSFET channel, D2 is the body diode of the MOSFET, and Sch2 is an external Schottky diode)

The input voltage has to be greater than the output voltage for energy flow from the input through to the output. Q1 is turned on and since there is a positive voltage difference between V_{in} and V_{out} then there is a current build up in the inductor according to:

$$\frac{di_L}{dt}=\frac{V_{in}-V_{out}}{L} \quad (2)$$

Once Q1 is turned off (Figure 3), the current flowing through the inductor cannot instantaneously be reduced to zero and as such the current needs a freewheel path, which will be Q2, D2, or Sch2, depending on the circuit topology. The current decays through the freewheel path according to:

$$\frac{di_L}{dt}=\frac{V_{out}}{L} \quad (3)$$

B. Power Losses in a Buck Converter

The power loss of the MOSFET in the buck converter can be split into four categories, viz. switching losses, on-state losses, off-state losses and gate losses. However, the leakage currents in power semiconductor devices during the off state are several orders of magnitude smaller than the rated current and hence can be assumed to be negligible

C. Conduction losses in a Buck Converter

The generic conduction losses (P_{con}) can be equated to the product of the saturation voltage of the device ($V_{ds(sat)}$) under consideration, the current (I) through it and the time the device is on (t_{on}).

$$P_{con}=V_{ds(sat)}It_{on} \quad (4)$$

Typical low power consumer buck converters use MOSFETs as the power switches and, as such, the conduction loss can be shown to be:

$$P_{con}=R_{ds(on)}I^2\delta \quad (5)$$

where δ is the duty cycle

D. Conduction losses with synchronous rectification

With synchronous rectification there will be a time when either the body drain diode, or external Schottky diode will be in conduction. This period can be approximated to the deadtime ($t_{deadtime}$).The conduction losses for the synchronous MOSFET under these conductions can be related to:

$$P_{con}=R_{ds(on)}I^2(1-\delta-t_{deadtime}f_{sw}) \quad (6)$$

and the diode losses (P_D) can be equated to:

$$P_D=V_{DO}+r_{DO}I_o(t_{deadtime}f_{sw}) \quad (7)$$

E. Switching losses in a buck converter

Switching losses are difficult to accurately predict and model since the parameters which make up switching transients vary greatly not only with temperature, but also with parasitic elements in the circuit. Also the gate drive capability, gate drive parasitics and the operating conditions such as current and voltage influence the switching times, which are greatly dependent on individual circuit designs. Therefore, the following expressions, for switching losses should be used to obtain an approximation of the performance of the device and should not be used as a definitive model. The turn-on power (P_{on}) loss will be:

$$P_{on}=\frac{1}{2}V_{in}t_rI_of_s \quad (8)$$

Whereas the turn-off losses (P_{off}) will be

$$P_{off} = \frac{1}{2} V_{in} I_o t_f f_s \quad (8)$$

There are other losses which occur in the Buck converters, although the derivation of these equations are beyond the scope of this paper, a summary are shown in Table 1.

	Buck	Synchronous Buck
Q1	$P_{con} = R_{ds(on)} I_o^2 \delta$ $P_{sw} = \frac{1}{2} V_{in} I_o (t_f + t_r) f_s$ $P_{gate} = 2 Q_g V_g f_{sw}$	$P_{con} = R_{ds(on)} I_o^2 \delta$ $P_{sw} = \frac{1}{2} V_{in} I_o (t_f + t_r) f_s$ $P_{gate} = 2 Q_g V_g f_{sw}$
Q2	-	$P_{con} = R_{ds(on)} I_o^2 (1 - \delta - \delta_{bbm})$ $P_{sw} \approx 0 \quad P_{gate} = 2 Q_g V_g f_{sw}$
D2 or Sch2	$P_{con} = V_{sat} I_o (1 - \delta)$	$P_{con} = V_{sat} I_o \delta_{bbm}$
Q1 &(D2 or Sch2)	$P_{rr} = V_{in} t_{rr} \left(\frac{I_{rr}}{2} + I_o \right) f_s$	$P_{rr} = V_{in} t_{rr} \left(\frac{I_{rr}}{2} + I_o \right) f_s$

Table 1. Summary of generic loss equations for a buck converter.

F. Boost (step-up) converters

The boost (or step up) converter shown in Figure 11, is used to convert a positive DC voltage to a higher positive DC voltage. As with the buck converter, it can have a bi-directional power flow, but for simplicity we will only consider the power flow from the lower voltage to the higher voltage.

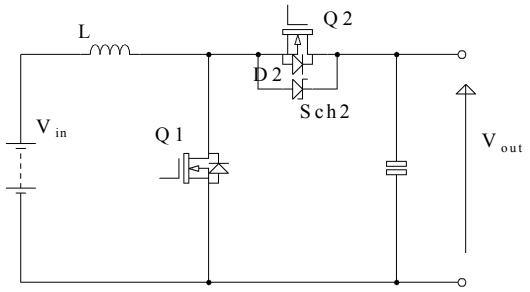

Figure 4. Basic circuit schematic for a boost converter.

The input voltage has to be less than the output voltage otherwise the freewheel diode will be forward biased and uncontrolled power will flow.

Q1 is turned on (Figure 4.) which builds up the current in the inductor. During this period the output capacitor will have to support the load current. Once Q1 is turned off the current flowing through the inductor is passed to the freewheel component, this being either the body drain diode, the Schottky diode or the synchronous MOSFET depending on the control strategy and the topology implemented.

G. Losses in a Boost Converter

The simple loss model for a boost converter is given in Table 2. These equations are similar to those derived for the buck converter. However, in this case the inductor current is not the same as the load current and as such the rms current through the controlling MOSFET Q1 will be:

$$I_{rms} = \frac{I_o}{(1 - \delta)} \quad (9)$$

	Boost	Synchronous Boost
Q1	$P_{con} = R_{ds(on)} \frac{I_0^2 \delta}{(1 - \delta)^2}$ $P_{sw} = \frac{1}{2} V_{in} \frac{I_0}{(1 - \delta)} (t_f + t_r) f_s$ $P_{gate} = 2 Q_g V_g f_{sw}$	$P_{con} = R_{ds(on)} \frac{I_0^2 \delta}{(1 - \delta)^2}$ $P_{sw} = \frac{1}{2} V_{in} \frac{I_0}{(1 - \delta)} (t_f + t_r) f_s$ $P_{gate} = 2 Q_g V_g f_{sw}$
Q2	-	$P_{con} = R_{ds(on)} \frac{I_o^2}{(1 - \delta)^2} (1 - \delta - \delta_{bbm})$ $P_{sw} \approx 0 \quad P_{gate} = 2 Q_g V_g f_{sw}$
D2	$P_{con} = V_{sat} I_o$	$P_{con} = V_{dsat} \frac{I_o}{(1 - \delta)} \delta_{bbm}$
Q1 & D2	$P_{rr} = V_{in} t_{rr} \left(\frac{I_{rr}}{2} + \frac{I_o}{(1 - \delta)} \right) f_s$	$P_{rr} = V_{in} t_{rr} \left(\frac{I_{rr}}{2} + \frac{I_o}{(1 - \delta)} \right) f_s$

Table 2. Summary of the generic loss equations for a boost converter

VI. MAXIMISING EFFICIENCY IN POWER MANAGEMENT

The power loss in the converters and regulators described above have a direct impact on the battery life of the consumer product. It is no longer acceptable just to have discrete regulators powering multiple sub-systems in an application, as this will not optimize the performance and battery life of the portable device. Therefore Power Management Integrated Circuits (PMIC), which are described in the next section, incorporate many DC-DC converters and many LDOs. In conjunction with this, the PMICs generally have some intelligence and the ability to interact with the processors that they are powering. This allows for optimisation of the power system and results in increased battery life. An example of a typical PMIC is shown in Figure 5. This includes 3 DC-DC synchronous buck converters, 1 DC-DC boost converter, 13 LDOs, a one-time programmable memory, battery charger, power path management, general purpose input-output circuits, an auxiliary analogue to digital converter (ADC), frequency locked-loop and LED drives. The device is designed to power portable consumer applications which typically include an ARM-based processor.

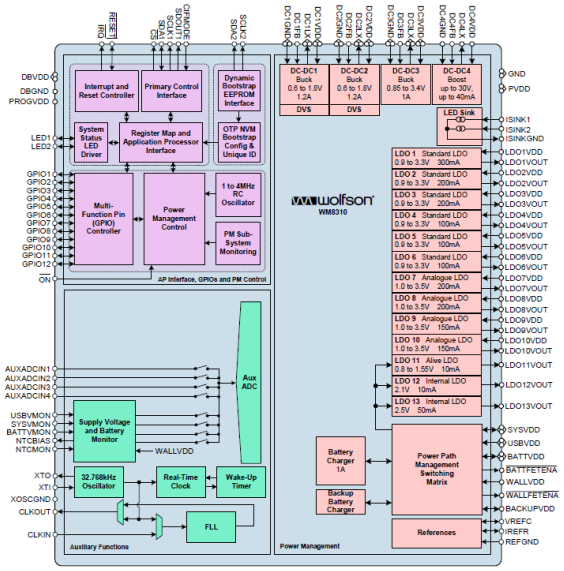

Figure 5.Typical PMIC – WM8310.

VII. Power Management Integrated Circuits

With the increased power demands of mobile consumer electronics having all the power supplies as individual circuits would not result in the most optimum solution. The Power Management Integrated Circuit (PMIC) or Power Management Unit (PMU) combines several DC-DC converters and LDO regulators in one Integrated Circuit. By doing this, it is possible to optimise the system performance.

The main objective for the PMIC is to increase battery life. Typical processor core currents for small portable consumer applications with ARM processors are now approaching 2A and above. With a 1000mAHr battery, a processor running at 2A continuously would potentially discharge this battery (to a usable level) in an hour. Therefore, this would make the consumer device totally unusable, so the processor must limit how long it draws the full current. This is typically achieved by switching the processor to low power modes, which can mean the processor voltage can be reduced to as low as 0.7V.

There are two key elements to supply the voltages in low power modes. The first is the DC-DC supplying the processor switch between high power voltages (say 1.2V) and low power voltages (say 0.7V). A discrete regulator typically does not have any interface to enable it to be controlled via a software interface, such as I2C. In this instance, some form of external discrete circuit would be required to achieve this. This conflicts with the requirements of saving space and cost.

A. Dynamic Voltage Scaling (DVS)

An integrated PMIC typically has some form of software interface to change the output voltage of the DC-DCs, but this alone does not mean that it will meet the requirements of the processor. In order to do this and to change the voltage in a PMIC, a dynamic voltage scaling (DVS) system is usually employed. These typically use one register write or a hardware pin to change voltages and allow an element of scalability. For instance, the WM831x family of PMICs employs 4 different ramp rates during DVS (12.5mV/32µs; 12.5mV/16µs, 12.5mV/8µs and immediate). This ensures that the designer can determine which slew rate is best to minimise the time changing modes, and ensure that there are no significant voltage overshoots due to parasitic elements in the design, which would cause damage to the processor or cause the processor to under-voltage. Figure 2 shows the WM8312 switching between low power mode (0.6V) and high power mode (1.4V).

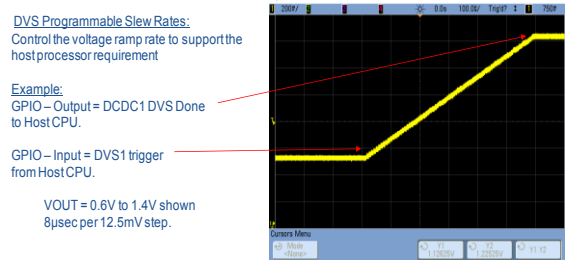

Figure 4. Example of Programmable Dynamic Voltage Scaling using the WM8312

B. Current Mode Control

Low power processor modes mean low DC-DC output voltages, however this is not straightforward to achieve. Typically, the majority of control schemes employ ***Peak Current Mode Control*** to regulate the output voltage. However, there are limitations on the lowest output voltages achievable with this control scheme, since the minimum duty cycle is limited by a minimum on-time of the high-side switch in the DC-DC (shown in Figure 3 and Equation 1). With high input voltages and low output voltages a new control scheme is required to ensure the processor can operate at the lowest voltage node possible.

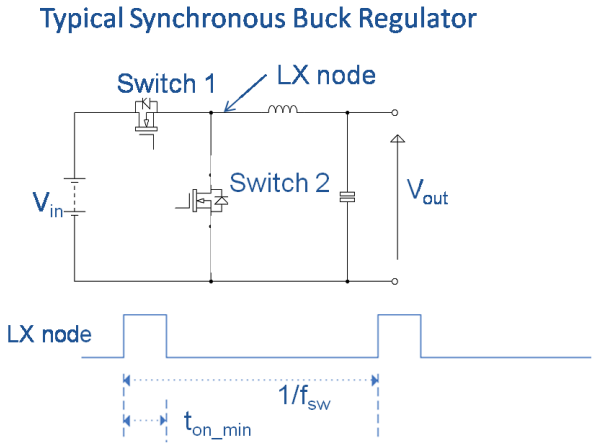

Figure 4. Typical DC-DC showing minimum duty cycle with Peak Current Mode Control.

$$V_{out\_min}=f_{sw}\times t_{on\_min}\times V_{in} \quad (3)$$

One such control scheme is ***Valley Current Mode Control*** where the regulation is controlled with the low-side switch (switch2). This results in a limitation in the maximum output voltage, but does not result in any limitation in the minimum voltage, as shown in Figure 4 and Equation 2. This means that even with multiple Li-Ion battery cells in series it is possible to achieve the low voltage requirements of the processors.

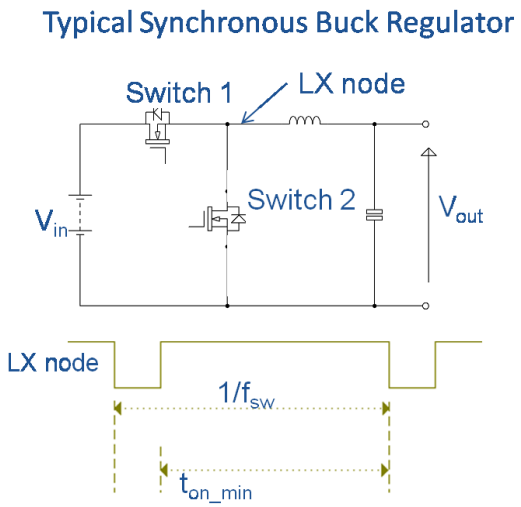

Figure 5. Typical DC-DC showing maximum duty cycle with Valley Current Mode Control.

$$V_{out\_max}=V_{in}(1-f_{sw}\times t_{on\_min}) \quad (4)$$

In the past, the transient response of a DC-DC converter was critical to make sure there were no over voltage transients seen by the load. This could cause catastrophic failure of the load and was therefore critical in the design of DC-DCs. However, it has now become vital to ensure that during the transition from low power mode to high power mode, the voltage must not drop to such an extent that the processor under voltages. The minimum voltage supplied to the processor must be such that any voltage disturbance must not fall below the minimum voltage required by the processor, causing it to shut down. Any margin overhead over the minimum voltage is directly related to an increase in power dissipation, due to the power dissipated being directly related to the square of the supply voltage. For instance, with Wolfson's BuckWise™ technology, the voltage disturbance for a 1.2A load is 33mV (Figure 5). When compared to a industry standard of 63mV, this equates to a possible 10% increase in battery life.

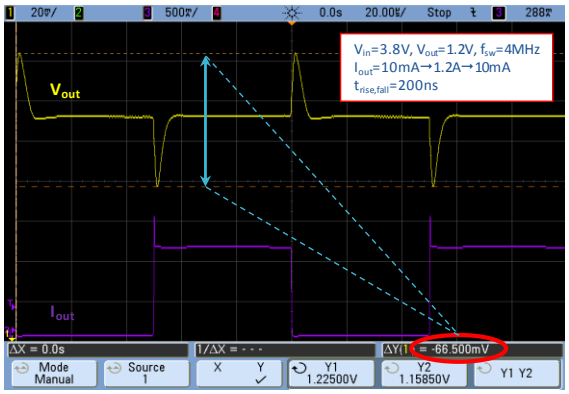

Figure 6. Transient performance of the Valley Mode Current Control WM8312 DC-DC

VIII. CONCLUSION

To maintain form factor and preserve the enhanced user experience of multi-functional portable consumer electronics, the power management has to control the total system power requirements in order to maximise the battery life. There are several factors which can be implemented to improve the efficiency. If, for instance, the application is put into standby mode, then the application is not using the processor fully and the processor can be put into standby mode. If, for example, the core voltage is reduced from 1.2V to 0.9V then with everything else being equal the consumer device immediately saves over 44% of processor power losses. The power dissipated by the processer is a factor of the voltage squared, so reducing the voltage supply instantly saves power. The more frequently the processor can transfer to a lower voltage (i.e. a low power mode) the more power can be saved. So the quicker the DC-DC can facilitate this the more frequently the device can go into low power mode. The converse of this operation is transferring from low power mode to high power mode. If the DC-DC cannot switch voltages quickly, then the user may experience lag in switching modes, DVS is required to make sure the device switches between power modes with no degradation of the user experience.

Power is one of the key elements of the system to maximise user experience. Individual power devices can no longer operate in isolation; they have to become part of the total system solution. Without an optimum power solution, the user experience can be greatly degraded, and in the worst case scenario the devices can fail due to extreme heat caused by power dissipation. The technology associated with PMICs will continue to develop and efficiency improvements will continue, however it is the improvements in how the power is managed that will make the difference, and the PMICs that incorporate these technologies are the ones that will be successful.