Systematic Design of a Programmable Low-Noise CMOS Neural Interface for Cell Activity Recording

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***Abstract*—The increasing electrode density in multielectrode arrays and the use of new materials for electrode fabrication are motivating the migration from passive to active neuroprobes. Numerous circuit design challenges for the implementation of optimal integrated neural recording systems are still present and need to be addressed. In this paper we present the systematic design of a programmable low-noise multi-channel neural interface that can be used for the recording of neural activity in *in vitro* and *in vivo* experiments. The design methodology includes modeling and simulation of important parameters, allowing the definition, optimization and testing of the architecture and the circuit blocks. In the proposed architecture, individual channel programmability is provided in order to address different neural signals and electrode characteristics. A 16-channel fully-differential architecture is fabricated in a 0.35 µm CMOS technology, with a die size of 5.6 mm × 4.5 mm. Gains (40-75.6 dB) and band-pass filter cut-off frequencies (1-6000 Hz) can be digitally programmed using 7 bits per channel and a serial interface. The circuit consumes a maximum of 1.8 mA from a 3.3 V supply and the measured input-referred noise is between 2.3 and 2.9 μV_{rms} for the different configurations. We successfully performed simultaneous recordings of action potential signals, using different electrode characteristics in *in vitro* experiments.**

I. INTRODUCTION

In order to study the function of the nervous system at the circuit level as well as the signal processing performed in complex neural networks, implantable electrodes and electronic systems are being used to monitor the neural signals. Therefore, microfabricated, multi-site neuroprobes are being designed in advanced silicon technologies, customized to the anatomy and morphology of the recording site.

The migration from passive to active probes offers numerous advantages, including the proximity between electrode and circuitry, full implantability, reduction of infection and tissue damage, long-duration experiments and treatments, and patient's comfort. Also, the density of microelectrode arrays is increasing fast, allowing selective recording from small groups of neurons [1]. This evolution in the neural recording interfaces is posing several important circuit design challenges, as regards miniaturization, noise and power dissipation reduction, programmability, and handling and transmission of large quantities of data.

Extracellular recordings, measured several micrometers from the cell, can capture small potential traces with amplitudes in the order of 100 µV, which are called action potentials (APs). Neural APs are biphasic in nature and usually have durations of 0.3-1 ms [2]. The recorded trace also contains low-frequency (< 200 Hz) oscillations resulting from the combined activity of many neurons in the surrounding of the electrode [3]. These oscillations are called local field potentials (LFPs) and they represent another source of information. Fig. 1 shows the approximate frequency and amplitude distribution of both APs and LFPs. An important challenge in the design of neural interfaces is the successful conditioning of both AP and LFP signals with optimized parameters according to their nature. As these two kinds of signals have different amplitude ranges and bandwidths, they will also require different gains, filters and even electrodes in order to be measured.

Existing neural recording architectures include some or all of the following stages: pre-amplification, filtering, analog multiplexing, additional amplification, buffering, digitalization and wired/wireless data transmission/storage [4]-[9]. More sophisticated features such as spike detection circuits [8], [9], or LFP measurement circuits [3] are also included in some designs in order to obtain data reduction in multielectrode applications. Discrete [4], [5], hybrid [6] and custom integrated [7]-[9] implementations in the last three decades have attempted to address problems such as connectivity, noise/interference, size, power consumption and data transmission. However, with the increasing density of multielectrode arrays, the need for fully implantable recording devices and the use of different electrode materials, sizes and shapes, many of the these problems still remain.

This paper describes the different design aspects of a low-noise integrated interface for neural recording. We propose a 16-channel architecture with individual channel programmability, so that different kinds of signals (APs and LFPs) and electrodes can be addressed at the same time. The programmable settings include gain, high-pass and low-pass

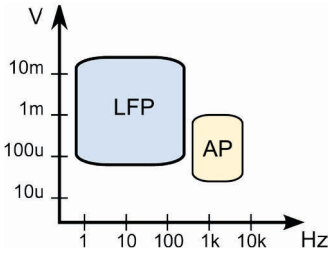

Figure 1. Frequency and amplitude distributions of LFP and AP signals.

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filter frequencies. We demonstrate successful functionality in *in vitro* experiments with different electrode characteristics and signals.

II. Modelling of the Neural Interface Architecture

For the design of efficient neural interfaces, numerous characteristics from the neuroprobes, the neural signals, the electrode-tissue interface and the test conditions have to be taken into account. All these characteristics allow the extraction of the design specifications required for any block inside the circuit. In this section we discuss some important specifications, including input impedance, overall gain, noise and dynamic performance of the output stage.

A. Input Impedance Model

In order to determine the input impedance required for the recording system, the impedance of the electrode-tissue interface seen by the input stage has to be estimated by measurement or modeling. Then, after knowing the maximum impedance within the required frequency range, we can set the input impedance of the system to be high enough (i.e. > 10 times higher) to limit signal attenuation.

Accurate modeling of neurons, electrodes and the electro-tissue interface represents one of the most challenging aspects in the study of neural signals. These models are of utmost importance in the design of electronic neural interfaces as they can provide a good characterization of the input signal conditions (impedances, offsets, time- and frequency-variable parameters, among others). For the design described in this paper, we have considered the characteristics of two different recording devices: a commercial MEA system from Multi Channel Systems [10] with titanium nitride (TiN) electrodes of 10, 20 and 30 µm diameter, and a micro-fabricated probe [11] with platinum (Pt) electrodes of 50 µm diameter. Fig. 2

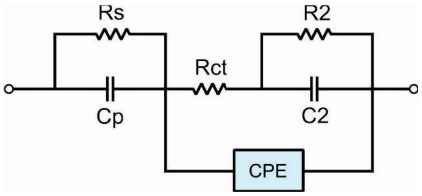


Figure 2. Electrode-electrolyte interface for a 50 µm Pt electrode, where Rs = 4690 +/- 57 kΩ, Cp = 135 +/-4 pF, Rct = 215 +/- 23 kΩ, R2 = 2.7 +/- 0.2 GΩ, C2 = 78 +/- 4 pF and Z_{CPE} =(1/Y) $(j\omega)^{-\alpha}$, with Y = 1.1 +/- 0.006 nF and α = 0.93 +/- 0.0006.

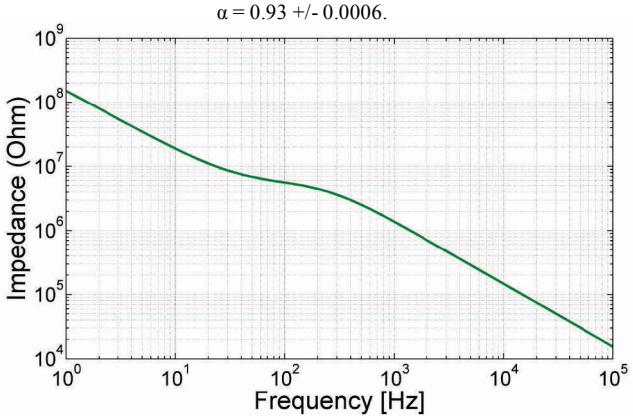


Figure 3. Absolute impedance of a 50 µm Pt electrode (model in Fig.2).

shows a 50 µm Pt electrode model proposed by Eberle *et al*. [12]. The frequency distribution of the total impedance for this model is shown in Fig. 3. From this distribution we can extract the expected impedance range at the input of the system, which is between 100 kΩ and 20 MΩ for the targeted frequency range of 10-10000 Hz. For the commercial MEA, impedances of 250-400 kΩ are reported for a 10 µm TiN electrode [10].

Using these parameters as the input conditions of our recording system, the specification for the input impedance is set to be higher than 200 M Ω.

B. Noise Model

As neural recording involves the measurements of very small voltages, noise can become a limiting factor in the system performance. The total noise at the input of the neural interface is composed of the noise introduced by the electrodes and the input-referred noise of the electronic circuitry. The former is determined by the material of the electrodes, the impedance and other characteristics of the electrode-electrolyte/tissue interface. The latter mainly includes thermal and flicker noise of every component in the circuit. The noise of the electronic system must be kept lower than the electrode noise so that it has a minor contribution to the overall noise.

In a multi-stage system, the noise of the first stage (input) has the largest effect on the circuit noise due to the amplification of the following stages. Therefore, the design of the input stage becomes critical and involves numerous trade-offs with other important specifications such as power consumption and area. If the input stage is an instrumentation amplifier, the ideal input-referred noise, assuming transistors in the subthreshold region and a first-order frequency response, can be expressed as [13]

$$V_{ni,rms} = \sqrt{\frac{4kT \cdot U_T \cdot \pi}{\kappa^2 I_{tot}} \cdot BW}\ , \qquad (1)$$

where k is Boltzmann's constant, T is the absolute temperature, U_T is the thermal voltage, κ is the subthreshold gate coupling coefficient, I_{tot} is total supply current and BW is the -3 dB bandwidth of the amplifier. As can be seen, for a given bandwidth the noise is inversely proportional to the square root of the supply current, that is, there exists a trade-off between noise and power consumption.

When measuring the noise of a 50 µm Pt electrode with a commercial recording system (LeadPoint from Medtronic) [11], we can find typical noise levels of around 30 $\mu V_{p\text{-}p}$, coming mainly from the electrode noise as the electronic system has only a small contribution (maximum 10 $\mu V_{p\text{-}p}$).

An important figure of merit in the design of biopotential amplifiers is the noise-efficiency factor (NEF) [14], which scales the noise, power and bandwidth of a design against a reference BJT amplifier. The NEF is calculated as

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{tot}}{4kT \cdot U_T \cdot \pi \cdot BW}}\ . \qquad (2)$$

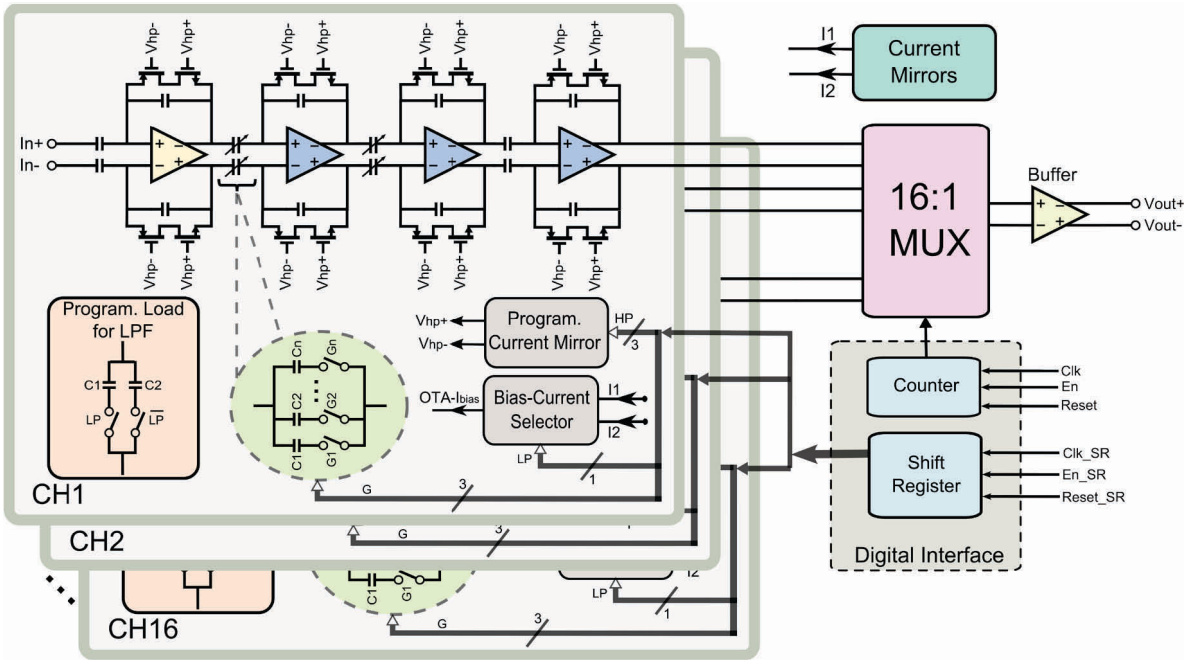


Figure 4. Architecture of the 16-channel neural recording system.

C. *Overall Gain Model*

The overall gain of the recording chain will depend on the range of the input signal, the input noise and the resolution at which the output signal must be digitized. In this design we have considered an input rage of 60-1000 $\mu V_{p\text{-}p}$ for AP signals and 1-20 $mV_{p\text{-}p}$ for LFP signals, and a total input noise of 30 $\mu V_{p\text{-}p}$. If we assume a 10-bit analog-to-digital converter (ADC) at the system output with a full-scale input swing of 3 $V_{p\text{-}p}$ (i.e. 2.93 mV resolution), then we can calculate the required gain as follows: to accurately resolve the minimum AP signal amplitude of 60 $\mu V_{p\text{-}p}$ with a minimum of 7 bits (at least 10% of the full scale), the gain is calculated as

$$G = \frac{2^7 \times \text{Resolution}}{Min.\ AP} \approx 6000\ \text{V/V}. \qquad (3)$$

Also, to resolve the maximum LFP amplitude signal of 20 mV with 10 bits (the maximum possible resolution), the gain is calculated as

$$G = \frac{2^{10} \times \text{Resolution}}{Max.\ LFP} = 150\ \text{V/V}. \qquad (4)$$

Thus, the total system gain must be within the range 100-6000 V/V.

D. *Power*

The power constraints of the design are mainly determined by the kind of application and measurement conditions. For fully-implantable devices, the total power dissipation is limited to around 10mW to avoid heating of the surrounding tissue [9]. In wireless chronic applications, the limits are determined by the duration of the experiments and the battery capacity. In this design, the power consumption specification was set to 5 mW, so that future circuit blocks (e.g. ADC or wireless) can be added without exceeding the limit of 10 mW.

E. *Output Stage Model*

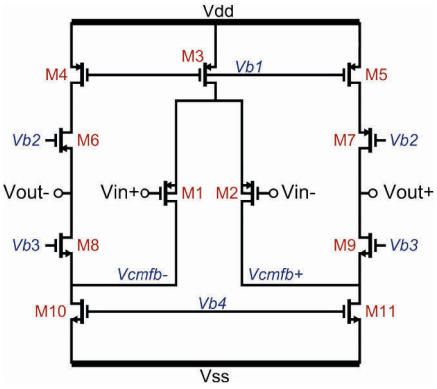
For a multi-channel application, the typical output stage includes an analog (time-division) multiplexer, a sample-and-hold circuit, an ADC and other possible analog/digital signal processing blocks. Some important design parameters include the number of input channels, the sampling frequency required for each channel and the sampling frequency of the ADC that will depend on its architecture and the required resolution.

A sampling frequency of 15 kS/s per channel with a 10-bit resolution is considered to be sufficient for most scientific and clinical applications [2]. Therefore, a total sampling frequency of 240 kS/s would be required when 16 recording channels need to be recorded at the same time. This would produce a data rate of 2.4 Mbit/s for a 10-bit resolution ADC. The total sampling frequency sets the specification for the settling time of the multiplexer and sample-and-hold circuit, which must be lower than one sampling period. In this case, a settling time lower than 4 µs is required. As we are expecting a large signal swing at the output of each channel, a buffer with very good slew rate and overload recovery time can be placed after the analog multiplexer in order to drive the ADC.

When designing the multiplexer, special care has to be taken with regard to the switching noise, charge injection, clock feedthrough and crosstalk between adjacent channels. For very-low-voltage applications, standard analog switches are not suitable since not enough overdrive is provided to the gates of transistors to be turned on over the whole signal range. Thus, special techniques (e.g. switched opamp [15]) have to be used to overcome this problem in standard CMOS technologies.

F. *The System Architecture*

Several architectures are possible for multichannel neural recording systems. The selection of the architecture depends on the design specifications and the area and power constrains



	Size
M1,2	500/4
M3	60/50
M4,5	7.5/50
M6,7	16.25/1
M8,9	6.5/1
M10,11	30/160

Figure 5. Fully-differential folded cascode input amplifier.

of the application. For example, when the main limitation is the area, we can optimize the channel area and place the multiplexer as close to the inputs as possible. When the main constraint is the power (e.g. wireless applications), we can consider static multiplexing in order to reduce the data rate (transmitting only one channel at a time) and use low-power techniques with low supply voltages. If the main requirement is low noise, we can place a low-noise input amplifier in each channel and consider a fully differential architecture in order to reduce common-mode noise and interferences.

In our design, the noise is the main constraint for the design due to the small signal levels we need to measure. The selected architecture is shown in Fig. 4, which is a fully-differential design with 16 input channels. Each channel consists of a low-noise preamplifier and a programmable fourth-order band-pass filter. The output stage includes an analog time-division multiplexer and an output buffer. The ADC was not included in this first design and is placed later off-chip on the printed circuit board (PCB) (future versions will also include the ADC on chip).

The preamplifier (Fig. 5) is a fully-differential folded-cascode operational transconductance amplifier (OTA) with a gain of 50. The input transistors are operating in the sub-threshold region so than we can achieve very low input-referred noise. A common-mode feedback circuit is required to control the common-mode voltage at the output nodes. The inputs are capacitively coupled in order to eliminate dc offsets coming from the electrode-electrolyte/tissue interface. Additional programmable gains of maximum 12 and 10 are added in the subsequent two stages respectively. The total gain can be selected with 3 bits from 8 predefined values between 100 and 6000.

The low-frequency high-pass filter is implemented with a MOS-bipolar pseudoresistor (formed by a NMOS and a PMOS transistor) and a capacitor placed in the amplifier feedback loop. These feedback elements are also included in the next three stages in order to achieve a very selective fourth-order high-pass filter. The cutoff frequency can be tuned via a digital-to-analog converter that changes the gate voltages of the transistors (i.e. the resistance of the pseudoresistor elements) in order to accept or reject the LFP signal frequencies. A total of 6 predefined cutoff frequencies can be digitally selected with 3 control bits.

The fourth-order low-pass filter characteristic is realized by a cascade of first-order voltage integrators consisting of an OTA and a load capacitor. The load capacitor is implemented as a capacitor array that allows the programming with one bit of two different frequency ranges: one for the LFP signals and another for AP signals. Also, for low-frequency LFP recording, the supply current of the amplifiers is lowered to save power. In total, 7 bits are used to program independently the gain and the band-pass filter of each channel.

For the implementation of the time-division analog multiplexer, an array of standard transmission gates is used to achieve rail-to-rail voltage operation. The multiplexer is controlled by a digital counter in order to sample each channel with a minimum rate of 12.5 kS/s. A differential output buffer is placed at the output of the multiplexer to drive an external load (an ADC or other instrument) of maximum 50 pF.

G. *Simulations*

In order to define the above described architecture, simulations at different levels were performed. Initially, we used VerilogA (standard modeling language for analog circuits) for the modeling of the different blocks in the architecture. These models were used for the architecture definition and the optimization of the design parameters and programmable capabilities. The simulations at system level of the VerilogA models were performed in Cadence Spectre. Finally, the resulting architecture was implemented in Cadence Virtuoso and simulated at circuit level with Spectre.

III. Experimental Results

The 16-channel architecture in Fig. 4 has been fabricated in a 0.35 µm On Semiconductor CMOS technology, which has been selected to keep compatibility with future designs that

TABLE I. Measured Performance Characteristics

Parameter	Measured Value			
	This work	[16]	[17]	[18]
Techn. [µm]	0.35	0.35	0.35	0.18
# Channels	16	32	128	16
Supp. voltage [V]	3.3	3.0	3.3	1.8
Total current [mA]	0.8 (LFP) 1.8 (AP)	2.35	1.82	0.38
Input-ref. noise [μV_{rms}]	2.3 – 2.9	6.9	4.9	5.4
Preamp. NEF	6.2 (LFP) 5.1 (LFP)	9.4	--	4.9
CMRR [dB]	69 (LFP) 65 (AP)	134	90	--
PSRR [dB]	71	62.7	80	--
Gain [V/V]	Prog. 100-6000	Prog. 2500-8000	Prog. 700-1000	3200
Low cutoff freq. [Hz]	Prog. 1-500	Prog. 100-1000	Prog. 0.1-200	100
High cutoff freq. [Hz]	Prog. {230, 6200}	8000	Prog. 2k-20k	9200
Area [mm^2]	25.2	16.4	63.4	2.3

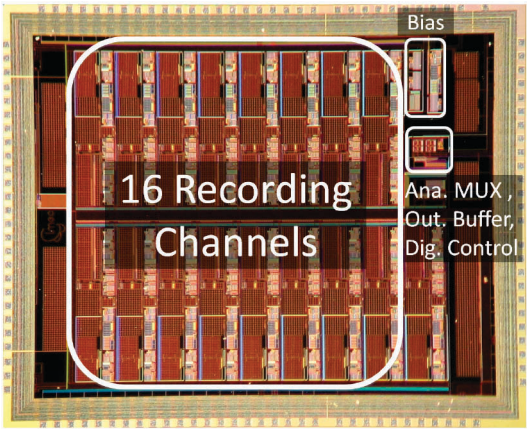


Figure 6. Die photo of the 16-channel neural recording system. The total area is 5.6 mm × 4.5 mm and the core area is 4.1mm × 3.8 mm.

will include stimulation circuits and, therefore, need higher voltage headroom. The capacitors are implemented as metal-insulator-metal (MIM) capacitors and the resistors as polysilicon resistors. The die (Fig. 6) occupies a total area of 5.6 × 4.5 mm^2, with a core area of 4.1 × 3.8 mm^2. The area of one channel is 0.76 mm^2.

A. *Performance Measurement*

The measured characteristics of the neural recording system are summarized in Table I. The chip consumes 1.8 mA from a 3.3 V supply (i.e. 5.9 mW) when the chip is configured to record AP signals, while for LFP recordings the consumption is reduced to 0.8 mA (i.e. 2.6 mW). One channel consumes 70 µA and 17 µA in the two configurations, respectively. The measured input-referred noise is between 2.3 and 2.9 μV_{rms} (integrated from 1 Hz to 6 kHz) for the different programmable possibilities. Comparison with recently reported neural recording systems is also included in this table. This work achieves a good noise level at the expense of higher power consumption, while still keeping an acceptable NEF.

Fig. 7 shows the frequency response of one channel measured with a spectrum analyzer. Approximated gains of 100, 200, 500, 1000, 2000, 3000, 4000 and 6000 can be digitally programmed for all the frequency ranges. The measured -3-dB programmable cutoff frequencies of the high-pass filter are 2.6, 5.6, 13.4, 213, 323 and 572 Hz and the programmable cutoff frequencies of the low-pass filter are 230 Hz and 6.2 kHz.

The common-mode rejection ratio (CMRR) of one channel, measured with a spectrum analyzer as the ratio of the differential-mode gain to the common-mode gain, is 69 dB between 1Hz and 200 Hz for LFP recordings and 65 dB between 300 Hz and 6000 Hz for AP recordings. Similarly, the power-supply rejection ratio, measured as the ratio of the differential-mode gain to the power-supply gain (gain from the power supply to the channel output), is around 71 dB for both LFP and AP ranges.

B. *Recording of APs*

In order to test the functionality of the recording system, signals have been recorded from cardiac cell cultures. Cardiac cell action potentials have the same frequency distribution as

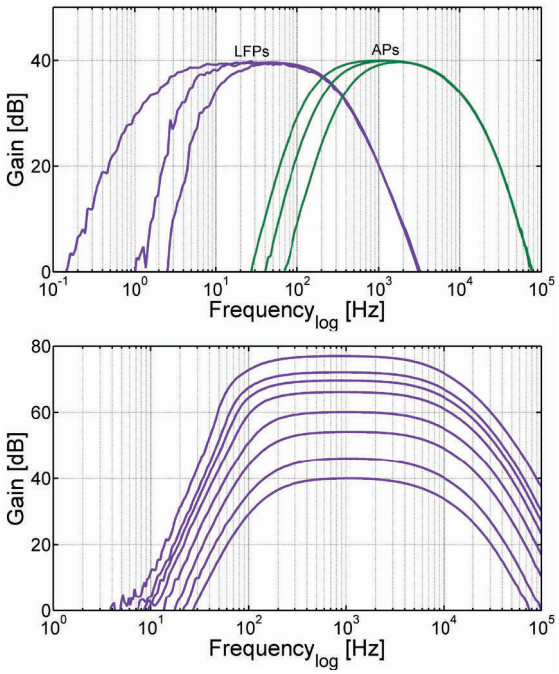


Figure 7. Transfer function of one channel, measured for different bandwidths and gains.

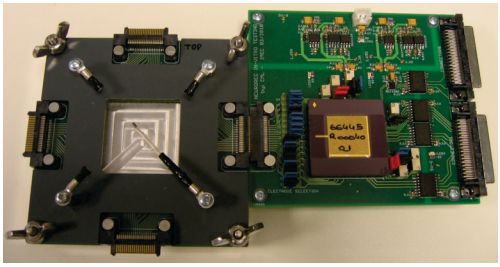


Figure 8. Picture of the *in vitro* setup used for cell activity recording and computer interfacing.

neural signals with slightly higher amplitudes, and they are used in our experiments because of the ease of the cell culturing and the straightforward interpretation of the data. Embryonic cardiac cells from rat were grown for 4 days *in vitro* on top of commercial MEAs (Multichannel Systems) with 30 µm TiN electrodes and on top of micro-fabricated probes with 50 µm TiN electrodes. The setup used for the measurement is shown in Fig. 8. It consists of a structure to contact the MEA (or probe) and a PCB with the recording chip, the ADC and the interface with the computer. In the computer, custom-built acquisition software allows the programming of the chip as well as the real-time transferring, display and saving of the recorded data.

Simultaneous recordings from the 16 input channels have successfully been performed. Signals as small as 30 μV_{p-p} have been detected due to the low input noise levels (around 10 μV_{p-p}). Fig. 9 shows 30-second recordings from four adjacent channels with a gain of 1000 V/V. Nearly synchronized APs can be seen in three of the channels because of the network coupling that exists in cardiac cell cultures [19] through gap junctions. Therefore, if the cells are growing adjacent to each other, the APs will propagate through the cell layer.

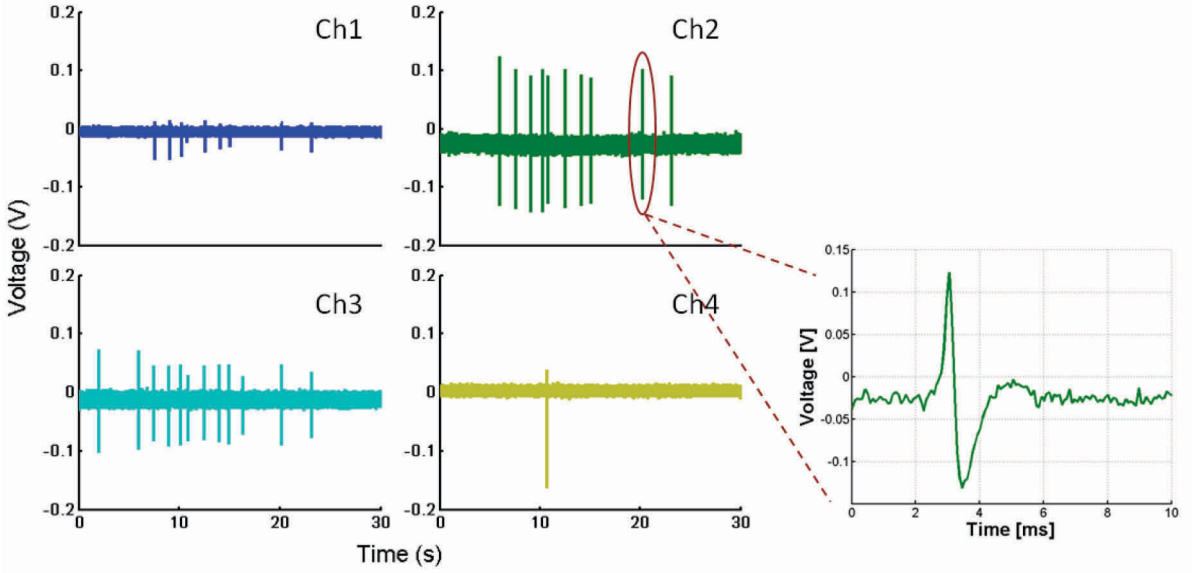


Figure 9. Extracellular recording of APs from four adjacent channels. Cardiac-cell signals are monitored through a 50-µm TiN-electrode probe.

IV. CONCLUSION

This paper has presented the systematic design of a neural recording interface. Different specifications and design aspects have been discussed, pointing out the design criteria for our system. To address the extracted specifications, a low-power fully-differential architecture has been proposed and implemented in a 0.35 µm CMOS process. The experimental results show satisfactory circuit performance, matching the specifications used for the design and the simulation results. The functionality of the recording system has been verified by the multichannel acquisition of APs from cardiac cell cultures. Future experiments include the *in vitro* recording of hippocampal/cortical neuron APs and the *in vivo* recording in rat.

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