On Design of Test Structures for Lithographic Process Corner Identification

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***Abstract*—Lithographic process variations, such as changes in focus, exposure, resist thickness introduce distortions to line shapes on a wafer. Large distortions may lead to line open and bridge faults and the locations of such defects vary with lithographic process corner. Based on lithographic simulation, it is easily verified that for a given layout, changing one or more of the process parameters shifts the defect location. Thus, if the lithographic process corner of a die is known, test patterns can be better targeted for both hard and parametric defects. In this paper, we present design of control structures such that preliminary testing of these structures can uniquely identify the manufacturing process corner. If the manufacturing process corner is known, we can easily attain highest possible fault coverage for lithography related defects during manufacturing test. Parametric defects such as delay defects are notorious to test because such defects may affect paths that are subcritical under nominal conditions and not ordinarily targeted for test. Adoption of the proposed approach can easily flag such paths for delay tests.**

Keywords-photolithography, defocus, Resistance, process corner analysis, test pattern optimization

I. INTRODUCTION

Integrated circuit designs have enjoyed improved performance and reduced power consumption with advancements in semiconductor manufacturing technologies. Historically, the number of manufacturing process steps has increased with every new semiconductor technology generation, while parameter variation requirements become more stringent [1]. As industry ventures into manufacturing devices 22nm and smaller, the requirement of producing defect free dies with minimal functional and parametric variation has become a critical challenge [2].

The focus of this paper is lithographic process variation. Such variations are attributed to lens imperfections, overlay and alignment issues, wafer tilt, optical focus and dosage variations, optical diffraction and reflection from the wafer, and chemical processes to name a few. Impact of lithographic variations can be both random and systematic. Focus variation is an example of systematic source of defects, while chemical processes may result in random variations. Process variations are also characterized by their locality and range. These include lot-to-lot, wafer-to-wafer, inter-die and intra-die variations. Historically, the wavelength of the light source used in photolithography scaled in tandem with transistor feature size. However, since 180nm technology, the wavelength of the light source has not scaled – amplifying the effects of the above sources of variations. Today, 32nm devices are printed using a 193nm wavelength light source. This is known as sub-wavelength lithography.

Lithographic variations induce defects in circuits. They range from incorrect circuit operation to variations in circuit parameters such as gate length, width, and interconnect parasitics. In pre-sub-wavelength era, particulate defects were the predominant defect mechanism. However, continuous scaling of devices has caused feature driven defects to play a greater role in high volume manufacturing. It has been shown that layout related systematic defects, are on the rise for current and future technology nodes [1][2] and they already dwarf random defects today.

As the manufacturing process moved into producing devices of width 65nm and below, the importance of lithographic distortion arose. Distortions caused by lithography occur due to inherent limits of resolution and contrast for a particular imaging system. With continued use of 193nm wavelength light sources for producing polygons of sizes less than the theoretical diffraction limit, lithographic distortions are here to stay [3]. Lithographic distortions predominantly include those that lead to line width roughness (LWR), line end shortening (LES), corner rounding and across the chip linewidth variations (ACLV)[4]. Primary distortion sources classified systematic include spacing between metal lines (forbidden pitches), defocus, exposure dose fluctuations and resist thickness variation. Whereas, line edge roughness (LER) caused by various factors is classified as a random variation inducing interconnect and gate parameter fluctuations [7]. Design for Manufacturability (DFM) tools and mask modification techniques such as optical proximity correction (OPC) are used to analyze and modify designs and mask polygon to overcome predicted layout distortions. Such aids however cannot insulate a layout from distortions due to variations in focus, exposure-dose and resist thickness. [3][4][5].

Lithographic distortions are typically attributed to reduction in polygon width or length [8]. These include change in interconnect and transistor length and width. Such changes can lead to potential opens, shorts, resistive opens and resistive bridges. With increased measures taken today to control the variation in lithography process, majority of defects seen today are resistive opens and resistive shorts. For testing purposes, these type of defects fall under the category of parametric faults. Automatic test pattern generation (ATPG) tools generate test patterns that will be used during the manufacturing test step. For parametric failures, ATPG tools are used to generate delay tests. Delay tests aim to trigger paths in the circuit that cause a difference in propagation delay between good and faulty versions. As the number of paths in a circuit can be exponential, only a set of highly critical paths is tested by automatic test equipment (ATE) to identify faulty sites.

The ultimate goal of any manufacturing test is to screen defective chips by detecting at least one defect during manufacturing test. Manufacturing test generation is driven by

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fault models that either model defects directly or act as surrogates. For parametric faults such as delay defects, it can be observed that the test patterns are highly dependent on the fault site. The locations of the faults in-turn are dependent on where lithographic distortions occur, which in turn depends on focus, exposure dose, resist thickness and similar manufacturing process parameters. With any change in imaging system parameters, a particular location may or may not exhibit distortion. If we gain knowledge of these parameters through direct or indirect measurements, then lithographic analysis may be used to identify exact fault locations. Also, because delay faults can occur on any path depending on litho parameters, often paths that were deemed non-critical during timing analysis become critical on silicon.

A circuit consists of an exponential number of circuit paths. During testing, only critical paths may be targeted. Since the lithographic distortions may affect non-critical paths, thereby making them critical, it is vital to have knowledge of where the distortions are. At this stage, having lithographic process corner information can be of tremendous benefit as it can reveal the location of polygons affected by lithographic distortions. By knowing the manufacturing process corner, the best pattern set targeting an actual set of potential fault locations may be used, increasing fault coverage. Thus, it is important to know the current lithographic process corner during manufacturing test. This is the objective of this paper. We aim to design test/control structures on the die that can be used to read out the lithographic process corner information from silicon. These test structures produce digital values that are read by tester to determine the current process corner which will then be used to apply preselected tests for that process corner.

The paper is organized as follows: a background survey of existing lithographic process calibration techniques and their applications is briefly described in Section II. Section III provides a short description of our experiment and the impact of process variation on defect locations. In Section IV, control structures devised to utilize multiple aspects of lithographic distortion have been described. Section V shows the experimental setup followed by results. Section VI concludes our paper.

II. BACKGROUND

Process corner analysis (PRCA) is a well known technique to estimate the range of parameter fluctuation at various stages of the circuit realization process. It is important to know the range of such variations to perform any kind of parameter characterization in the design phase. Manufacturing process calibration through analyzes has been existent for various applications within the semiconductor manufacturing industry [14][15]. As the thrust of this paper is lithographic fluctuations, we delve into techniques used to analyze such variations.

Process control in lithography is typically performed using metrology techniques. Well known metrology techniques include scanning electron microscopy (SEM), electrical linewidth metrology (ELM) and spectroscopy. SEM scans a region of the wafer using an electron beam. The topography changes on the wafer causes fluctuations in the observed intensity profile. The slope of the intensity profile is used to locate the edge of the feature being scanned. CD-SEM is the most predominantly used method of the three aimed at process control and OPC model calibration [9][10][11]. As SEM has area limitation, ELM technique is used to analyze large regions of the mask. Control structures are drawn with interconnect lines connecting to probe pads. ELM uses probes to measure the change in resistance through an interconnect line due to linewidth fluctuation. There exist two methods to perform CD measurement using ELM. One method measures the change in conductance of the region under consideration; whereas the other method uses the change in resistance at different points with the region. ELM has been proven to be very effective in identifying systematic CD variations [12]. Spectroscopy uses the reflectance of light due to change in wafer topography to identify edge location. Other methods bordering ELM techniques include the use of transistor structures and ring oscillator features to predict process fluctuations using secondary impacts on the control structure parameters.

The problem with CD-SEM is that it cannot be automated. The disadvantage of ELM type measurements is that the user does not have direct value for polygon CD variation, instead, a function of the CD variation [14][11][12]. Due to the on-the-fly requirement of our application, we use ELM based methods to identify the current process corner with acceptable confidence.

III. PRELIMINARIES

The goal of this experiment is to aid ATE tool to effectively identify the current process corner such that the overall test coverage is improved. In this section we first explain the motivation behind this project. It is then followed by a detailed overview on the method of experiment aimed at identifying the correct process corner.

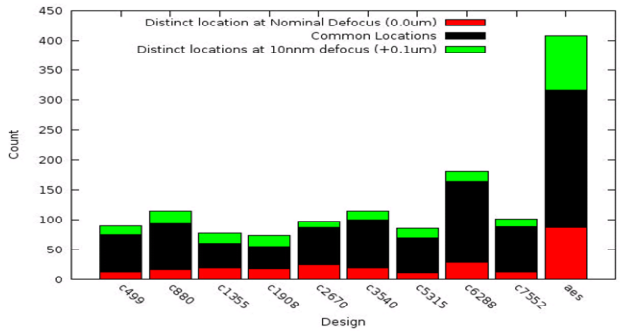

Figure 1 Number of common and distinct potential defect locations with small focus variation

A. *Fault Coverage under process variation*

As described in the introduction section, change in process corner due to various issues during the manufacturing process is a well known phenomenon. The impact has been observed to be present at every stage of the circuit design process. It is also important for processing of the die after manufacturing step.

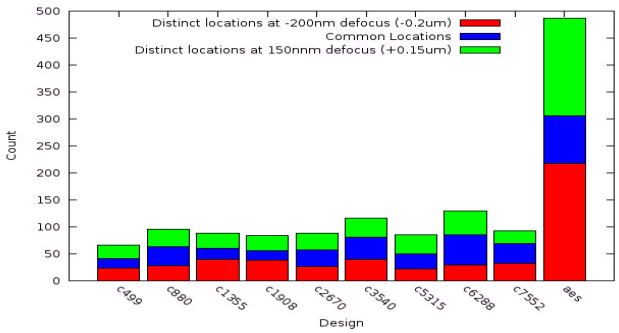

Figure 2 Number of common and distinct potential defect locations with large focus variation

The manufactured die goes through a battery of tests ranging from wafer sorting, burn-in tests, class tests, manufacturing tests and quality assurance tests. Each type of test aims at targeting a particular set of weaknesses of the die. Test patterns to be applied during the manufacturing test are chiefly aimed to perform stuck-at and delay (transition) tests. Test patterns devised for these failures are tied to potential opens, shorts, resistive opens and bridges that may occur due to various reasons. Lithographic distortion is a major source of open and bridge defects.

To illustrate the importance of this problem, we ran lithography simulation on a given layout to observe the change in location of defects due to change in lithography imaging parameter. As many sources of imaging errors are typically consolidated as defocus, we consider focus fluctuations as the major contributing factor. Figure 1 shows the number of common and uncommon regions of potential defects for multiple designs when focus is set at nominal and 100nm above the nominal focal position. The layouts used here were mapped to 45nm technology node. Figure 2 on the other hand shows the similar defect counts for defocus at 200nm below the focal point and 150nm above the nominal focus. The yellow region indicates an intersection of locations, whereas the red and blue regions indicate uncommon regions. A comparison of defects locations using net information will result in higher number of common regions, as a logical net can run through multiple metal layer masks. In the data plotted, the comparisons were performed between specific polygon coordinates against the same mask.

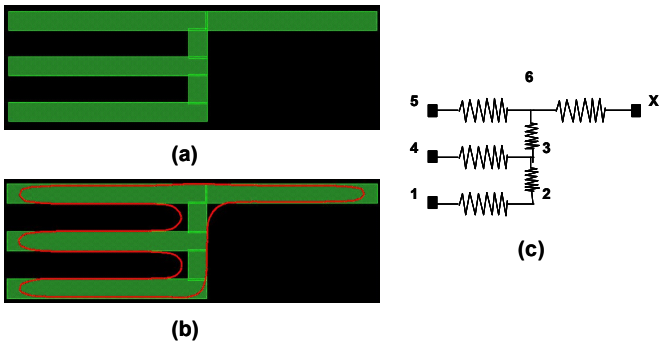

Figure 3 Illustration of a simple control structure and its resistive network.

It can be observed from the plots that a small change in imaging system focus can lead to a small change in defect locations. On the other hand, a substantial change in defocus will result in reduced number of common regions of error for the same design. Hence, this calls for an effective on-the-fly probing based process.

B. Control Structure based Analysis

We follow a technique quite similar to electrical linewidth metrology (ELM). But as the aim is to use on-the-fly probing for process corner identification, the prime constraint is the limitation on the number of probe points. Hence, we limit the number of control structures that will be placed around the design to 9.

Instead of reading the resistance through an interconnect, probes are used to measure voltage differential with respect to reference structures. Each probe will read either a value 0 or 1 based on the difference between the voltage obtained through the control structure and a reference structure. A simple control structure is shown in **Error! Reference source not found.**. Node 2 is connected to supply voltage VDD and Node 1 & Node 5 is connected to supply voltage VSS. Node X is the output node to be connected as an input to a voltage comparator such as an OP-AMP. The control structure here creates a resistive divider circuitry. As the line width and lengths change with defocus, the resistance of the interconnect wires change. This causes a change in voltage at node X. Based on the voltage from a resistive divider, and another reference circuit, the output of the OP-AMP will be a 0 or a 1. Upon reading the values from probe points connected to the OP-AMPS, the 10 bit digital readout is compared to a pre-computed lookup table. The pre-computed lookup table stores distinct 10-bit values for each process corner for confident identification.

As similar identification may not be achieved due to other inter-die fluctuations over the existing defocus, the probed digital readout is compared with all existing 10 bit values in the pre-computed lookup table. The one with the least hamming distance from the obtained value is identified as the current process corner.

IV. LITHOGRAPHY CONTROL STRUCTURES

Design rules were established to prevent features from being placed at distances that can cause non-ideal patterns being created on the wafer. Each design is run through a rigorous set of design rule checks (DRC) during the circuit realization and tape out stages. Similarly, physical design process uses layout enhancements for manufacturing (LEM) techniques to mitigate process variation effects in today's layout. By avoiding DRC and LEM, we can engineer test structures that are sensitive to the lithographic process and highly sensitive to variation in them. Specifically, we take advantage of line end erosion (LEE), line-end shortening (LES), line-edge roughness (LER) and line placement near forbidden pitches to increase sensitivity.

In our experiment, we design multiple control structures to utilize the various systematic variation sources in lithography. In this section we describe in detail the type of systematic variation source being utilized and the control structures used for each case.

A. *Using Forbidden pitches*

During projection printing, light passing through a feature with high transmittance causes a diffraction pattern on the image plane. The diffraction pattern of a single feature extends on both sides to approximately 3 times the wavelength o the light source. If a feature exists within this region on any side of the current polygon being imaged, interferences between the diffraction patterns may be present. A constructive interference occurs when the two diffraction patterns are in-phase leading to increased width. Destructive interference on the other hand, happens when the patterns are out of phase with each other causing metal width reduction.

It has been shown that forbidden pitches (FP) are pitches at which destructive interference between adjacent metal lines are at their maximum. At 130nm, the reducing in metal width for features placed at FP were 10%. At 45nm it was observed to be >70% and over a range of pitches. We utilize this change in interconnect width for features placed at forbidden pitches to produce a voltage differential. The widths of interconnect features constituting the control structure vary both with forbidden pitches and also at different defocus values. It might be possible to produce an acceptable feature placed at forbidden pitch but exposed at a non-nominal focus value. In each of the illustrated control structures, the length of the interconnect line is made 5X-10X the width of the structure to avoid LWR effects.

B. *Using Corner Rounding & other proximity effects*

Corner rounding in photolithography is defined as an irregularity in printing polygons with "T" and "L" shaped corners. The other proximity effects include bridging of metal lines due to increased constructive interference between adjacent lines placed very close to each other (typically at minimum spacing specifications).

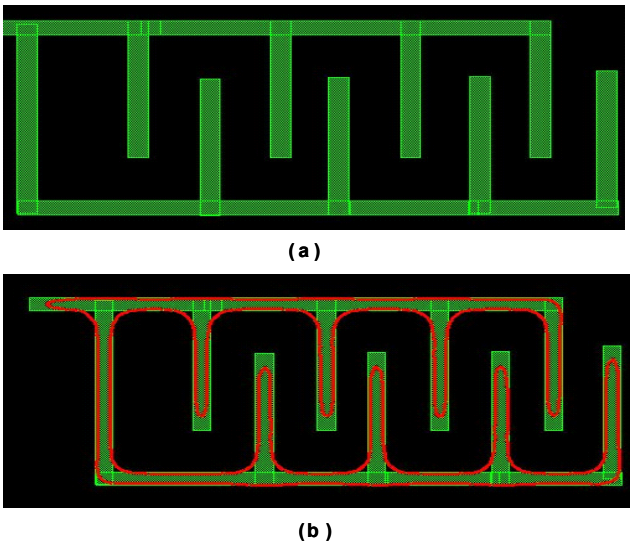

Figure 4 Snake-like (Comb) test circuitry and its post-lithography contours

A very well known structure is used to estimate CD variation due to systematic proximity effects, namely the spiral structure. In traditional ELM based metrology, multiple probes are connected at different interconnect lengths for measurement. The measurements are later used to calibrate the process for fluctuations caused by inter-die, shadowing, wafer alignment or etching-related defects. In this work, we use the spiral structure to perform the same resistance change-based voltage differential measurement. Other variants of the spiral structure such as resistive comb divider have been implemented. An illustration of the comb divider and its resistive model is shown in Figure 4

C. *Using CMP fluctuations*

Chemical Mechanical Polishing (CMP) is a process through which metal and dielectric layers are planarized to the required thickness. Research shows that the post-CMP thickness is dependent on the placement of current and all underlying layers [6]. Isolated lines lead to decrease in final thickness (dishing) and dense features lead to erosion of the planarized material (erosion). Both these problems lead to defocus issues.

4 structures have been designed to utilize CMP induced interconnect height variation in the presence of defocus. Multi layer structures connected to each other through vias have been drawn. Each layer either consists of isolated lines or dense lines forming the structure. An example structure consisting of dense metal 3 and metal 4 laid on top of each other is shown in Figure 5 .

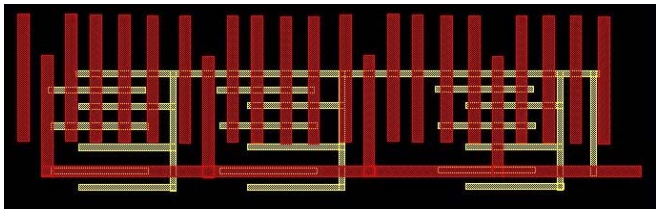

Figure 5 Illustration of control structure targetting CMP induced fluctuations

D. *Poly-gate distortions*

Lithographic distortions also occur for poly-gate and diffusion features. Change in width and length of features on a poly-gate and diffusion affects the transistor channel length and width. These distortions cause changes to transistor parameters and hence voltage fluctuation across it. It is known that poly-gate masks, when simulated produce a non-rectangular gate (NRG). It means that the channel length varies over the width of the device. Also, rounding caused by the diffusion region lying underneath the poly layer causes change in transistor width. We use existing models to arrive at a particular transistor width and length. More in-depth analyses of various available models on these effects are available in the literature [3].

We use pass transistor-based test structures to utilize the variations in transistor length and width due to lithographic distortions. A series of parallel pass transistors are drawn very close to each other inducing proximity-based changes to the drawn length and width. Similar to the above 3 cases of structures, the control structure voltage drop is compared with a reference voltage to generate a 0 or 1. This output value will be probed for process corner analysis.

V. MEASUREMENT SETUP & RESULTS

Control structures are drawn to 45nm technology node specifications. The control structures were initially drawn and simulated separately to create the digital lookup value at each process corner. Nine defocus process corners were selected for this experiment. Four defocus values above the nominal focus and four defocus values below the nominal focus values.

For each control structure, the length and width of contributing polygons are measured through lithography simulation. As 3-dimensional simulation is not being performed, the height of the feature cannot be obtained from the lithography simulation. We instead use a pre-characterized library of base widths at each defocus to estimate the height of the feature after the resist develop stage. This pre-characterized library/table contains height, sidewall angle and base CD values at multiple spacing and defocus for a polygon of particular width. The following two sections discuss the experimental results in detail. The first section describes some sample control structures, their constituent polygon dimensions and their respective resistance values at multiple defocus values. Section B shows implementation of control structures in the design and the confidence level of corner identification.

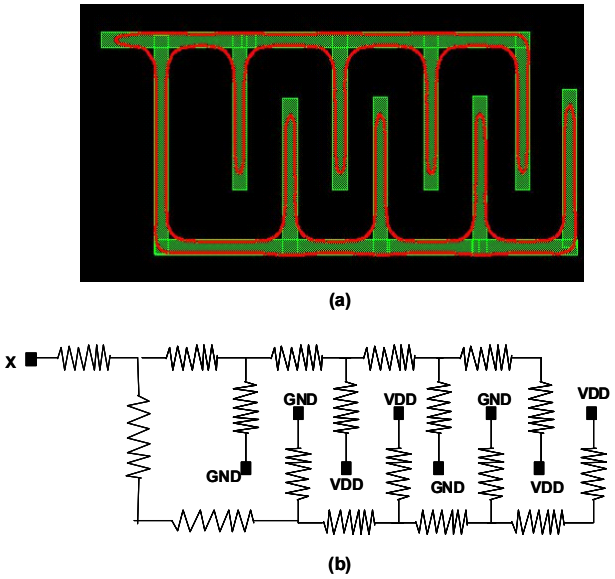

Figure 6 An illustration of (a) a comb resistive divider and (b) its resistor network.

A. Probing

Let us look into two control structures in detail here. Control structure A is a modified spiral structure, otherwise termed as a "comb" structure. As the illustrated in Figure 6 (a) shows, there are multiple fingers on each side intertwined to each other. In circuit terms, it forms a deep resistive divider circuitry, as shown in Figure 6 (b).

The drawn layout is simulated at multiple defocus values ranging from -0.2µ to +0.2µ. The symbols "+"and "-", indicate focus positions above and below the nominal focus value respectively. At each defocus value, the change in dimension of every polygon is noted. As mentioned before, the width of a polygon is used as the base CD width to obtain the height at the given defocus and spacing specification. The dimensions of a polygon are used to estimate its resistance. The circuit information is now populated and simulated using HSPICE to obtain the output voltage. It is to be noted that certain nodes of the comb structure are connected to supply voltages VDD and GND to form a resistive divider.

TABLE I. OUTPUT VOLTAGES AT NODE X FOR CONTROL STRUCURES AT VARYING FOCUS

	Voltage (mV)								
Defocus (µm)	-0.25	-0.2	-0.15	-0.1	0.0	+0.1	+0.15	+0.2	+0.25
CS_A	533	535	560	559	557	580	549	524	574
CS_B	342	287	261	256	265	305	327	0	0

At every defocus value, the output node voltage is recorded. On comparison with digital values generated by other control structures, the required reference voltage is decided and a reference structure is drawn to produce the same. As the reference structure is required to produce the same voltage at different defocus values (avoid fluctuations in its dimensions), it is usually drawn at larger than minimal width and spacing. The output node voltages of control structure A at every defocus value is listed in TABLE I. .

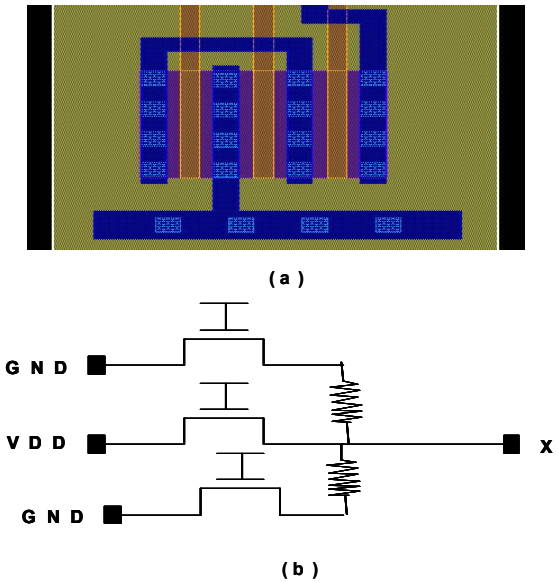

Figure 7 Sample layout and circuit description for a pass transistor based control structure targetting NRG variation

Control structure B is a pass transistor-based resistive divider network. It aims at utilizing lithographic distortions in poly-gate layer and diffusion layer masks. Continuing from section IV D, poly layer and diffusion layer distortions are modeled using a simple NRG model. The NRG model provides a single gate length and width value that satisfies the ON/OFF drain current of any non-rectangular transistor. This NRG transistor is used in the circuit version of the control structure to perform SPICE simulation to arrive at a voltage value. Similar to control structure A, a reference structure that withstands defocus changes is drawn

to provide the required reference voltage in this case. TABLE I. shows the obtain voltages at multiple defocus values.

Once every control structure has a 9-bit defocus process corner value, they are stored in a lookup table. The lookup table consisting of values from all control structures is shown in TABLE II. . It can be observed that for every defocus value, a 10-bit distinct digital value can be obtained. Care was taken during pre-characterization phase in choosing the reference structure for each control structure so that no two rows in TABLE II. have the same digital value.

B. Corner Identification

Simulation of corner identification during ATE probing phase is done by implementing the control structures on existing designs. This can also be used to estimate the increase in area of the design.

The design exchange format (DEF) file of each design is modified to accommodate the control structures. Each control structure is carefully placed at varying locations around the design. The design is simulated and the resistance values are similarly obtained. For each control structure, the output voltage is compared to the reference voltage to arrive at a digital value. The obtained 10-bit value is used to map to a process corner using the lookup table. As it is possible that some digital values might get flipped due to other random variations, exact matches to a process corner may not be obtained at times. The hamming distance between the obtained 10-bit value and each value in the lookup table is computed. The corner with lowest hamming distance is determined to be the current process corner.

TABLE II. DIGITAL READOUT FOR CONTROL STRUCTURES AT MULTIPLE PROCESS CORNERS

	Digital Readout									
Defocus (µm)	**CS0**	**CS1**	**CS2**	**CS3**	**CS4**	**CS5**	**CS6**	**CS7**	**CS8**	**CS9**
-0.25	0	1	0	1	0	0	1	0	0	0
-0.20	0	0	1	0	0	0	1	0	0	1
-0.15	0	0	0	0	1	0	0	0	0	1
-0.10	0	0	0	0	1	1	0	0	0	1
0.0	0	0	0	0	1	0	0	0	1	0
+0.10	0	0	0	0	1	1	0	1	1	1
+0.15	0	1	0	1	0	1	0	0	0	1
+0.20	1	0	0	1	0	0	1	0	0	0
+0.25	0	0	1	1	0	0	0	1	0	0

The deciphered process corners validated with the set of faulty locations. We repeated the experiment by changing the location of the control structures to observe the confidence level of process corner identification. In some outlying cases, the process corner identification by certain configurations was marginally inaccurate. It was found that the digital values read out by control structure that used CMP distortions were affected by increased density in the neighborhood. The increase in area for each design was found to <0.3% including the pad area.

VI. CONCLUSION

In this paper, we presented a DFT technique for digital readout of lithographic process corner. The design exploits increased sensitivity to lithographic distortions near forbidden pitches and hillocks and troughs that may result from non-uniformity in density during CMP process. Knowledge of lithographic process corner helps better target test patterns, particularly for delay faults as the increased delays may affect any net including non-critical ones, which may not ordinarily have been targeted for delay testing. Experimental results illustrate the changes in number and location of defect sites with variation in focus. We demonstrated that carefully designed and placed layout polygons can form effective test structures in identifying the current lithographic process corner. The design overhead including required pads is estimated to be less 0.3% of the total chip area for ISCAS benchmarks.

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